cold to hot and the TED's from a chilling condition to a heating condition. An initial temperature nonuniformity is present when the fluids are switched. This nonuniformity is removed by the closed-loop controller. The MSE is 0.41.

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Applications of Total Reflection X-Ray Fluorescence to Analysis of VLSI Micro Contamination

Bor Wen Liou and Chung Len Lee

***Abstract*—This paper demonstrates the microcontamination analysis on wafers after they went through the conventional ULSI processing steps, by using the vapor phase decomposition/total reflection X-ray fluorescence (VPD/TXRF) technique. It was found that the wafer location in the holding cassette during the chemical cleaning step affected the cleanness of the wafer, and the class 1 environment was not enough to keep the wafer to a contamination level below 5×10^9 atoms/cm^2 for three days storing. The breakdown characteristic of a gate oxide was shown to be closely related with the cleanness of the surface of the oxide.**

I. Introduction

The drive toward smaller device geometry and higher yield in ULSI processing requires strict process control to reduce particles and metallic contamination since these particles and metallic contamination cause defects on devices, severely affecting device electrical characteristics. Thus, microelectronic ULSI manufacturing requires a high level and quality clean-room environment in the whole range of semiconductor device fabrication. For example, for 64M DRAM production, the tolerable level of metal contamination on a wafer surface is typically below 10^{10} atoms/cm^2 [1], [2]. To assure the high level of contamination control, various techniques had been developed to monitor particles and metallic contamination on the surface of wafers during fabrication steps. For example, the vapor phase decomposition–atomic absorption spectroscopy (VPD/AAS), the vapor phase decomposition–inductively coupled with the plasma spectrometry (VPD/ICPMS), and surface photo-voltage (SPV) are used to characterize the level of a surface metallic contamination [3], [4]. However, these techniques are not suitable for multielement detection since it requires a tedious sample preparation process. Recently, the vapor phase decomposition–total reflection X-ray fluorescence (VPD/TXRF) spectroscopy became a popular technique to analyze the surface contamination of silicon wafers because it is a nondestructive measurement and has a high detection sensitivity up to 10^8 atoms/cm^2 [5], [6]. For this technique, the VPD is used to collect the metallic contamination into a dot of metallic residue and the TXRF directs a low incident angle X-ray beam onto the residue to excite fluorescence which is detected to identify the residue metallic species.

In this brief, the VPD/TXRF is shown to be a powerful technique to monitor the microcontamination of wafers after they were cleaned in a conventional chemical cleaning station or kept in a conventional wafer stock box for various lengths of time. It is shown that the location of wafers in the holding cassette when they went through the cleaning step affected the cleanness of the wafers, and the storing environment for wafers was critical in determining the cleanness of wafers. Also, the VPD/TXRF technique was used to identify the close relationship of the I–V characteristics, especially the breakdown characteristics, of a gate oxide with the cleanness of the surface of the oxide. All the contamination data were found to result in degradation of the final probe yield of the product. This demonstrated the powerfulness of the VPD/TXRF technique and also revealed the deficiency in the conventional wafer cleaning step and stocking for contamination control.

Manuscript received April 17, 1998; revised October 2, 1998. This work was supported by the National Science Council of the R.O.C. through Contract NSC-83-0404-E009-017.

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Publisher Item Identifier S 0894-6507(99)03773-2.

II. Measurement Procedure of the VPD/TXRF Technique

In all the experiments of this work, 8-in p-type of a resistivity 2.5–3.2 Ω-cm (100) wafers were used. For the VPD/TXRF system used in the experiment, the VPD system was made by GeMeTec Company [3], [5] and the TXRF system was an Atomika [3], [7] 8010 model which used a tungsten source emitting a W-L_β X-ray beam. The beam diameter was 8 mm and the detector used was a Si(Li) single-crystal detector. The angle of the incident X-ray beam was 2 mrad and the measurement time was set to be 1000 s.

III. Monitoring Wafer Cleanness after Chemical Station Cleaning

Much effort has been made to improve the cleaning of wafer by using different cleaning solutions and by adjusting the cleaning conditions. In this experiment, it was to monitor cleanness of wafers after they were put through the standard cleaning process in wafer cassettes by using the VPD/TXRF technique.

Two sets of cassettes of wafers, each of 25 wafers, were cleaned together by a 5 : 1 mixture of sulfuric acid solution and hydrogen peroxide (SPM) solution. Then, these wafers were cleaned by using SC-1 ($NH_4OH : H_2O_2 : H_2O = 1 : 4 : 20$) and by using SC-2 solution ($HCl : H_2O_2 : H_2O = 1 : 1 : 5$) at 70–85 °C, respectively [9], [10]. Following this, the wafers were cleaned with the FPM solution ($HF : H_2O_2 : H_2O = 1 : 10 : 100$) again. Between the above two cleaning steps, the wafers were over-flow-rinsed. Finally, the wafers were spin-dried. The wafers were then measured, the particle counts by using a KLA-Tencor 301 laser-based wafer surface scanner, and the metallic contamination by using the VPD/TXRF system.

In Fig. 1, the results of the measurement for the 50 wafers of the two cassettes in terms of the wafer location inside the cassettes are shown. The wafer location in each cassette is that each wafer is numbered sequentially with number one being the wafer with its polished side facing out. The particle-counts of the particles of the size larger than 0.2 μm on each wafer were typically less than ten for the all measured wafers. It is seen that the wafer-to-wafer variation of the iron contamination and particle counts appeared to be location-dependent within the cassette. The greater the number of

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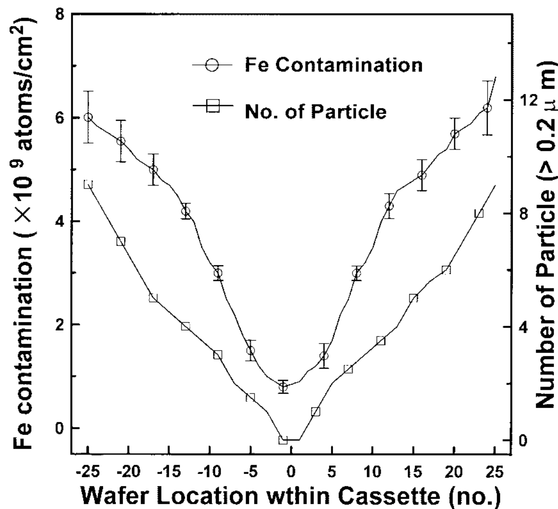

Fig. 1. Microcontamination levels of wafers in terms of their locations inside the cassette during the cleaning step.

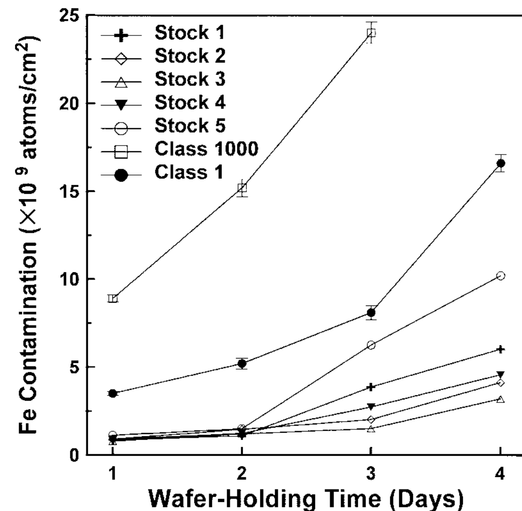

Fig. 2. Fe contamination level of the wafer in terms of the wafer-holding time for different stocking conditions.

the wafer location, the more the metallic contamination and particle counts. Since wafer one was at the center while wafer 25 at the peripheral position of the chemical station, the chemical cleaning-solution transportation and the DI water wafer rinsing at the center were more effective than that at the peripheral location of the chemical station. There was about eight particle counts and 5×10^9 Fe atoms/cm^2 contamination level difference between the center wafer and the peripheral wafer after the chemical station cleaning. This resulted in approximately 5.5% yield loss at the final wafer-probe production stage as our production yield statistics showed.

IV. Cleanness Monitoring for Wafer Stocking

During the wafer processing, it is very difficult to continuously process the wafer without interruption due to facility and manpower limitation. Wafers are usually stored in specially conditioned environments such as wafer stocks. This experiment aimed to monitor the cleanness of wafers which were stored in such stocks. The results were compared with those wafers which were just exposed to the clean room environments of classes 1 and 1000.

Wafers were first chemical-station cleaned as in the previous sections and then stored in wafer stocks and in classes 1 and 1000 clean rooms for various lengths of time, and then their iron contamination levels were measured by the VPD/TXRF system. Fig. 2 shows the iron contamination levels in terms of the length of the storing time for different storing conditions. As was expected, as the storing time increased, the contamination level increased. The wafers stored in the class 1000 clean room had the highest contamination level, those in the class 1 clean room had the next contamination level, and those in wafer stocks had the least contamination level. For wafers stored in wafer stocks, it seems that even four days storing still could keep the contamination level below 5×10^9 Fe atoms/cm^2.

V. Correlation of Oxide Breakdown with Oxide Cleanness

Oxide film is one of the critical layers in determining device reliability. Among many oxide characteristics, the oxide breakdown voltage is one of the most important characteristics to be considered. In this experiment, the oxide cleanness with the oxide breakdown voltage was studied to find their correlation.

In this experiment, the nMOS capacitors were fabricated. The devices were made by first RCA cleaning the p-type 5×10^{15} cm^{-3} wafer. After the cleaning, the wafers' metallic contamination levels were measured by using the VPD/TXRF system. All the measurements showed no detectable metallic contamination. After that, the wafers were then thermally grown an oxide of 8 nm in a dry O_2 ambient at a temperature of 900 °C in a double-walled tube furnace. After oxidation, the wafers' metallic contamination was then measured again by the VPD/TXRF system. Some metallic contamination was detected which was believed to be due to the introduction of the carrying gas or the furnace. Following this, phosphorus-doped polysilicon was deposited and the photolithography was applied to form the capacitor structure. Aluminum was sputtered and alloyed at the backside of the wafers to form the contact. The capacitors' I–V characteristics were then measured with a well-shielded HP 4145B semiconductor parameter analyzer.

Fig. 3 shows the I–V characteristics of several nMOS capacitors in terms of their measured Fe contamination levels, which were 1.2×10^9, 8.2×10^8, 5.4×10^8, and 2.5×10^8 atoms/cm^2, respectively. It can be seen that the Fe contamination affected the leakage current and breakdown voltage. The larger the Fe contamination was, the higher the leakage current and the lower the breakdown voltage existed. However, the Fowler–Nordheim tunneling region of I–V curves for all samples merged together, and the slopes of the tunneling region seemed to be the same. This showed that the Fe contamination did not affect the barrier height of the gate-oxide of the MOS capacitors. Furthermore, the breakdown voltages of these capacitors were intrinsic, which were referred as "good capacitors." That means that the Fe contamination does not cause weak points in the oxide to cause early breakdown [11]–[13], but to cause the oxide to be susceptible to electron trap generation to cause breakdown. The statistical breakdown voltage of nMOS capacitors in terms of the Fe contamination of the oxide film is shown in Fig. 4, where each data point represented the average value of at least ten samples and the scatter value of each data point was about 5%. The breakdown voltage is clearly seen to decrease with the increase of the Fe contamination. For the data shown in this figure for the samples of the 2.5×10^8 and 1.2×10^9 atoms/cm^2 contamination levels, it represented a 4.2% wafer-probe yield difference of the final product as our production testing results showed.

VI. Conclusions

Success in ULSI manufacturing tracks the ability to control the microcontamination in factories of a company. The VPD/TXRF

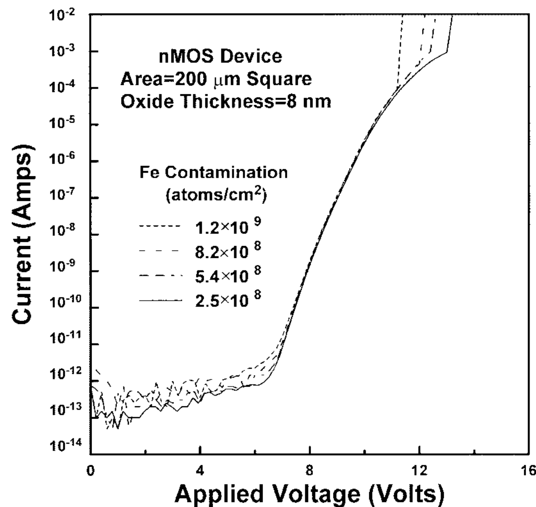

Fig. 3. I–V characteristic of gate oxides for different Fe contamination levels, i.e., 1.2×10^9, 8.2×10^8, 5.4×10^8, and 2.5×10^8 atoms/cm^2, respectively.

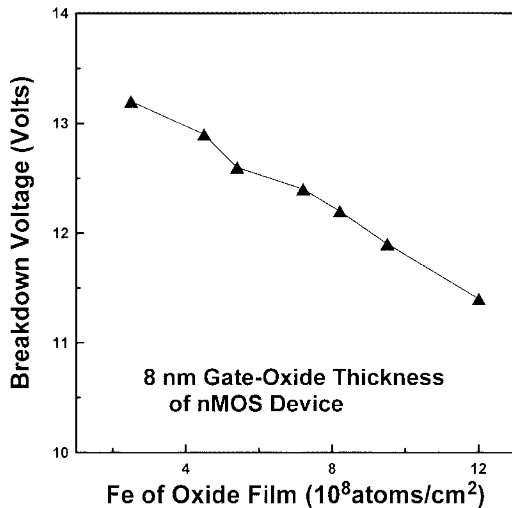

Fig. 4. Breakdown voltages of the gate oxides versus their Fe contamination levels.

analysis technique is a very effective method to monitor cleanness of wafers during ULSI processing steps. In this paper, it has been shown how the technique was applied to monitor the cleanness of wafers when they went through cleaning station, storing in different stocking conditions, and to correlate the wafer oxide cleanness with the I–V characteristics of MOS devices. The study provides us understanding on the microcontamination control of chemical station cleaning, wafer stocking, and the I–V characteristics of the gate-oxide with the surface metallic contamination and their effects on degrading the production yield. That is, the contamination level of wafers depends upon their location inside the cassette during the chemical station cleaning. For wafer storing, class 1 environment is still not enough to keep the wafer to a contamination level below 5×10^9 atoms/cm^2 for three days storing, and for a gate oxide device of a breakdown voltage greater than 15 MV/cm, it needs an Fe contamination level below 1×10^9 atoms/cm^2.

ACKNOWLEDGMENT

The authors would like to acknowledge the technical support of the Vanguard International Semiconductor Corporation.

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