High-Speed Optical Receiver with Soft Decision ISI Cancellation

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***Abstract*—Due to the stimulating success in developing optical amplifiers, intersymbol interference (ISI) will become the dominant limit on both bit rate and transmission distance in long-haul optical fiber communication systems. Here we present a receiver with "Soft Decision ISI Cancellation" (SDIC) to deal with ISI in high-speed lightwave systems. The analytical and simulation results show that the transmission distance can be doubled with SDIC. In addition, the receiver with SDIC allows the ISI cancellation circuit operating with processing and propagation delay much longer than 1-b period. Therefore, it is very promising in very high bit rate optical systems.**

I. Introduction

In the area of optical fiber communications, fiber loss and dispersion are two main constraints on the maximum bit rate and transmission distance. Recently, the problem of transmission loss has been significantly relaxed by the introduction of erbium-doped fiber amplifier. Therefore, transmission loss will no longer be a critical issue in system design whereas the intersymbol interference (ISI) caused by fiber dispersion, will be treated as the limiting factor in future long-haul high-speed optical systems.

The receiver architecture proposed by Personick [1] forces the Fourier transform of the output pulse be of raised-cosine shape. In time domain, the output of the neighboring pulses will be zero at the sampling instant of the decision bit. Hence this equalizer can completely eliminate ISI. However, in order to compensate high-frequency components of the transmitted signal, the zero-forcing equalizer inevitably passes excessive noise components which reduces the signal-to-noise ratio.

Tradeoff between the minimization of noise and ISI had been made by using Chernoff–Bound approximation to optimize the equalizer [2]–[4]. The optimization does improve performance analytically, but the resultant filter is too complicated to be implemented practically. Furthermore, the filter is linear so it cannot deal with nonlinear distortion in a lightwave channel such as the chirping of a semiconductor laser.

A promising way to cancel both linear and nonlinear ISI is taking discrete-time electrical signal processing such as maximum likelihood (ML) sequence estimation or decision feedback [5]. The best and well-known ML sequence estimation, the Viterbi algorithm, is unfortunately not suitable for high-speed lightwave systems because of limited electronic speed. The nonlinear cancellation (NLC) based on decision feedback algorithm was introduced by Winters and Gitlin for optical communication systems [6]. Before deciding a bit, the NLC detector first estimates total ISI contributions due to neighbor bits through a lookup table. Second, the ISI level is fed back to adjust the decision threshold. For every decision bit, the above two steps must be concluded in a time much less than 1-b duration to ensure a correct decision. For optical communication systems with gigabit per second bit rate, however, the bit duration is less than 1 ns. In addition, the feedback switching transients tend to corrupt the input analog signal. Therefore, the NLC circuit is difficult to implement and/or is complicated [7].

In this paper, we present the "Soft Decision ISI Cancellation" (SDIC) algorithm to eliminate linear and nonlinear ISI. It has excellent performance and is easy to be implemented at high transmission rate above gigabit per second without much circuit complexity. Unlike the previous NLC technique, the key idea of SDIC lies on the fact that it is not necessary to do ISI cancellation for every bit, we merely cancel ISI for those marginal bits near the decision threshold. In other words, whether to do ISI cancellation or not is soft decided that the ISI cancellation process is actuated only when the signal level is near the decision threshold. Therefore, a much longer processing and propagation delay time in the ISI cancellation circuit is permissible and the cancellation circuit can operate at a lower speed than the transmission bit rate. Thus the present algorithm is quite suitable for high-speed optical systems. The analysis and simulation results show that SDIC can even double the transmission distance while keeping at the same bit error rate (BER).

There are several differences between the NLC technique and the SDIC algorithm. First, the NLC technique continuously performs ISI cancellation for every bit whereas merely marginal bits near the decision threshold are treated in the SDIC scheme. Therefore, the permissible processing time of the SDIC scheme is inherently much longer than that of the NLC technique because the occurrence probability of a marginal bit is very small. Second, the NLC technique can employ multiple decision elements and look-ahead computation to increase permissible propagation and processing delay [7]. However, the circuit complexity increases about L times for L-fold increases in the permissible delay. For the SDIC technique, the permissible delay can be easily extended with little increase in circuit complexity. Third, theoretically the NLC technique will have better performance than the SDIC scheme because the ISI is canceled for every bit. And the NLC technique works in the presence of large ISI whereas

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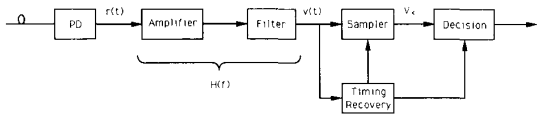

Fig. 1. Optical receiver block diagram.

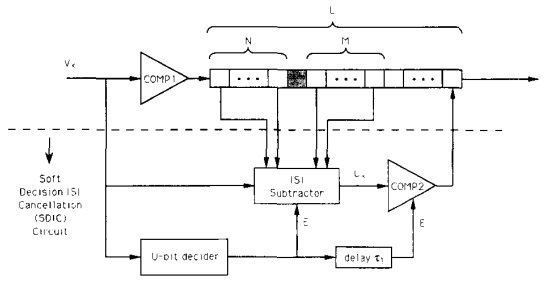

Fig. 2. Decision circuit with soft decision ISI cancellation.

the SDIC scheme works only when the ISI is small. However, because the contribution to bit error rate due to ISI mainly comes from those marginal bits near the decision threshold and the presence of large ISI is seldom found, the SDIC scheme should have nearly the same performance as the NLC technique in practice.

In Section II we show the receiver block diagram and its operation. The performance of the SDIC algorithm is analyzed in Section III by evaluating the error probability. Next, a computer simulation is executed to verify the performance and the results are shown in Section IV. Finally, we present conclusions for this paper in Section V.

II. System Architecture

Fig. 1 shows the block diagram of the optical receiver with SDIC. It is the same as the usual optical receiver except that SDIC is included in the decision circuit. The photodiode (PD) converts the optical power to electrical current and adds noises at the same time. In principle, to minimize noise the impulse response of the transfer function $H(f)$ of the cascade of the amplifier and filter should match the input pulse shape, i.e., a matched filter. However, a matched filter will spread each pulse and increase ISI. Therefore, $H(f)$ should be chosen to reduce noise but not to significantly increase ISI. In general, it may be a low pass filter with appropriate bandwidth.

Assume the timing recovery circuit is ideal without jitter, so after sampling, the signal is converted to discrete samples ready for decision. The decision circuit with SDIC is shown in Fig. 2. Above the dashed line is a one-threshold comparator COMP1 followed by several shift registers. Below the dashed line is the SDIC circuit which selectively performs ISI cancellation. The SDIC circuit is composed of a U-bit decider, an ISI subtracter, and another one-threshold comparator COMP2.

The operation of the decision circuit is described as follows. As shown in Fig. 2, the kth sampler is fed into COMP1 and the SDIC circuit. The threshold of COMP1 is chosen optimally for signals with ISI. The outputs of COMP1, we call them the first decision bits, are stored in the shift registers. On the other hand, the U-bit decider determines whether a bit needs ISI cancellation or not. If the kth sampler is near the decision threshold of COMP1, it is recognized as an "Undetermined bit" (U-bit), the output of the U-bit decider enables the ISI subtracter to cancel ISI from the previous M and next N neighboring bits, then the ISI canceled sampler comes to COMP2 to make the second decision. Note that the threshold of COMP2 is chosen optimally for signals without ISI. The second decision then replaces the first decision in the register at the appropriate time. And the delay τ_1 is used for accurate replacement timing. Otherwise, the kth bit is recognized as a "determined bit" (D-bit). In this case the SDIC is not actuated and the first decision is unchanged. Thus not all the bits but those near the decision threshold of COMP1 need ISI cancellation and make the second decision. It is because of these marginal bits that the contribution of ISI of the bit error is very significant, therefore cancellation of ISI for these bits can significantly reduce bit error probability. Because the SDIC executes ISI cancellation merely for some specific bits rather than for all the bits, the processing speed can be much slower than the system bit rate and it renders SDIC suitable for high-speed lightwave systems.

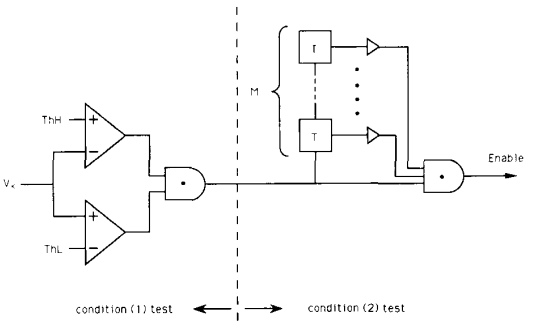

Fig. 3. U-bit decider block diagram.

The heart of the SDIC circuit is the U-bit decider. Its block diagram is shown in Fig. 3. There are two threshold levels: ThH for high threshold level and ThL for low threshold level. ThH is higher than $Th1$, the threshold of COMP1, and ThL is lower than $Th1$. The optimal ThH and ThL can be determined for a particular signal power, ISI, and noise. The optimization will be discussed later. The U-bit decider determines which bit needs further processing based on the following two test conditions:

1) The sampled signal level is between ThL and ThH.
2) Neither of the previous M bits satisfies test condition1).

The first test, which is the key idea of SDIC, is to examine which is a marginal bit. The second test is to prevent from successive ISI cancellations and to provide a much longer time than a bit period for processing and propagation delay through the cancellation and replacement path. By increasing M, one can force the ISI cancellation circuit to operate at a desired slow speed with little performance degradation.

A decision bit with sampled level V_k, if both conditions are true, is marked as U-bit, and the ISI cancellation circuit begins to work. Otherwise, the bit is marked as a D-bit and the SDIC does nothing if any of the two conditions is false.

ThH is the threshold of "1" (high-level signal) and ThL is the threshold of "0" (low-level signal). If V_k is greater than ThH, the kth bit is definitely judged as a "1." We can choose ThH high enough that the probability of V_k being greater than ThH is extremely small when a "0" is sent. Similarly, if V_k is smaller than ThL, the error probability that it represents a "0" is also extremely small. We mark these two kinds of the sampled signal as D-bits without question. For bits for which condition 1) is true but condition 2) is false, the ISI cancellation circuit will also not be enabled in order to provide enough time for the cancellation process and to prevent error propagation. So we mark them as D-bits as well. If there are successive bits located between ThL and ThH, all bits except the first are marked as D-bits so as not to interrupt the ISI cancellation process of the first bit. The reason that condition 2) prevents error propagation is explained below. If a U-bit is detected, none of the previous M bits may be U-bits. That is, we find ISI contribution of the decision bit merely by the estimates of the previous M bits which are all D-bits and unchanged by SDIC. Thus error propagation may occur only when some estimates of the D-bits are wrong. As discussed earlier, however, the error probability of a D-bit is extremely small. Consequently, there is nearly no error propagation with test condition 2). It is not necessary to consider the next N bits here because their ISI contributions are fed forward instead of backward. If the bit in process is a U-bit, and some of its next N bits are also located in the marginal region, the ISI cancellation process starts regardless of the marginal bits. And when the bits come into the U-bit decider, they will be marked as D-bits due to the preceding U-bit.

The U-bit decider classifies bits into D-bits and U-bits. For a D-bit, the decision of COMP1 is kept unchanged. If a sampled signal is classified to be a U-bit, ISI subtracter begins to work. The block diagram of ISI subtracter is shown in Fig. 4. It is made up of an ISI lookup table, a buffer, a holder, and an adder/subtracter. All the linear and nonlinear ISI caused by the $M+N$ neighbor bits can be predetermined and stored in the table. Therefore, total ISI contributions of the previous M and next N bits can be subtracted from the sampled signal V_k. The buffer and the holder are used to holding the first decisions, or estimates the $M+N$ neighbor bits and the sampled signal during the subtraction process, respectively. The delays τ_2, τ_3 are used for accurate subtraction. The delay τ_2 is adjusted for holding the correct sampled signal which waits for ISI subtraction. The delay τ_3 is adjusted for holding the correct neighbors of the U-bit.

Note that not every bit need to be further processed; and if any need, the time between this and the last ISI cancellation is at least of M- bit duration time (usually much more than that). This characteristic is very promising when the receiver is operated at very high speed. Only the COMP1, the shift registers, and the U-bit decider must operate at the speed of the transmission bit rate, the other circuits may operate at a much lower speed.

III. Performance Evaluation

We evaluate the performance of SDIC by both statistical analysis and computer simulation. In this section, the error probability is evaluated by statistical analysis. In the next section, we will carry out computer simulation to verify the analysis. Results of both show that a receiver with SDIC indeed can effectively improve system performance.

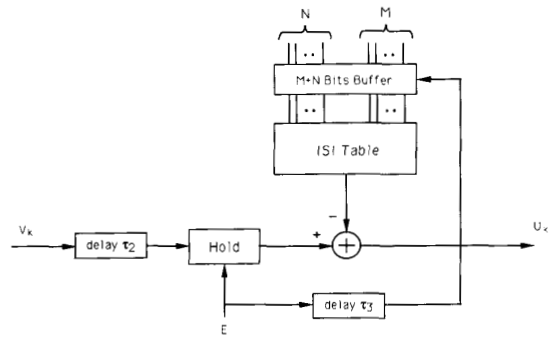

Fig. 4. ISI subtracter block diagram.

A receiver with SDIC is a nonlinear system. To evaluate the error probability, we consider a bit with its previous M and next N bits as a bit block, and find the error probability of the bit for all the combinations of the binary-bit pattern in the block. Because every bit has its block with length $M+N+1$, the average error probability is the estimate of BER.

The filter output can be written as

$$v(t) = \sum_{i=-\infty}^{+\infty} d_i p(t - iT) + n(t) \tag{1}$$

where $n(t)$ is the effective noise, d_i is the binary data for the ith bit, and $p(t)$ is the pulse shape.

By merely considering the ISI induced by previous M and next N bits, the discrete-time sampler at $t = kT$ is

$$V_k = d_k P + \sum_{\substack{i=k-M \\ i \neq k}}^{k+N} d_i I_i + n_k \tag{2}$$

where $P = p(0)$ is the signal level of the decision bit. $I_i = p(kT - iT), i \neq k$, is the ISI level contributed by the ith bit at $t = kT, n_k = n(kT)$ is the sample of $n(t)$ at $t = kT$, M is the number of the previous bits which generate ISI to the decision bit, and N is the number of the next bits which generate ISI to the decision bit. Assume all the bits are equally probably as "1" or "0," then the error probability of the first decision is readily given as

$$P_{e,\text{first}} = \frac{1}{2}[\text{Prob}\,(V_k > Th1 | d_k = 0) + \text{Prob}\,(V_k < Th1 | d_k = 1)]. \tag{3}$$

The error probability with SDIC, denoted as $P_{e,\text{SDIC}}$, depends not only on the sample at $t = kT$ but also on the first decisions of the neighbor $M+N$ bits because of the ISI subtraction.

Define the general neighborhood bit pattern set $\boldsymbol{D_k}$ as

$$\boldsymbol{D_k} \equiv \{d_{k-M}, \cdots, d_{k-1}, d_{k+1}, \cdots, d_{k+N}\} \tag{4}$$

which is a set including 2^{M+N} combinations. The error probability with SDIC can be expressed as

$$P_{e,\mathrm{SDIC}} = \frac{1}{2^{M+N}} \sum_{D \in \boldsymbol{D}_k} \frac{1}{2}[P_{e0D} + P_{e1D}] \tag{5}$$

where D is a specific bit pattern in $\boldsymbol{D}_k$ with $M + N$ bits. P_{e0D} is the error probability with SDIC when $d_k = 0$ and its neighbors are D. P_{e1D} is the error probability with SDIC when $d_k = 1$ and its neighbors are D.

P_{e0D} can be further written as

$$\begin{aligned} P_{e0D} = {} & \mathrm{Prob}\,(V_k > ThH | d_k = 0) \\ & + \mathrm{Prob}\,(V_{k+i} \in (ThL, ThH) \exists i \in \{1, \cdots, M\}, \\ & V_k \in (Th1, ThH) | d_k = 0) \\ & + \mathrm{Prob}\Bigg(V_{k+i} \notin (ThL, ThH) \forall i \in \{1, \cdots, M\}, \\ & V_k \in (Th1, ThH) \\ & V_k - \sum_{\substack{i=k-M \\ i \neq k}}^{k+N} \hat{d}_i I_i > Th2 | d_k = 0 \Bigg) \end{aligned} \tag{6}$$

where $\hat{d}_i$ is the first decision of the ith bit.

There are three terms in the right-hand side of (6). The first term is the probability that as "0" is sent, the sampled signal V_k is already greater than the high threshold level ThH. The second term is the probability that as "0" is sent, some of the previous M samples locate between ThL and ThH and V_k is greater than $Th1$ but smaller than ThH. In this case, though V_k is near the threshold $Th1$, the U-bit decider does not mark it as a U-bit. Therefore the second decision is not made and the final decision is wrong. The third term is the probability that as "0" is sent, the kth bit is marked as a U-bit, but the output of the ISI subtracter is still greater than $Th2$. Although the first decision is replaced, the second decision by COMP2 is still wrong. Note that the effect of ISI due to the previous M and next N bits is included in V_k (by (2)) in all the above three terms.

Similarly, P_{e1D} can be further written as

$$\begin{aligned} P_{e1D} = {} & \mathrm{Prob}\,(V_k < ThL | d_k = 1) \\ & + \mathrm{Prob}\,(V_{k+i} \in (ThL, ThH) \exists i \in \{1, \cdots, M\}, \\ & V_k \in (ThL, Th1) | d_k = 1) \\ & + \mathrm{Prob}\Bigg(V_{k+i} \notin (ThL, ThH) \forall i \in \{1, \cdots, M\}, \\ & V_k \in (ThL, ThH) \\ & V_k - \sum_{\substack{i=k-M \\ i \neq k}}^{k+N} \hat{d}_i I_i < Th2 | d_k = 1 \Bigg) \end{aligned} \tag{7}$$

The other parameter of interest is the occurrence probability of the U-bit. It can be written as

$$P_u = \frac{1}{2^{M+N}} \sum_{D \in \boldsymbol{D}_k} \frac{1}{2}[P_{u0D} + P_{u1D}] \tag{8}$$

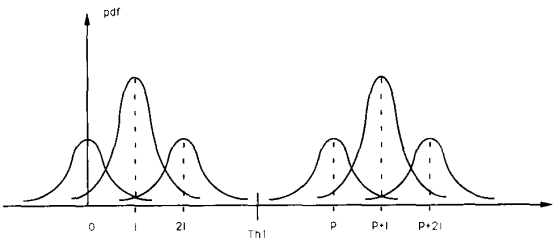

Fig. 5. Probability density function of V_k.

where P_{u0D} and P_{u1D} are the probabilities that the kth bit is classified as a U-bit with neighborhood pattern D and $d_k = 0, 1$ respectively. They can be easily written as

$$\begin{aligned} P_{u0D} = \mathrm{Prob}\Big(& V_{k+i} \notin (ThL, ThH) \forall i \in \{1, \cdots, M\}, \\ & V_k \in (ThL, ThH)\, d_k = 0 \Big) \end{aligned} \tag{9}$$

$$\begin{aligned} P_{u1D} = \mathrm{Prob}\Big(& V_{k+i} \notin (ThL, ThH) \forall i \in \{1, \cdots, M\}, \\ & V_k \in (ThL, ThH)\, d_k = 1 \Big). \end{aligned} \tag{10}$$

In general, the probabilities $P_{e,\mathrm{first}}, P_{e,\mathrm{SDIC}}$, and P_u depend on the bit pattern set D, ISI level, and noise distribution, which are difficult to be analytically expressed. Here for illustrative purpose, we find them for a simplified case. For a decision bit, consider the ISI generated merely by the preceding 1 b and next 1 b with the same contributions. Namely, $M = N = 1, \boldsymbol{D}_k = \{d_{k-1}, d_{k+1}\}$, and

$$I_i = \begin{cases} I, & i = k-1, k+1 \\ 0, & \text{others.} \end{cases} \tag{11}$$

Then V_k is given as

$$V_k = d_k P + d_{k-1} I + d_{k+1} I + n_k. \tag{12}$$

Further assume the effective noise to be Gaussian distributed with variance σ_n^2. The mean of V_k varies for different combinations of d_{k-1}, d_k, and d_{k-1}. The probability density function (pdf) of V_k is shown in Fig. 5.

Clearly, from the pdf of V_k the optimal threshold of COMP1 should be chosen as

$$Th1 = \frac{P + 2I}{2} = \frac{P}{2} + I. \tag{13}$$

Define the Q function as

$$Q(y) = \frac{1}{\sqrt{2\pi}} \int_y^\infty \exp\left(-\frac{x^2}{2}\right) dx. \tag{14}$$

Thus the error probability of the first decision is

$$\begin{aligned} P_{e,\mathrm{first}} = {} & \frac{1}{8} Q\left(\frac{Th1}{\sigma_n}\right) + \frac{1}{4} Q\left(\frac{Th1 - I}{\sigma_n}\right) \\ & + \frac{1}{8} Q\left(\frac{Th1 - 2I}{\sigma_n}\right) + \frac{1}{8} Q\left(\frac{P - Th1}{\sigma_n}\right) \\ & + \frac{1}{4} Q\left(\frac{P + I - Th1}{\sigma_n}\right) + \frac{1}{8} Q\left(\frac{P + 2I - Th1}{\sigma_n}\right). \end{aligned} \tag{15}$$

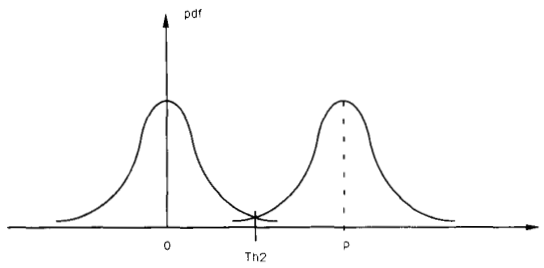

Fig. 6. pdf of U_k if ISI is correctly canceled.

By (13), it can be simplified as

$$P_{e,\text{first}} = \frac{1}{4}Q\left(\frac{Th1}{\sigma_n}\right)+\frac{1}{2}Q\left(\frac{Th1-I}{\sigma_n}\right)+\frac{1}{4}Q\left(\frac{Th1-2I}{\sigma_n}\right). \tag{16}$$

Note that $P_{e,\text{first}}$ is in fact the error probability of an usual receiver with optimum decision threshold.

Now we consider the error probability with SDIC. If all the ISI are correctly canceled, the ISI subtracter output U_k becomes ISI-free with pdf as shown in Fig. 6. Therefore, the optimal threshold of COMP2 is

$$Th2 = \frac{P}{2}. \tag{17}$$

The probabilities P_{e0D} and P_{e1D} are in general pattern-dependent. For example, let d_{k-1}, d_k, d_{k+1} be 1, 0, 1, respectively, i.e., $d_k = 0, D = \{1,1\}$, then $P_{e0\{1,1\}}$ is as given by (18), shown at the bottom of this page, where $\Delta Th = \frac{1}{2}(ThH - ThL)$ is a half of the deviation between the two thresholds, and min (a,b) denotes the smaller one of a, b. The first and second terms of (18) arise from the first and second terms of (6), respectively. And the last four terms are generated by the third term of (6). All the error probabilities for any other combinations of d_{k-1}, d_k, d_{k+1} can be found similarly. The average of all these probabilities is the estimate of BER.

The probability that the kth bit is a U-bit for $d_k = 0, D = \{1,1\}$ is

$$P_{u0\{1,1\}} = \left\{1-\frac{1}{2}\left[\left(\left(\frac{P-ThH}{\sigma_n}\right)-Q\left(\frac{P-ThL}{\sigma_n}\right)\right)+\left(Q\left(\frac{P+I-ThH}{\sigma_n}\right)-Q\left(\frac{P+I-ThL}{\sigma_n}\right)\right)\right]\right\} \times\left[Q\left(\frac{ThL-2I}{\sigma_n}\right)-Q\left(\frac{ThH-2I}{\sigma_n}\right)\right]. \tag{19}$$

In the above equation, the right-hand sides consist of two product terms. The first product term is the probability that the $(k-1)$th bit is not located between ThL and ThH. The second term is the probability that the kth bit is located between ThL and ThH. The probabilities for other combinations of d_{k-1}, d_k, d_{k+1} can be found similarly. The overall U-bit occurrence probability is the average of these probabilities.

In the following discussion, we assume the transmitted pulse be an ideal square pulse stream in NRZ format. The optical fiber is modeled as a linear filter with impulse response

$$h_f(t) = \frac{1}{\sqrt{2\pi}\sigma_F}\exp\left(-\frac{(t-\tau_f)^2}{2\sigma_F^2}\right) \tag{20}$$

where τ_f is the time for light to travel through the fiber, σ_F is the root mean square pulse width of the impulse. For convenience, we use a normalized root mean square pulsewidth σ_f equal to σ_F/T, where T is the bit duration. The response of the amplifier and the filter are jointly modeled as a Butterworth filter with bandwidth BW, and for simplicity, a normalized bandwidth bw equal to $BW * T$ is used instead of

$$\begin{aligned}
P_{e0\{1,1\}} =& Q\left(\frac{ThH-2I}{\sigma_n}\right)+\frac{1}{2}\left\{\left[Q\left(\frac{P-ThH}{\sigma_n}\right)Q\left(\frac{P-ThL}{\sigma_n}\right)\right]+\left[Q\left(\frac{P+I-ThH}{\sigma_n}\right)-Q\left(\frac{P+I-ThL}{\sigma_n}\right)\right]\right\}\\
&\times\left[Q\left(\frac{Th1-2I}{\sigma_n}\right)-Q\left(\frac{ThH-2I}{\sigma_n}\right)\right]+\frac{1}{2}\left\{\left[1-Q\left(\frac{P-ThH}{\sigma_n}\right)\right]+\left[1-Q\left(\frac{P+I-ThH}{\sigma_n}\right)\right]\right\}\\
&\times\frac{1}{2}\left\{\left[1-Q\left(\frac{P-Th1}{\sigma_n}\right)\right]+\left[1-Q\left(\frac{P+I-ThH}{\sigma_n}\right)\right]\right\}\\
&\times\left[Q\left(\frac{Th2+I+\min(\Delta Th,I)-2I}{\sigma_n}\right)-Q\left(\frac{ThH-2I}{\sigma_n}\right)\right]\\
&+\frac{1}{2}\left\{\left[1-Q\left(\frac{P-ThH}{\sigma_n}\right)\right]+\left[1-Q\left(\frac{P+I-ThH}{\sigma_n}\right)\right]\right\}\times\frac{1}{2}\left\{\left[Q\left(\frac{P-Th1}{\sigma_n}\right)\right]+\left[Q\left(\frac{P+I-ThH}{\sigma_n}\right)\right]\right\}\\
&\times\left[Q\left(\frac{Th2+I-2I}{\sigma_n}\right)-Q\left(\frac{ThH-2I}{\sigma_n}\right)\right]+\frac{1}{2}\left\{\left[Q\left(\frac{P-ThH}{\sigma_n}\right)\right]+\left[Q\left(\frac{P+I-ThH}{\sigma_n}\right)\right]\right\}\\
&\times\frac{1}{2}\left\{\left[1-Q\left(\frac{P-Th1}{\sigma_n}\right)\right]+\left[1-Q\left(\frac{P+I-ThH}{\sigma_n}\right)\right]\right\}\times\left[Q\left(\frac{Th2+I-2I}{\sigma_n}\right)-Q\left(\frac{ThH-2I}{\sigma_n}\right)\right]\\
&+\frac{1}{2}\left\{\left[Q\left(\frac{P-ThH}{\sigma_n}\right)\right]+\left[Q\left(\frac{P+I-ThH}{\sigma_n}\right)\right]\right\}\times\frac{1}{2}\left\{\left[Q\left(\frac{P-Th1}{\sigma_n}\right)\right]+\left[Q\left(\frac{P+I-ThH}{\sigma_n}\right)\right]\right\}\\
&\times\left[Q\left(\frac{Th2+I+\min(\Delta Th,I)-2I}{\sigma_n}\right)-Q\left(\frac{ThH-2I}{\sigma_n}\right)\right]
\end{aligned} \tag{18}$$

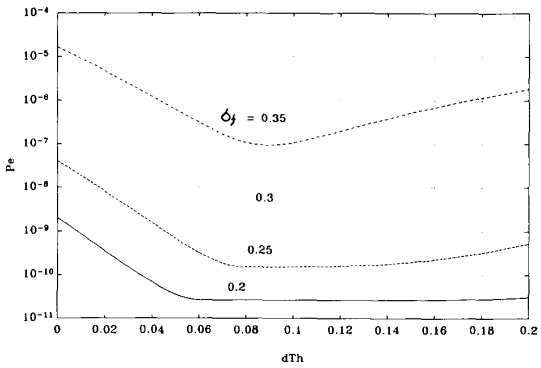

Fig. 7. $P_{e,\mathrm{SDIC}}$ versus dTh with $bw = 0.5$.

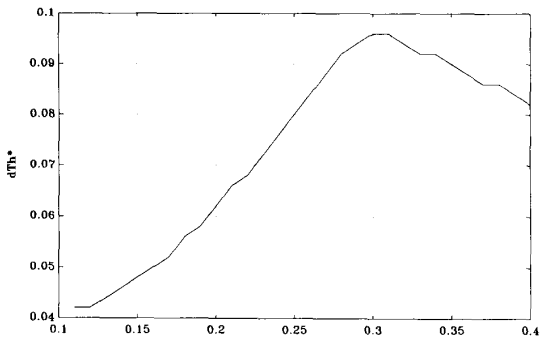

Fig. 8. dTh^* versus σ_f with $bw = 0.5$.

BW. We further define a parameter dTh as

$$dTh = \frac{1}{2}(ThH - ThL)/P \tag{21}$$

which is half the deviation between ThL and ThH normalized by P.

Fig. 7 shows the error probabilities with SDIC as a function of dTh for different σ_f with $bw = 0.5$. When $dTh = 0$, there will be no U-bit detected, and the first decision of every bit is kept unchanged. In this special case, $P_{e,\mathrm{SDIC}}$ is equal to $P_{e,\mathrm{first}}$ and is the error probability of an usual receiver without SDIC. As dTh increases, the ISI cancellation circuit begins to work, $P_{e,\mathrm{SDIC}}$ decreases as expected. There exists an optimal dTh, beyond which $P_{e,\mathrm{SDIC}}$ does not decrease but increases instead. As dTh becomes too large, the probability that a bit locates between ThL and ThH increases, by test condition 2) of the U-bit decider, the number of U-bits may decrease, and the ISI cancellation circuit works less frequently.

There exists an optimal dTh, dTh^*, to reach the minimum error probability. Fig. 8 shows that dTh^* varies with σ_f. For small σ_f, dTh^* increases with σ_f extending the ISI cancellation process. When σ_f becomes large, the probability of wrong ISI cancellation increases, dTh^* therefore decreases.

To demonstrate the excellent performance of a receiver with SDIC, the error probabilities $P_{e,\mathrm{first}}, P_{e,\mathrm{SDIC}}$ versus σ_f are shown in Fig. 9. The upper curve is $P_{e,\mathrm{first}}$, the error probability of an usual receiver. The lower curve shows $P_{e,\mathrm{SDIC}}$, the error probability of the receiver with SDIC. Let σ_f be linearly proportional to the system transmission distance,

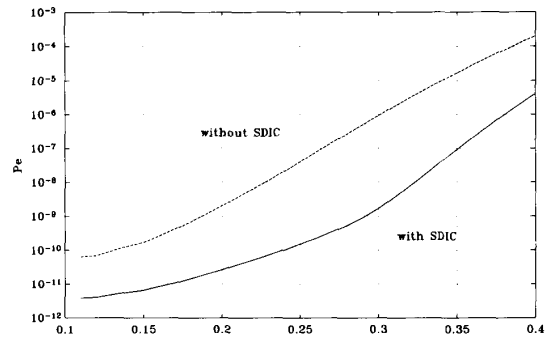

Fig. 9. $P_{e,\mathrm{first}}$ and $P_{e,\mathrm{SDIC}}$ versus σ_f with $bw = 0.5$.

the receiver with SDIC can nearly double the transmission distance at BER = 10^{-10}, and extends half of the transmission distance for BER = 10^{-9}. If longer distance is not needed, the SDIC receiver can substantially reduce error probability. For $\sigma_f = 0.3$, as an example, the receiver with SDIC can reduce error probability by nearly three orders of magnitude (from 10^{-6} to 10^{-9}). Note that as σ_f increases, the difference between $P_{e,\mathrm{first}}$ and $P_{e,\mathrm{SDIC}}$ increases because the receiver with SDIC cancels ISI. Unfortunately, the improvement by SDIC decreases as ISI becomes large due to the incorrect ISI cancellation processes. This is different from that of continuous-time equalizer.

Another major advantage of the SDIC algorithm is that the ISI cancellation circuit can operate at a lower speed than the transmission bit rate when optimal dTh is chosen. Because one U-bit occurrence represents one ISI cancellation process, let us consider the characteristic of U-bit occurrence probability (P_u). Fig. 10 shows P_u versus dTh for different σ_f. It is reasonable to assume that the increase of P_u with the increase of dTh means that the rate of the ISI cancellation process increases as well. If dTh is kept fixed, larger σ_f creates more sampled signals located between ThL and ThH, hence, it results in larger P_u. From Fig. 8, the optimal dTh is usually less than 0.1. It is apparent that P_u is of a lower order than 10^{-3}. Namely, the ISI subtraction circuit can work at a lower rate than the transmission bit rate, which is suitable for high-speed receivers. In the next section, we will show that one can force the subtraction circuit to operate at a desired low speed with little performance degradation. In addition, the ISI cancellation is very efficient. Notice when $\sigma_f = 0.3$, it can decrease error probability by nearly three orders of magnitude by merely doing ISI cancellation 1/1000 of the transmitted bits. This means after ISI cancellation, most error bits can be recovered.

Next let us consider the effect of filter bandwidth. The noise in the receiver is dominated by circuit noise or shot noise and both can be approximated as additive white Gaussian noises [6]. If a large bandwidth is chosen, although the ISI can be minimized, the effective noise increases. On the other hand, small bandwidth will result in significant ISI. Hence there exists a tradeoff between noise and ISI. This is shown in Fig. 11 with $\sigma_f = 0.3$. The upper curve is $P_{e,\mathrm{first}}$ and the lower curves shows $P_{e,\mathrm{SDIC}}$. It is clear that the optimal bandwidth of

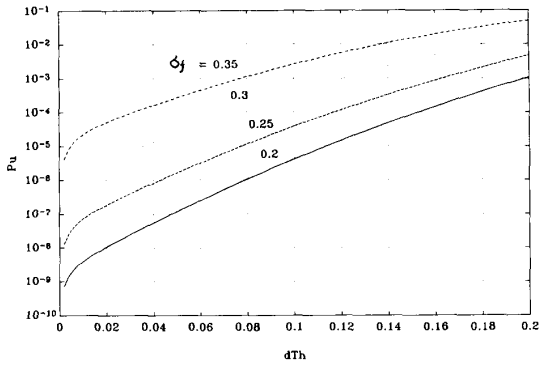

Fig. 10. P_u versus dTh with $bw = 0.5$.

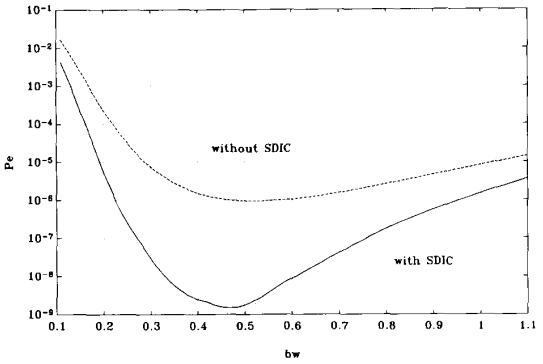

Fig. 11. $P_{e,\text{first}}$ and $P_{e,\text{SDIC}}$ versus bw with $\sigma_f = 0.3$.

$P_{e,\text{first}}$ is 0.52 and 0.48 for $P_{e,\text{SDIC}}$. The optimal bandwidth for $P_{e,\text{SDIC}}$ is slightly smaller than that for $P_{e,\text{first}}$ because the SDIC algorithm enhances ISI cancellation capability, the optimal bandwidth would like to reduce noise while allowing more ISI. Consequently, the resulting bandwidth is smaller. On the left side of the optimal bandwidth, the performance is degraded by ISI; and on the right side, the performance is degraded by noise. Fig. 11 shows that the optimal bandwidths for $P_{e,\text{first}}$ and $P_{e,\text{SDIC}}$ are nearly the same. If an usual receiver is operating at its optimal filter bandwidth for lowest error probability, the SDIC algorithm can significantly reduce the error probability while keeping about the same bandwidth.

IV. Computer Simulation

In the preceding section, we evaluated the performance of the SDIC receiver by statistical analysis. However, real lightwave systems are nonlinear, for example chirping in high-speed modulation of a semiconductor laser may result in nonlinear ISI which is pattern-dependent. Therefore, statistical analysis can only approximately predict system performance. To understand the performance of the SDIC receiver in the presence of light-source nonlinearity and the accuracy of analytical results, in this section we carry out computer simulations taking into account a practical laser model.

In the simulation, each function block in the system is modeled by computer and the overall system is a cascade of each model in sequence. The example we take here is an

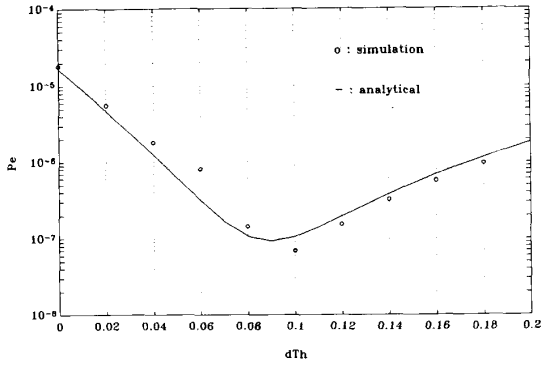

Fig. 12. Analytical and simulation results: $P_{e,\text{SDIC}}$ versus dTh with $bw = 0.5$.

intensity modulation/direct detection system with transmission bit rate of 2.4 Gb/s through a single-mode fiber. A pseudo-random binary data stream is generated by shift registers with length 7. The stream contains all bit patterns with length 7 which is enough for ISI generation. A total of 10^9 b have been transmitted. In the transmitter, the laser driving current pulse is modeled in the NRZ form as

$$I(t) = \begin{cases} I_b, & t < 0 \\ I_b + I_m\left[1 - \exp\left(-\dfrac{t^2}{t_r^2}\right)\right], & 0 < t < T \\ I_b + I_m \exp\left(-\dfrac{(t-T)^2}{t_r^2}\right), & t > T \end{cases} \tag{22}$$

where I_b is the bias current, I_m is the peak modulation current, t_r is the pulse rise time, and T is bit duration equal to 417 ps [8]. Here I_b, I_m, and t_r are taken as 38 mA, 28 mA, 100 ps, respectively. The optical pulse of the semiconductor laser is obtained by solving the rate equation with the same parameter as in [8]. Hence the nonlinear distortion induced by high-speed modulation of the diode laser can be simulated. The optical fiber is modeled as a linear filter with impulse response as in (20). In the receiver, the amplifier and the filter are again modeled as a Butterworth filter with normalized bandwidth bw and the overall noise is Gaussian distributed.

Fig. 12 shows the BER as a function of dTh with $\sigma_f = 0.35$. The solid line is the analytical result and the circles are simulation results. The deviation between the analytical and simulation results comes from the linear channel and equal ISI contributions of neighboring bits assumed in the analysis. Both results indicate that there exists an optimal dTh to get minimum BER. We further see that the analytical result is close to the simulation result, i.e., that the analytical expressions can appropriately evaluate system performance even in the presence of nonlinear distortion. Fig. 13 shows P_u with respect to dTh with $\sigma_f = 0.35$. It is obvious that the analytical formula is very close to the simulation result. Because the number of U-bits is much larger than that of error bits, therefore the analytical expression of P_u comes closer to the simulation result than that of P_e. From the above figures, it can be found that the analytical results provide an accurate estimate of U-bit occurrence and are close to BER

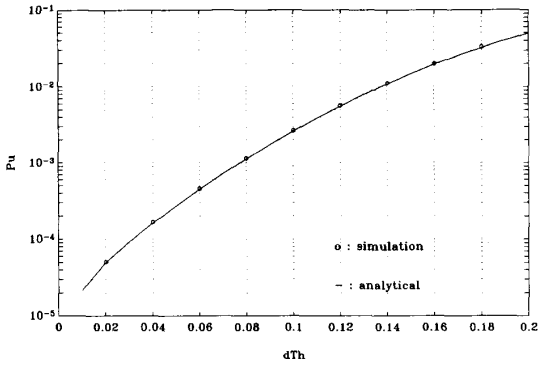

Fig. 13. Analytical and simulation results: P_u versus dTh with $bw = 0.5$.

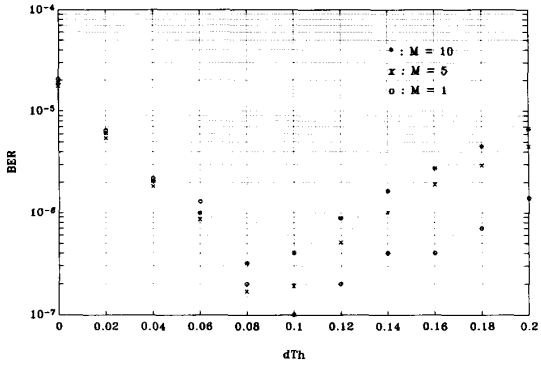

Fig. 14. Simulation results for the effect of different M with $\sigma_f = 0.3$, $bw = 0.5$.

of simulation results. Therefore, the analytical formula can be used to determine the optimal dTh and to estimate the error probability of the receiver with SDIC.

Note that P_u is also the occurrence probability of the ISI cancellation process. For $P_u = 10^{-3}$, on the average we just have to do one ISI cancellation per 10^3 b. However, because the U-bit occurs randomly, the real processing speed should be faster than a 10^{-3}-b rate. By the test condition 2) of the U-bit decider, the cancellation process is actuated at most once per $M + 1$ b. Thus the permissible processing time of the cancellation circuit is extended to $M+1$ b duration. But if two U-bits occur within $M+1$ b then one of them will be ignored and judged as a D-bit without a second decision. Therefore, the BER is expected to increase with M. the simulation results of Fig. 14 show how BER's vary with dTh for different M. At the optimum dTh, the BER for $M = 5$ is slightly larger than that for $M = 1$. And the BER for $M = 10$ is still on the same order as that for $M = 1$. Therefore, we can easily extend the permissible delay of the cancellation circuit with little performance degradation, which renders SDIC a promising scheme to implement ISI cancellation in high-speed lightwave systems.

V. Conclusion

In this paper, we present a receiver with "Soft Decision ISI Cancellation" to deal with ISI problem in high-speed optical systems. The major constraint in treating the ISI problem of high-speed receivers is the limited processing speed. Here the SDIC receiver can easily relax this limitation by doing ISI cancellation merely for some marginal bits but not for all bits, therefore the cancellation circuit can operate at a desired lower speed than the transmission bit rate with little performance degradation. Additional features of the present receiver include: 1) the ISI is treated by discrete-time signal processing instead of continuous-time equalization, 2) both linear and nonlinear ISI can be canceled, and 3) there is nearly no error propagation. Both statistical analyses and computer simulations are carried out to evaluate the system performance. The results show that the SDIC receiver can nearly double the transmission distance at BER = 10^{-10}, and for fixed distance, it can decrease the BER by approximately three orders of magnitude.

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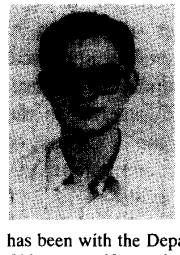

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