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MBE—Enabling technology beyond Si CMOS

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ABSTRACT

Achievement of low interfacial densities of states, small equivalent oxide thickness, high κ values, and thermal stability at high temperatures in the high κ dielectrics on high carrier mobility semiconductors, the leading candidates for technology beyond Si CMOS, has been made using MBE. This paper reviews our recent advances in meeting the unprecedented demands in materials and physics for the new technology. Moreover, self-aligned inversion-channel InGaAs and Ge MOSFETs using MBE-$Ga_2O_3(Gd_2O_3)$ as the gate dielectric are compared favorably with those using the gate dielectrics made from other thin film techniques.

1. Introduction

Molecular beam epitaxy (MBE) has given landmark discoveries in physics and high-performance opto-electronic and electronic devices. On the other hand, silicon-based integrated electronic technology, relying on the excellent properties of SiO_2 and SiO_2/Si (1 0 0) interface with extremely low interfacial densities of states (D_{it}'s) and thermal stability at temperatures $\sim$1000 °C, has not been closely related to MBE. This may be changing, as the scaled SiO_2 thickness approached the quantum tunneling limit, giving rise to unacceptably large electrical leakage. The high-κ plus metal gate, one of the most important recent innovations in complementary metal-oxide-semiconductor (CMOS), has replaced SiO_2 and poly-Si and resolved the gate leakage issue in the 45 and 32 nm MOS field-effect-transistors (MOSFET) production. However, the dimensional scaling in the transistors, which in the past provided simultaneously high-density, low-cost, and high-performance Si ICs, does not give device performance advantages. The role of Si as the channel in the MOS devices is now in question. High κ dielectrics and high carrier mobility channels [1–3] are beginning to play important roles for enhancing the transport performance and reducing power dissipation.

Key issues on fundamental materials and physics for the realization of the above MOS devices are: (1) equivalent oxide thickness (EOT) to be less than 1 nm; (2) interfacial density of states (D_{it}) to be in the order of 10^{11} eV^{-1} cm^{-2} or smaller; (3) self-aligned process, including high temperature thermal stability for activating implanted ions in the source/drain region; (4) low parasitic in ohmic contacts and sheet resistance; and (5) integration with Si.

Note that capacitance effective thickness (CET) is derived directly from the relationship of $CET(V)=(\kappa_{SiO2})*(\varepsilon_0)*(Area)/C(V)$, where κ_{SiO2} is the dielectric constant of SiO_2, ε_0 is the permittivity of free space, and $C(V)$ is the measured capacitance at a biasing voltage V. After quantum-mechanical corrections, the equivalent oxide thickness (EOT) is lower than CET.

MBE with its layer-by-layer growth and its mature development/mass-production in growing III–V compound semiconductors is inherently advantageous to other thin-film technologies on solving the above challenges. Already, the *in-situ* multi-chamber MBE/analysis system [4,5] has made pioneering contributions to the InGaAs MOSFETs [6–12]; MBE-$Ga_2O_3(Gd_2O_3)$ (GGO) [5] and Gd_2O_3 [6] films on (In)GaAs have achieved a low D_{it}, low leakage current densities, and thermal stability at high temperatures, required for fabricating self-aligned inversion-channel InGaAs MOSFET. Indeed, the first inversion-channel GaAs and InGaAs MOSFETs [7–9], and a CMOS [13] were demonstrated with GGO as a gate dielectric. Also, depletion-mode (In)GaAs MOSFET's [14,15], and a power device [16] were shown to exhibit negligible drain current drift and hysteresis.

With the ability in atomically tailoring the high κ's/semiconductor interfaces [17] and in epitaxy-stabilizing non-equilibrium phases with enhanced high κ values [18,19], the *in-situ* MBE will continue to play a very critical role in addressing/solving the challenges of EOT, D_{it}, and thermal stability at high temperatures. The multi-chamber system combines InGaAs, oxide, and metal

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MBE chambers, and other analysis chambers, such as X-ray photoelectron spectroscopy (XPS), and ultra high vacuum (UHV) transfer modules connecting these chambers (Fig. 1(a) and (b)). An ALD reactor was connected *in-situ* into our system to eliminate the surface contaminations of InGaAs prior to ALD oxides [20].

In the following, our recent accomplishments using MBE for solving the urgent material, physics, and device challenges facing the post Si CMOS are reviewed. Intensive efforts on the area of (4) low parasitic in ohmic contacts and sheet resistance; and (5) integration with Si, however, would not be reviewed here, due to the page limit.

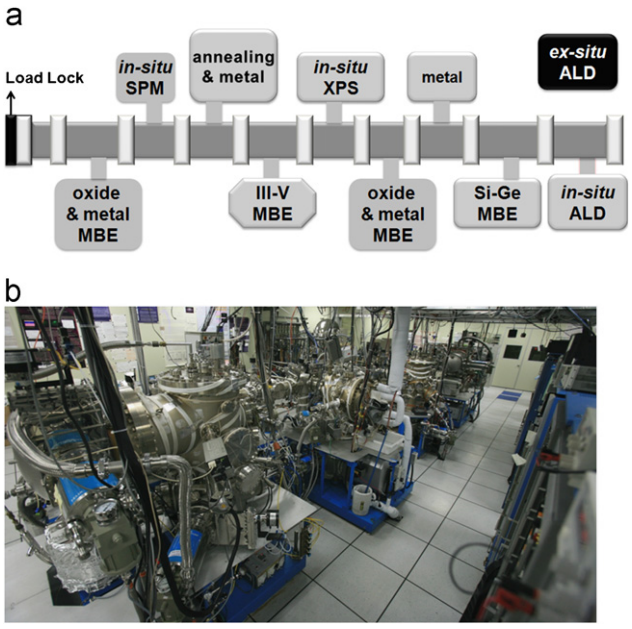

Fig. 1. Schematic (a) and photography (b) of the multi-chamber MBE/analysis/ALD system.

2. Interfacial tailoring

The growth of MBE is different from that using ALD, particularly in the very initial stage of depositing the high κ dielectrics on semiconductors. For ALD-Al_2O_3 and -HfO_2 on Si, the formation of an interfacial layer (SiO_2) is inevitable due to its inherent growth mechanism [21]. The existence of such interfacial layer reduced the dielectric constant of the overall gate stack, and hampered further reductions of CET/EOT. MBE-Al_2O_3 and -HfO_2 on Si, on the other hand, have given atomically abrupt interfaces without the interfacial layer [22]. An innovative MBE+ALD-HfO_2 on Si has given an EOT of 0.7 nm with a leakage current density of 5.3×10^{-1} A/cm^2 at $V_{FB}-1V$, a D_{it} value of 3.6×10^{11} cm^{-2} eV^{-1}, and a MOSFET with good device performance [23,24].

For the high κ's on InGaAs, with its interfacial self-cleaning of arsenic oxides and removing most of the other native oxides, ALD has now received a lot of attention [25]. Residual In_2O_3 and Ga_2O_3, and their hydro-oxides at the ALD-oxide/InGaAs interface were further reduced with air exposure <10 min from the MBE system to an *ex-situ* ALD reactor, resulting in a CET of 1.0 nm with HfO_2 [26] and a D_{it} in the range of 10^{11} eV^{-1} cm^{-2} with Al_2O_3 [27]. In contrast, there are no such native oxides at the interfaces using MBE-GGO [28].

2.1. Oxides/InGaAs

2.1.1. MBE-GGO/InGaAs

The unique initial MBE-growth of GGO on InGaAs [29] has given MBE-Al_2O_3-GGO/$In_{0.2}Ga_{0.8}As$/GaAs excellent thermal stability

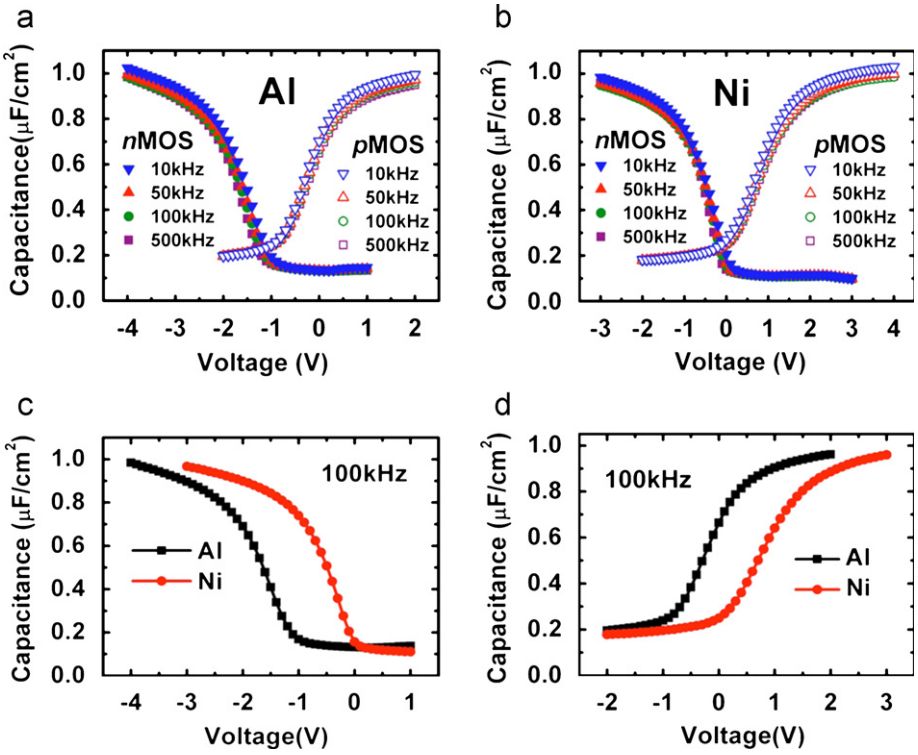

Fig. 2. *C–V* characteristics from 10 to 500 kHz of MBE-Al_2O_3/Ga_2O_3(Gd_2O_3) on both n-$In_{0.2}Ga_{0.8}As$ and p-$In_{0.2}Ga_{0.8}As$ with (a) Al and (b) Ni metal gate. *C–V* characteristics of MBE-Al_2O_3/Ga_2O_3(Gd_2O_3) on (c) p-$In_{0.2}Ga_{0.8}As$ and (d) n-$In_{0.2}Ga_{0.8}As$ with Al and Ni gates at frequencies of 100 kHz. The samples were RTA at 850 °C for 10 s in He ambience prior to the gate metal deposition.

(> 850 °C) [10], negligible interface/bulk traps, and a CET of 0.6 nm in GGO, with its κ value remaining ~14–16 for all the measured GGO film thicknesses [30]. Very importantly, the $In_{0.20}Ga_{0.80}As$/GaAs interface remains free of misfit dislocation observed by high-resolution transmission electron microscopy (HR-TEM) and the strained $In_{0.20}Ga_{0.80}As$ does not relax as revealed by thorough X-ray diffraction studies [31]. Both n- and p-MOSCAPs (MOS capacitors) using metal gates of various work functions [12] have exhibited low electrical leakage current densities, and excellent capacitance–voltage (C–V) characteristics with low D_{it} (in the range of 10^{11} eV^{-1} cm^{-2}) and small frequency dispersion (Fig. 2(a)–(d)). A well tuning of threshold voltage V_{th} with metal work function was demonstrated, crucial for high performance InGaAs MOSFET.

2.1.2. MBE-HfO_2/InGaAs

Monoclinic crystalline MBE-HfO_2 oxide films 4–6 nm thick epitaxially on GaAs [32,33] formed four equivalent in-plane domains rotating 90° about the surface normal, resulting in large electrical current leakages. A new dielectric stack of amorphous HfAlO (4 nm thick)+crystalline HfO_2 (3 mono-layer thick, as monitored by reflection high-energy electron diffraction (RHEED)) (Fig. 3(a) and (b)) epitaxially on $In_{0.2}Ga_{0.8}As$ has given C–V's (Fig. 3(c)) with small capacitance dispersion between 10 and 500 kHz. The CET value of the dielectrics is 1.18 nm, with an EOT of < 1 nm [34]. Moreover, the attainment of a low leakage current density (2.9×10^{-4} A/cm^2) at $|V_G - V_{FB}| = 1$, thermal stability up to 800 °C, and a low D_{it} has made this new MBE high κ stack a very promising gate dielectric for fabricating self-aligned inversion-channel InGaAs MOSFETs.

2.1.3. MBE-$LaAlO_3$/(In)GaAs

MBE-$LaAlO_3$ has been deposited on Si [35] and InGaAs [36] without employing an interfacial layer (IL). Electrical properties with C–V characteristics, having a hysteresis of 15 mV – 0.1 V, a κ value of 17 ± 1, and band offsets > 1 eV, and electrical current density versus field curves, showing a dielectric strength of ~4.3 MV/cm, have been obtained on (In)GaAs [36–37].

2.1.4. MBE-Al_2O_3/GaAs [38]

In another MBE approach, Al_2O_3 films were deposited on freshly grown GaAs with various As-coverage surfaces by evaporating aluminum from an effusion cell under an atomic oxygen flux using a plasma source. (Note that most of our MBE-oxide deposition has

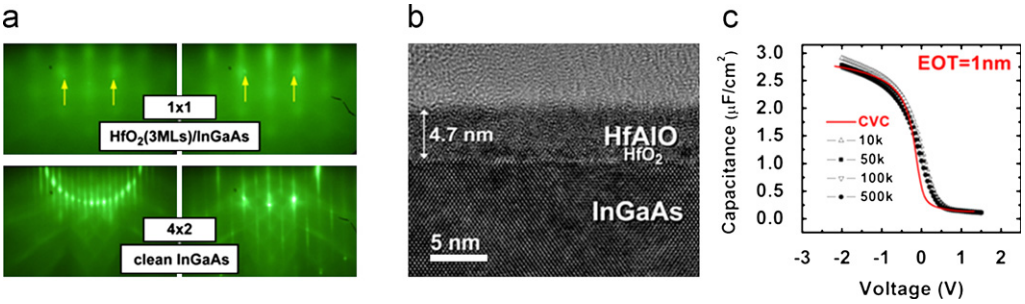

Fig. 3. (a) RHEED patterns for freshly prepared InGaAs surface (4 × 2) and 3MLs HfO_2 epitaxially grown on InGaAs (1 × 1) (the RHEED signal from the InGaAs epilayer was still observed as indicated by the arrows), (b) cross-sectional HR-TEM image of HfAlO/HfO_2(3MLs)/$In_{0.2}Ga_{0.8}As$/p-GaAs after RTA to 800 °C for 20 s in He ambience, and (c) C–V characteristics of the sample described in (b) using Ni as a gate metal with frequency varying from 10 to 500 kHz. The CVC modeling was performed in red line to fit the experimental data [73].

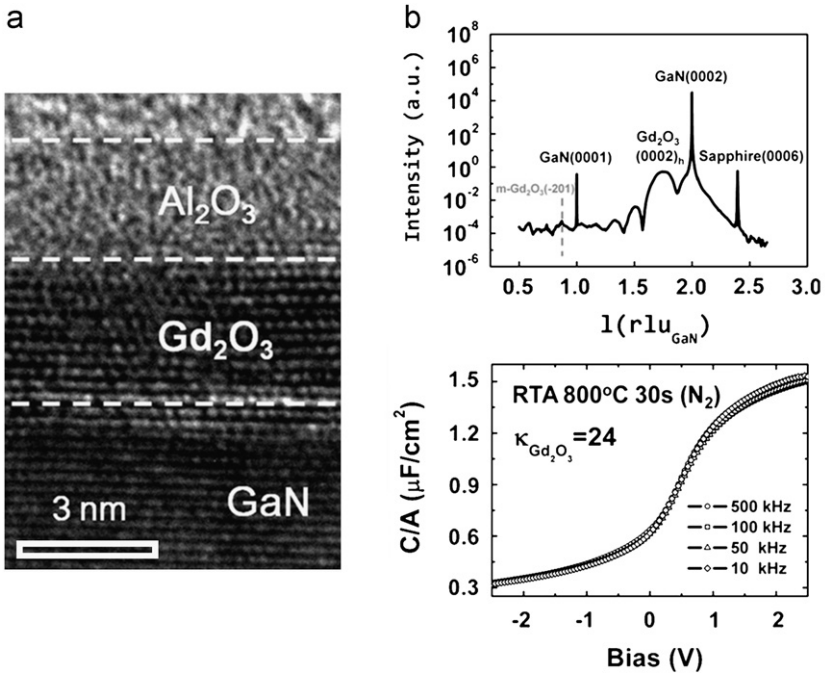

Fig. 4. (a) Cross-sectional HR-TEM image of Al_2O_3(3 nm)/Gd_2O_3(3.2 nm)/GaN after 800 °C annealing. (b) Intensity profile of a radial scan along the surface normal. All Bragg peaks are indexed. (c) C–V characteristics of the sample described in (a) using Au as a gate metal with frequency from 10 to 500 kHz after RTA to 800 °C for 30 s in N_2 ambience.

been carried out with e-beam evaporation from oxide targets.) The samples were post-annealed to optimize the oxide and interface quality under nitrogen ambience at various temperatures and dwelling durations. The corresponding D_{it}'s were derived using the conductance method at 25 and 150 °C on both p- and n-type GaAs MOSCAPs; a significant reduction of D_{it} around the critical mid-gap region is achieved by applying an optimized thermal annealing on samples grown on a Ga-rich (4×6) reconstructed surface.

2.2. Oxides/Ge

As Ge native oxides are unstable and volatile, interfacial passivation layers (IPLs), such as GeON [39], GeO_2 [40], Si [41], La_2O_3 [42,43], germanide (SrGe) [44], etc. between high κ dielectrics and Ge have been utilized for enabling the Ge MOS technology. Note that only the high κ's of HfO_2 on La_2O_3 [42], ZrO_2 on La_2O_3 [43], and $LaAlO_3$ on germanide [44] were deposited using MBE. However, degradation of the IPL/Ge interface and diffusion of Ge into the high κ's occur as the IPL becomes thinner, thus preventing further EOT scaling [45].

2.2.1. MBE-GGO on Ge

Direct deposition of GGO on Ge without IPLs has achieved low D_{it}'s, an EOT of 0.6 nm in GGO, low electrical leakage currents, and thermodynamic stability at 500 °C annealing [46–49]. CF_4 plasma on GGO/Ge and N_2 annealing have further reduced D_{it}'s to $7.7\times10^{11}\,cm^{-2}\,eV^{-1}$, extracted using a conductance method [48], with a mean D_{it} value of $\sim3\times10^{11}\,cm^{-2}\,eV^{-1}$, obtained using a charge pumping technique [47]. The frequency dispersions of less than 3.5% and 0.1 V have been achieved in accumulation and depletion regions, respectively. In contrast, direct ALD-oxides on Ge without IPLs have failed to give meaningful *C–V* characteristics.

Table 1
Summary of representative E-mode NMOSFETs reported since 1998.

No.	Year published [Ref]	Research group	Type/channel mat'l	Gate dielectric/deposition method/ (passivation)	Device characteristics
(1)	1998 [8]	Bell Labs Ren et al.	Inversion channel/ $In_{0.53}Ga_{0.47}As$	UHV E-beam evaporated GGO	$I_{D,max}$=375 μA/μm (1 μm) G_m=190 μS/μm (0.75 μm)
(2)	1999 [9]	Bell Labs Wang et al.	Inversion channel/GaAs	UHV E-beam evaporated GGO	L_G=1 μm $I_{D,max}$=30 μA/μm G_m=4 μS/μm
(3)	2007 [57]	Purdue Univ. Xuan et al.	Inversion channel/ $In_{0.53}Ga_{0.47}As$	ALD Al_2O_3	$I_{D,max}$=430 μA/μm L_G=0.5 μm G_m=160 μS/μm
(4)	2007 [58]	Freescale/U.Glasgow Hill, et al	implant-free/$In_{0.3}Ga_{0.7}As$	UHV E-beam evaporated Ga_2O_3/GaGdO	L_G=1 μm $I_{D,max}$=407 μA/μm G_m=477 μS/μm
(5)	2007 [59]	IBM Sun et al.	Buried channel/$In_{0.7}Ga_{0.3}As$	ALD Al_2O_3	L_G=0.26 μm $I_{D,max}$=117 μA/μm G_m=157 μS/μm
(6)	2008 [60]	Purdue Univ. Xuan et al.	Inversion channel/ $In_{0.65}Ga_{0.35}As$	ALD Al_2O_3	L_G=0.4 μm $I_{D,max}$=1050 μA/μm G_m=350 μS/μm
(7)	2008 [11]	Natl Tsin-Hua Univ. Lin et al.	Inversion channel/ $In_{0.53}Ga_{0.47}As$	UHV E-beam evaporated Al_2O_3/GGO	L_G=1 μm $I_{D,max}$=1050 μA/μm G_m=714 μS/μm
(8)	2008 [61]	Purdue Univ. Xuan et al.	Inversion channel/ $In_{0.75}Ga_{0.25}As$	ALD Al_2O_3	L_G=0.75 μm $I_{D,max}$=1000 μA/μm G_m=430 μS/μm
(9)	2008 [62]	IBM Sun et al.	Buried channel/$In_{0.7}Ga_{0.3}As$	ALD Al_2O_3*a*-Si	L_G=0.09 μm (90 nm) $I_{D,max}$=390 μA/μm G_m=610 μS/μm
(10)	2009 [63]	Natl Tsin-Hua Univ. Chiu et al.	Inversion channel/ $In_{0.53}Ga_{0.47}As$	ALD Al_2O_3	L_G=0.6 μm $I_{D,max}$=678 μA/μm G_m=354 μS/μm
(11)	2009 [64]	Purdue Univ.Wu et al.	Inversion channel/ $In_{0.75}Ga_{0.25}As$	ALD Al_2O_3	L_G=0.13 μm $I_{D,max}$=440 μA/μm G_m=705 μS/μm
(12)	2009 [65]	Univ. Singapore Chin et al.	Inversion channel/ $In_{0.53}Ga_{0.47}As$	MOCVD HfAlO SiH_4 and NH_3	L_G=0.25 μm $I_{D,max}$~420 μA/μm G_m=45.3 μS/μm ∗with S/D stressors
(13)	2010 [66]	Natl Tsin-Hua Univ. Lin et al.	Inversion channel/ $In_{0.75}Ga_{0.25}As$	ALD Al_2O_3	L_G=1 μm $I_{D,max}$=740 μA/μm G_m=325 μS/μm
(14)	2010 [67]	Natl Tsin-Hua Univ. Lin et al.	Inversion channel/ $In_{0.75}Ga_{0.25}As$	UHV E-beam evaporated Al_2O_3/GGO	L_G=1 μm $I_{D,max}$=1234 μA/μm G_m=464 μS/μm
(15)	2009 [2]	Intel Corp. Radosavljevic et al.	Quantum-well/$In_{0.7}Ga_{0.3}As$	$TaSiO_x$/InP (ALD-$TaSiO_x$)	L_G=0.075 μm(75 nm) $I_{D,max}$=490 μA/μm G_m=1750 μS/μm

3. Crystalline oxides on semiconductors

Growth of high-quality single crystalline oxides (Gd_2O_3, Y_2O_3, La_2O_3, Sc_2O_3, Al_2O_3, HfO_2, etc.) on semiconductors (Si, (In)GaAs, Ge, and GaN) is always scientifically interesting and has made contribution to nano-electronics [6,50,51]. Single crystal semiconductors were grown on these hetero-structures forming semiconductor/oxide/semiconductor; a couple examples are given here: Si/Gd_2O_3/Si, GaN/Sc_2O_3/Si, and GaN/Gd_2O_3/GaN [52–54].

Moreover, enhanced κ values were obtained in MBE grown single crystal cubic HfO_2 doped with Y_2O_3 (denoted as YDH) with a κ over 30 [18]. The monoclinic phase is commonly observed and the most stable phase below 1750 °C, while the cubic phase exists at ~2600 °C. The attainment of the cubic YDH has eliminated the four azimuthal domains [32,33], thus significantly reducing electrical leakage.

MBE deposited nm-thick hexagonal single crystal Gd_2O_3 epitaxially on GaN [19] (Fig. 4(a) and (b)), a high-temperature phase at > 2473 °C, stabilized with epitaxy at a lower deposition temperature, has a dielectric constant of ~24 (Fig. 4(c)), about twice of the usual value of its cubic counterpart when deposited on (In)GaAs or Si, resulting in a low measured CET of 0.5 nm. The hetero-structure is thermally stable at high temperatures and has low D_{it}'s after high temperature annealing.

Another example is epitaxy-stabilized monoclinic nm-thick Y_2O_3 films grown on GaN (0 0 0 1) using MBE [55], in which excellent electrical properties were obtained. At atmospheric pressure, Y_2O_3 exists in either cubic or hexagonal structure.

4. D_{it} distribution within the bandgap of InGaAs [56]

Systematic temperature-dependent C–V and conductance measurements were used to study the electrical characteristics of MBE and ALD oxides on $In_{0.2}Ga_{0.8}As$. The distribution of D_{it} within the band gap of $In_{0.2}Ga_{0.8}As$ using MBE-GGO, deduced with the conductance method, has given D_{it} values of $\sim 5\times10^{11}$ eV^{-1} cm^{-2} above, $\sim 2\times10^{12}$ eV^{-1} cm^{-2} below, and $\sim 5\times10^{12}$ eV^{-1} cm^{-2} around the mid-gap region (0.5–0.7 eV above valence energy (E_v)); the high D_{it} value near the mid-gap, extracted at 100 and 150 °C, may be related to the temperature effect, which tends to induce more interfacial traps. In contrast, the ALD-Al_2O_3/$In_{0.2}Ga_{0.8}As$ has yielded higher D_{it} values of $>10^{13}$ eV^{-1} cm^{-2} around the mid-gap region.

5. High κ's/InGaAs and κ/Ge MOSFET

5.1. Inversion-channel MBE-GGO/InGaAs MOSFET and other enhancement-mode InGaAs MOSFETs

The state-of-the-art enhancement-mode InGaAs MOSFETs [2,8,9,11,57–67] are collected in Table 1 and compared in Fig. 5(a) and (b), in terms of drain currents and transconductance. The device configurations include inversion-channel (self-aligned and non-self-aligned), buried channel, and implant-free designs. In addition, a short-channel quantum-well InGaAs MOSFET on a Si substrate was included in Table 1; this indicates the trend of integrating the InGaAs MOSFETs onto Si ICs [2].

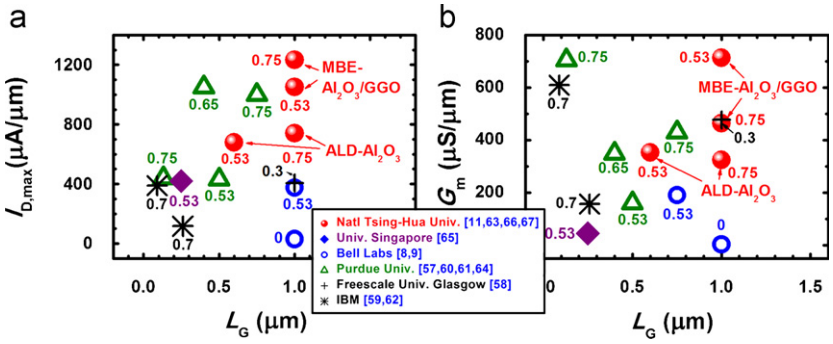

Fig. 5. Benchmark of (a) maximum drain currents $I_{D,max}$ and (b) peak transconductances G_m of state-of-the-art enhancement-mode $In_xGa_{1-x}As$ MOSFETs (x=0, 0.3, 0.53, 0.65, 0.7, and 0.75). Devices with gate-length larger than 1 μm are not included. The self-aligned inversion channel devices are denoted with solid circular symbol, and the data of the non-self-aligned counterparts are denoted with hollow circular symbol.

Table 2
Summary of representative Ge PMOSFETs reported since 2006.

No.	Year published [Ref]	Research group	Type/channel mat'l	Gate dielectric/deposition method/(passivation)	Device characteristics
(1)	2010 [49]	Natl Tsin-Hua Univ. Chu et al.	Inversion channel/Ge	UHV E-beam evaporated Al_2O_3/GGO	L_G=1 μm $I_{D,max}$=800 μA/μm
(2)	2007 [68]	IMEC Nicholas et al.	Inversion channel/Ge	ALD-HfO_2/CVD-Si(SiO_2)	L_G=0.125 μm $I_{D,max}$=1360 μA/μm
(3)	2010 [69]	IMEC Bellenger et al.	Inversion channel/Ge	MBD-AL_2O_3/RO-GeO_2	L_G=1 μm $I_{D,max}$=180 μA/μm
(4)	2009 [70]	Natl Tsin-Hua Univ. Chu et al.	Inversion channel/Ge	UHV E-beam evaporated Al_2O_3/Y_2O_3	L_G=4 μm $I_{D,max}$=98 μA/μm
(5)	2006 [71]	MIT/Intel/NCSRD Ritenour et al.	Inversion channel/Ge	MBD-HfO_2/MBD-GeON	L_G=10 μm $I_{D,max}$=24 μA/μm
(6)	2009 [72]	Univ. Singapore Xie et al.	Inversion channel/Ge	ALD-HfO_2/Thermal GeO_2	L_G=10 μm $I_{D,max}$=37.8 μA/μm
(7)	2008 [41]	Univ. Tokyo Nakakita et al.	Inversion channel/Ge	Al_2O_3 or SiO/Thermal GeO_2	L_G=200 μm $I_{D,max}$=0.38 μA/μm

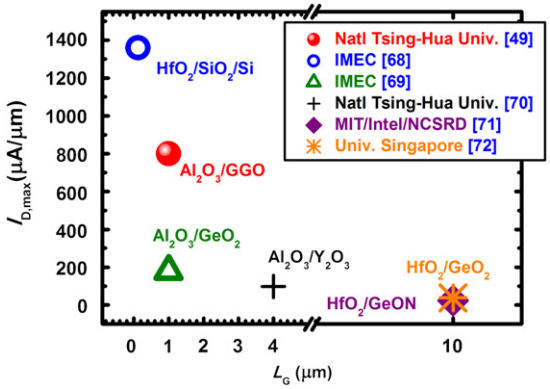

Fig. 6. Benchmark of maximum drain currents $I_{D,max}$ of representative Ge p-MOSFETs.

In general, InGaAs MOSFETs with inversion channels outperform those in other configurations (non-inversion-channel). Furthermore, among the inversion-channel InGaAs MOSFETs, self-aligned processed devices have shown better performance than those of the non-self-aligned counterparts, given the same gate dielectrics, e.g. ALD-Al_2O_3. The self-aligned inversion-channel MBE-Al_2O_3/GGO/InGaAs MOSFETs, with 1 μm-gate-length, have achieved drain currents of >1.2 mA/μm, transconductances of >710 μS/μm, and peak mobility of 1600 cm^2/V s at 1 μm gate length.

5.2. MBE-GGO/Ge MOSFET and comparison with Ge MOSFETs with other gate dielectrics

The representative Ge p-MOSFETs are summarized in Table 2 and compared in Fig. 6, in terms of drain currents. The comparison is emphasized on choices of IPLs.

Our approach is directly depositing GGO on Ge without using any IPL, while IPL is necessary in most other devices for achieving good performance. Nevertheless, GGO on Ge has given excellent electrical performances and thermodynamic stability. Moreover, self-aligned GGO/Ge p-MOSFETs have shown a high drain current of 800 μA/μm and peak transconductance of 420 μS/μm, at 1 μm gate length, the highest among those demonstrated in Ge MOSFETs with similar gate lengths. In comparison, Ge MOSFETs using ALD-HfO_2 with a CVD-Si IPL have exhibited high drain current of 1.36 mA/μm, but with a smaller gate length of 125 nm [68].

6. Conclusion

Low CET/EOT values of <1 nm, D_{it} values of $\sim 10^{11}$ eV^{-1} cm^{-2}, and thermal stability at high temperatures for high κ's on InGaAs, Ge, and GaN, all very challenging tasks, have been achieved using MBE. For the post Si CMOS push, MBE is an enabling technology. Device design/fabrication and growth development/production need to be intensified. Looking ahead beyond Si CMOS, efforts are focused on "hybrid" chips of integrating high κ's/high carrier mobility semiconductor channel MOSFETs onto Si substrates.

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