A New $I-V$ Model Considering the Impact-Ionization Effect Initiated by the DIGBL Current for the Intrinsic n-Channel Poly-Si TFT's

Hsin-Li Chen, *Student Member, IEEE* and Ching-Yuan Wu, *Member, IEEE*

***Abstract*—Considering the impact-ionization mechanism occurring in the high drain-bias $(V_{\rm DS})$ regime, a new $I-V$ model considering the impact-ionization effect initiated by the drain-induced-grain-barrier-lowering (DIGBL) current has been established for the intrinsic n-channel poly-Si TFT. The simulation results with considering the developed impact-ionization current model are in excellent agreement with the experimental output characteristics of the intrinsic n-channel poly-Si TFT with the mask-gate length ranging from 5 μm to 40 μm. In resolving the physical parameters and their underlying operation mechanisms including the grain-barrier height, DIGBL current, and impact-ionization current, the developed $I-V$ model will be beneficial to further understand the underlying physics of the intrinsic poly-Si TFT.**

***Index Terms*—DIGBL, impact-ionization, I–V model, poly-Si TFT.**

I. Introduction

RECENTLY, the intrinsic poly-Si thin-film transistors (poly-Si TFT's) by low-temperature process have received wide investigation for their important applications in the active-matrix liquid crystal display (AMLCD) [1], [2] and the static random-access-memories (SRAM's) [3]. To optimize the design of the poly-Si TFT's with high-performance, they should have a reliable analyzer based on the physical mechanisms to correlate the dependence of the electrical characteristics on the fabrication conditions.

The kink effect for the drain-source current $(I_{\rm DS})$ of the poly-Si TFT operating in the high drain-bias regime has been investigated by several works [4]–[8]. With the aid of two-dimensional (2-D) numerical simulation, the nature of the kink effect had been identified to be due to the impact-ionization mechanism in the high-field regime near the drain for the intrinsic poly-Si TFT [4]–[7]. On the other hand, when the drain voltage is applied, the grain-barrier heights for both sides of the grain boundary become asymmetric and the grain-barrier height for the side near the source junction will be lower than the side near the drain junction. As a consequence, there will be extra carriers injecting from the source junction through the side with lower grain barrier into the channel, resulting in the increased current. This phenomenon is so called the drain-induced-grain-barrier-lowering (DIGBL) effect [8]. Based upon the interfacial-layer thermionic-diffusion model [9], and considering the DIGBL effect, Lin *et al.* [8] had analytically simulated the kink output characteristics of the doped poly-Si TFT's. However, for the intrinsic poly-Si TFT, the doping concentration in the grain must be set to zero. The derivations by assuming the quadratic potential distribution for the grain with finite depletion depth to solve the 2-D Poisson's equation [8] will be invalid due to the zero doping concentration and the grain-barrier height model will break down. Therefore, the grain-barrier height model and the $I-V$ model developed in [8] cannot be used to simulate the grain-barrier height and the $I-V$ characteristics of the intrinsic poly-Si TFT. To solve this problem, the existence of the trap states in the grain is assumed and the grain-barrier height model for the intrinsic poly-Si TFT can then be established [10]. Moreover, the potential distribution across the depletion region in the grain, which is important to calculate the diffusion velocity of carriers in the $I-V$ model based on the interfacial-layer thermionic-diffusion theory, can be easily obtained. However, with the $I-V$ model considering only the DIGBL effect using the grain-barrier height model for the intrinsic poly-Si TFT, there is still a large deviation in the kink regime of the output curves between the results of simulation and measurement for the intrinsic poly-Si TFT. This implies that, in addition to the DIGBL effect, the impact-ionization should be considered for simulating the kink output characteristics of the intrinsic poly-Si TFT.

In this paper, we will propose an analytical $I-V$ model to simulate the impact-ionization mechanism initiated by the DIGBL current for the intrinsic n-channel poly-Si TFT's. It will be shown later that the physical meaning for the kink output characteristics is clearly represented in our model and good agreement is obtained between the simulated and experimental results.

II. The Impact-Ionization Current Model

Based on the interfacial-layer thermionic-diffusion theory [9], the $I-V$ model considering the DIGBL effect can be written as

$$I_{\rm DIGBL} = \frac{W}{L}\int_0^{V_{\rm DS}} \frac{\mu_n^i}{F_i} Q_n(V_i)\, dV_i \qquad (1)$$

Manuscript received May 25, 1998; revised September 14, 1998. This work was supported by the National Science Council, Taiwan, R.O..C, under Contract NSC87-2215-E009-050. The review of this paper was arranged by Editor M. Fukuma.

The authors are with Advanced Semiconductor Device Research Laboratory and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

Publisher Item Identifier S 0018-9383(99)02389-8.

0018–9383/99$10.00 © 1999 IEEE

where $I_{\rm DIGBL}$ is the current of the DIGBL effect; $W(L)$ is the channel width (length); μ_n^i is the effective mobility and is given as

$$\mu_n^i = \frac{\mu_0}{1+\theta(V_{\rm GS}-V_T-V_i)+\frac{\mu_0}{\nu_{\rm s1}}E_L^i+\xi} \tag{2}$$

with $E_L^i = \eta\frac{V_{\rm DS}}{L}$ and $\xi = 2\theta(\frac{qn_it_{\rm Si}}{C_{\rm OX}})$; Q_n is the density of carriers (free electrons for n-channel device) per area; and

$$F_i = \frac{\nu_{Dn}^i+\theta_n\nu_{\rm Rn}}{\nu_{Dn}^i\theta_n\nu_{\rm Rn}}\frac{\mu_n^i}{\beta L_g}\exp\bigl(\beta\phi_{\rm GB-}^i\bigr)+\bigl(1-W_T^i/L_g\bigr) \tag{3}$$

where

- ν_{Dn}^i diffusion velocity of electrons across the depletion region;
- $\theta_n\nu_{Rn}$ effective thermal velocity of electrons across the grain boundary along the channel direction;
- β inverse thermal voltage $(=q/kT)$;
- L_g grain size;
- W_T^i depletion width in the i-th grain;
- $\phi_{\rm GB-}^i$ grain-barrier height considering the DIGBL effect.

The grain-barrier height model, considering the DIGBL effect for the intrinsic poly-Si TFT, can be expressed as [10]

$$\phi_{\rm GB-}^i = \frac{t_{\rm Si}}{C_{\rm OX}(V_{\rm GS}-V_{T0}-V_i)}\frac{\bigl(qN_{\rm ST}-\epsilon_{\rm Si}E_L^i\bigr)^2}{8\epsilon_{\rm Si}} \tag{4}$$

where

- $t_{\rm Si}$ thickness of the active poly-Si film;
- $C_{\rm OX}$ capacitance of the gate oxide per area;
- $N_{\rm ST}$ density of the grain boundary states;
- V_{T0} intrinsic threshold voltage.

From the derivation of the grain-barrier height model for the intrinsic poly-Si TFT [10], it is shown that the potential variation $\phi(x)$ accounting for the formation of the grain-barrier is governed by the reduced Poisson equation

$$\frac{d^2}{dx^2}\phi(x)-K^2\phi(x) = -K^2V_{\rm QN}. \tag{5}$$

Within the turn-on regime $V_{\rm QN}\gg\phi(x)$ and the space-charge term $K^2V_{\rm QN}$, is equal to $C_{\rm OX}(V_{\rm GS}-V_{T0})/t_{\rm Si}$, which is just the average concentration of the induced free-carriers $(\bar{n})$ with positive sign; that is, the space-charge in the depletion region is composed of the induced free-carriers for the intrinsic poly-Si TFT. The depletion approximation for the diffusion velocity should then be expressed as

$$\nu_{Dn}^i \cong \mu_n^i\left(\frac{2q\bar{n}}{\epsilon_{\rm Si}}\right)^{\frac{1}{2}}\left[\bigl(\phi_{\rm GB-}^i-V_t\bigr)^{\frac{-1}{2}}+\bigl(\phi_{\rm GB+}^i-V_t\bigr)^{\frac{-1}{2}}\right]^{-1} \tag{6}$$

where V_t is the thermal voltage. Note that to calculate the diffusion velocity, the dopant concentration used for the poly-Si resistor has been replaced by the concentration of the induced free-carriers for the intrinsic poly-Si TFT. The concentration of the induced free-carriers is calculated with the Fermi energy in the strong inversion condition and the extracted grain-barrier height [10]. Based on the Boltzmann approximation

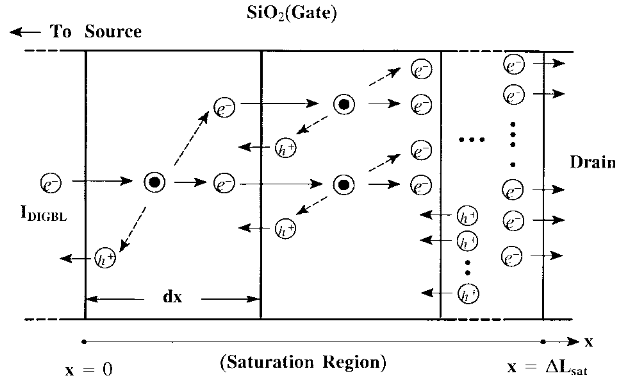

Fig. 1. Cross-sectional view of the saturation region in the intrinsic n-channel poly-SiTFT, which illustrates the multiplication process of the impact-ionization mechanism initiated by the DIGBL current, where ⊙ represents the Si atom-site; the arrow with the dashed line shows the path of the generated electron-hole pair.

$\bar{n}$ is expressed by

$$\bar{n} = n_i\exp\left(\frac{E_F-E_i|_{\rm inv}}{kT}\right). \tag{7}$$

This identification of the space-charge is important for correctly calculating the diffusion velocity of the free-carriers in the intrinsic poly-Si TFT and enables the extraction of the electrical parameters with reasonable values. Moreover, this conclusion is valid for both the intrinsic and doped poly-Si TFT's.

When the intrinsic poly-Si TFT operates in the kink regime, the impact-ionization of carriers occurs in the saturation region in which the lateral electric field is greater than the critical electric field $(\mathcal{E}_{{\rm imp},C})$. The impact-ionization mechanism in the saturation region is illustrated in Fig. 1, where $x=0$ is the beginning position for the occurrence of impact-ionization at which the electric field is equal to the critical value and the potential is equal to the saturation voltage $(V_{\rm DS,sat})$. As a first-order approximation, we assume that the critical electric fields for both the saturation of the carrier-velocity $(\mathcal{E}_C)$ [8] and the beginning of the impact-ionization $(\mathcal{E}_{{\rm imp},C})$ are reached in the same point of channel with the potential being $V_{\rm DS,sat}$. $\Delta L_{\rm sat}$ is the length of the saturation region and $x=\Delta L_{\rm sat}$ is the position of the drain junction.

The generated electrons together with the initiating ones from the DIGBL current form the total drain-source current

$$I_{\rm DS}(x) = I_{\rm DIGBL}+I_{{\rm imp},e}(x) \tag{8}$$

where $I_{\rm DS}(x)$ is the drain-source current composed solely of the *electron flow*, considering both the DIGBL effect and the impact-ionization mechanism, which will proceed to initiate the next impact-ionization when moving toward the drain; and $I_{{\rm imp},e}(x)$ is the impact-ionization current initiated by the electrons. The generated holes move toward the source *without* initiating impact-ionization. Naturally, the generation rate of the electron-hole pairs by the impact-ionization mechanism will be proportional to the quantity of the initiating electron flow. From the discussion above, we can obtain the differential equation for the variation of the impact-ionization current in

the saturation region as follows:

$$dI_{\mathrm{imp},e}(x) = \alpha(x)[I_{\mathrm{DIGBL}} + I_{\mathrm{imp},e}(x)]\,dx \tag{9}$$

where $\alpha(x)$ is the impact-ionization rate of the electrons; and dx is the incremental space along the channel. It is worthy to note that the DIGBL current participates in the impact-ionization mechanism but is *constant* over the whole channel region. This is because in the saturation region, the DIGBL current only contributes to initiate the impact-ionization current, and the impact-ionization current will not contribute to the DIGBL current. That is, the electrons of the generated electron-hole pairs are not added to the DIGBL current. The DIGBL current is completely calculated by (1). The variation of the drain-source current then comes mainly from that of the impact-ionization current and is expressed by

$$dI_{\mathrm{DS}}(x) = dI_{\mathrm{imp},e}(x). \tag{10}$$

With (8), (9) and (10), we can obtain

$$dI_{\mathrm{DS}}(x) = \alpha(x) I_{\mathrm{DS}}(x)\,dx. \tag{11}$$

In fact, (11) is a one-dimensional continuity equation of the drain-source current, which accounts for the impact-ionization mechanism of the intrinsic poly-Si TFT. By integrating both sides of (11) over the saturation region with the associated boundary conditions

$$I_{\mathrm{DS}}(x=0) = I_{\mathrm{DIGBL}}$$

and

$$I_{\mathrm{DS}}(x=\Delta L_{\mathrm{sat}}) = I_{\mathrm{DS},T} \tag{12}$$

and with the integration variable exchanged from the space x to the potential V, we can obtain

$$\int_{I_{\mathrm{DIGBL}}}^{I_{\mathrm{DS},T}} \frac{dI_{\mathrm{DS}}}{I_{\mathrm{DS}}} = \int_0^{\Delta L_{\mathrm{sat}}} \alpha(x)\,dx = \int_{V_{\mathrm{DS,sat}}}^{V_{\mathrm{DS}}} \alpha(\mathcal{E})\,\frac{dV}{\mathcal{E}} \tag{13}$$

where $\mathcal{E}$ is the lateral electric field. Thus, the total drain-source current considering both the DIGBL effect and the impact-ionization mechanism is obtained as follows

$$I_{\mathrm{DS},T} = I_{\mathrm{DIGBL}} \times \exp\left[\int_{V_{\mathrm{DS,sat}}}^{V_{\mathrm{DS}}} \alpha(\mathcal{E})\,\frac{dV}{\mathcal{E}}\right] \tag{14}$$

in which the impact-ionization rate can be derived based on the probability argument and is explicitly expressed as follows [11]

$$\alpha(\mathcal{E}) = \frac{q\mathcal{E}}{E_I} \times \exp\left(-\frac{E_I}{q\mathcal{E}\lambda}\right) \tag{15}$$

where E_I is the threshold energy of impact-ionization, which is $3/2$ times the bandgap energy of Si; λ is the optical-phonon mean free path of carriers in Si. Equation (14) intuitively shows that the drain-source current of the intrinsic poly-Si TFT with the kink effect comes from the mechanism of the impact-ionization *initiated* by the DIGBL current through the multiplication operation.

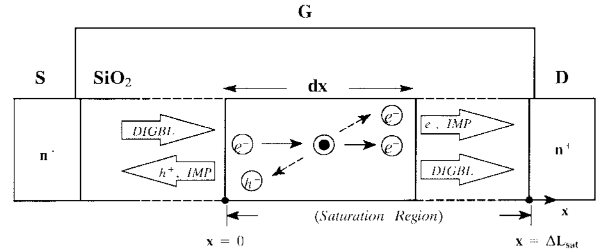

Fig. 2. Diagram illustrating the current continuity for the impact-ionization mechanism initiated by the DIGBL current in the intrinsic n-channel poly-Si TFT.

The physical meaning of the boundary conditions for the drain-source current within the saturation region can be identified to be consistent with the current-continuity condition and is illustrated in Fig. 2, in which it illustrates the continuity for the mechanism of the impact-ionization initiated by the DIGBL current. Initially, the electrons injecting from the source junction move toward the drain through the transport mechanisms combined in series, by surmounting the grain barriers, diffusing across the depletion regions near the grain boundaries, and drifting through the inversion regions between the depletion regions. This is the transport mechanism described by the interfacial-layer thermionic-diffusion model [9]. The DIGBL current is then formed and is constant over the whole channel region. Within the kink regime of the intrinsic poly-Si TFT, the electrons, from the DIGBL current, enter into the saturation region and perform the multiplication-ionization, as illustrated in Fig. 1. Additional electron-hole pairs are generated and the variation of $I_{\mathrm{DS}}(x)$ is governed by (11). The electrons and holes generated are separated by the high electric field and move toward the drain and source junction, respectively. When reaching the drain junction, the electron flows, coming both from the DIGBL current and the impact-ionization process, form the total drain-source current $I_{\mathrm{DS},T}$. On the other hand, it is important to note that the holes generated are not included as the initiating carriers for the impact-ionization mechanism, because the avalanche-breakdown of the intrinsic poly-Si TFT's is not observed from the experimental results. Thus, at the beginning of the saturation region where the electric field is of the critical value, $I_{\mathrm{DS}}(x=0)$ is equal to the DIGBL current and is the only source for initiating the impact-ionization mechanism. The DIGBL current and the hole flow generated from the impact-ionization mechanism, form the total drain-source current in the region near the source. Because the extra amount of electrons is equal to that of the holes through the electron-hole pairs generated and the DIGBL current is constant over the whole channel region, the total drain-source current obtained is then constant over the whole channel. Thus, the two boundary conditions considered for the drain-source current are reasonable, and are also the key points in determining whether the construction of this new analytical $I-V$ model is successful or not.

It is noted here that compared with the threshold energy of $3/2$ times Si bandgap for triggering the impact-ionization

process, the effect of carrier recombination is a high-order effect in determining the transport mechanism of the poly-Si TFT operating in the kink regime. Within the physical picture constructed in our $I-V$ model, the mechanism of carrier recombination occurs when the holes generated by the impact-ionization process move toward the source junction [4]. The electrons generated flow out the drain junction to be measured and meanwhile, extra electrons in addition to those due to the DIGBL current inject from the source junction into the channel and recombine with these holes. The impact-ionization current is then formed. Due to the high concentration of the trap states at the grain boundaries with energy level centering in the bandgap, the recombination rate of carriers is large enough that the recombination effect will not be the limiting process in determining the impact-ionization current. Although the mechanism of carrier recombination takes part in the formation of the impact-ionization current, the kink effect is dominated by the mechanism of the impact-ionization initiated by the DIGBL current.

To calculate the total drain-source current $I_{\mathrm{DS},T}$, the distribution of the electric field in the saturation region should be known first. The quasi-2-D method had been used to solve the Poisson's equation in the saturation region and shown that in this region, the distribution of the electric field is nonlinearly dependent on the position [12]. On the other hand, (14) possesses the freedom for the electric field in that any reasonable distribution of the electric field is allowable to be substituted into (14) to calculate the impact-ionization current, provided that the parameters used should be reasonably accepted. For simplicity, we will propose an empirical formula for the nonlinear dependence of the electric field on the position and then on the potential. It is given as follows:

$$\mathcal{E}(V) = \mathcal{E}_{\mathrm{imp},C}\left(\frac{V}{V_{\mathrm{DS,sat}}}\right)^{\gamma} \tag{16}$$

where $\mathcal{E}_{\mathrm{imp},C}$ is the critical electric field accounting for the occurrence of the impact-ionization within the saturation region; and γ is an empirical parameter indicating the nonlinear degree for the dependence of the electric field on the potential (and position). It is obvious that when γ is zero, the electric field is equal to the critical electric field over the whole saturation region and is given by

$$\mathcal{E}(V) = \mathcal{E}_{\mathrm{imp},C} \tag{17}$$

Substituting (17) into (14) with some mathematical manipulation, the drain-source current is obtained as follows:

$$I_{\mathrm{DS},T} = I_{\mathrm{DIGBL}} \times \exp\left[\alpha(\mathcal{E}_{\mathrm{imp},C})\frac{V_{\mathrm{DS}} - V_{\mathrm{DS,sat}}}{\mathcal{E}_{\mathrm{imp},C}}\right]. \tag{18}$$

Equation (18) will be appropriate for the $I-V$ simulation of the long-channel poly-Si TFT's because the weak dependence of the electric field on the position is considered. As γ is equal to unity, the electric field is given as

$$\mathcal{E}(V) = \mathcal{E}_{\mathrm{imp},C}\left(\frac{V}{V_{\mathrm{DS,sat}}}\right) \tag{19}$$

and the drain-source current can be obtained as

$$I_{\mathrm{DS},T} = I_{\mathrm{DIGBL}} \times \exp\left[\int_{V_{\mathrm{DS,sat}}}^{V_{\mathrm{DS}}} \alpha(\mathcal{E})\frac{V_{\mathrm{DS,sat}}}{\mathcal{E}_{\mathrm{imp},C}}\frac{dV}{V}\right] \tag{20}$$

where the integral in the exponent can not be obtained analytically and should be calculated with numerical integration. The calculation for this numerical integration is time-efficient as expected. Equation (20) will be appropriate for the $I-V$ simulation of the short-channel poly-Si TFT's because the strong dependence of the electric field on the position is considered.

III. Results and Discussion

In order to test the validity of the analytical model developed above, the intrinsic n-channel poly-Si TFT's were fabricated. An intrinsic poly-Si film of 1000 Å was deposited onto a 1500 Å TEOS buffer layer grown on glass by the LPCVD method and the intrinsic poly-Si film was annealed at 1000 °C for 4 h. After being patterned into individual devices, a 700 Å TEOS gate oxide was grown, and then another LPCVD poly-Si film of 2500 Å was deposited. The source, the drain, and the poly-Si gate were simultaneously implanted using phosphorus ions at 80 keV with a dose of 5×10^{15} cm^{-2}. It is noted that the poly-Si channel is undoped.

A. Parameter Extraction

The procedure of the parameter extraction can be divided into three steps. First, using the curve of ϕ_{GB} versus V_{GS} obtained from the Arrhenius plot of the drain-source current, the grain size, the density of the grain boundary states and the Fermi energy in the strong inversion condition are extracted with the analytical model of the grain-barrier height and the detail is presented in [10]. Second, based on the accurate modeling of the grain-barrier height with those parameters extracted previously, the parameters for the model of the interfacial-layer thermionic-diffusion current, including the maximum electron mobility in the surface channel (μ_0), the empirical constant of the surface-roughness scattering (θ), the effective thermal velocity of electrons across the grain boundary ($\theta_n \nu_{\mathrm{Rn}}$) and the scattering-limited velocity (ν_{sl}), are extracted from the transfer curve of the poly-Si TFT operating in the linear regime. After optimization of the transfer curves, the threshold voltage (V_T) extracted is 1.123 V. Third, the parameters for the DIGBL effect and the impact-ionization current are extracted from the output curves of the poly-Si TFT operating in the high V_{DS} regime. The critical electric field for velocity saturation ($\mathcal{E}_C$) and the nonlinear factor of the electric field (η) for the DIGBL effect are extracted by fitting the saturation point and the portion of the output curve before the saturation point. The critical electric field for impact-ionization ($\mathcal{E}_{\mathrm{imp},C}$) and the nonlinear factor of the electric field (γ) in (16) are extracted from the kink-portion of the output curve. It is noted that $\mathcal{E}_C$ is much smaller than $\mathcal{E}_{\mathrm{imp},C}$, as shown in Table I.

TABLE I
PARAMETERS USED TO SIMULATE THE $I-V$ CHARACTERISTICS

$L_M(\mu m)$	5	10	20	30	40
$\mu_0(cm^2/V-s)$	128.4	128.4	128.4	128.4	128.4
θ	0.753	0.753	0.753	0.753	0.753
$\theta_n \nu_{Rn}(10^6 cm/s)$	0.896	0.896	0.896	0.896	0.896
$\nu_{sl}(10^6 cm/s)$	8.0	8.0	8.0	8.0	8.0
η	0.65	0.50	0.45	0.30	0.25
$\mathcal{E}_C(10^4\,V/cm)$	4.0	4.0	4.0	4.0	4.0
$E_I(eV)$	1.68	1.68	1.68	1.68	1.68
$\lambda(\AA)$	76	76	76	76	76
γ	1.0	0.0	0.0	0.0	0.0
$\mathcal{E}_{imp,C}(10^5\,V/cm)$	7.2	10.0	6.2	5.8	5.6

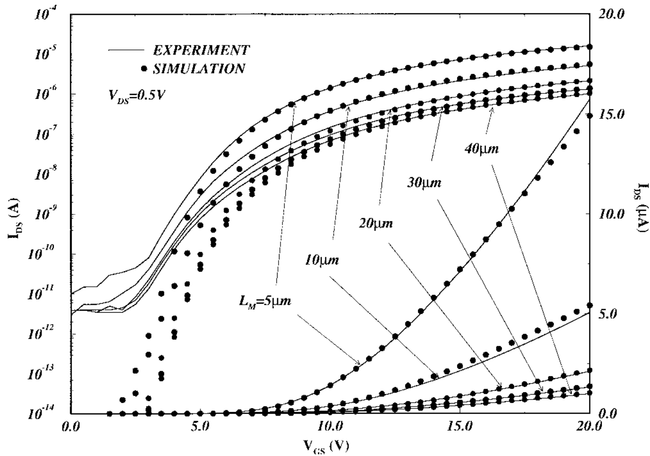

Fig. 3. Transfer curves of the intrinsic n-channel poly-Si TFT shown in both the logarithmic and linear scales.

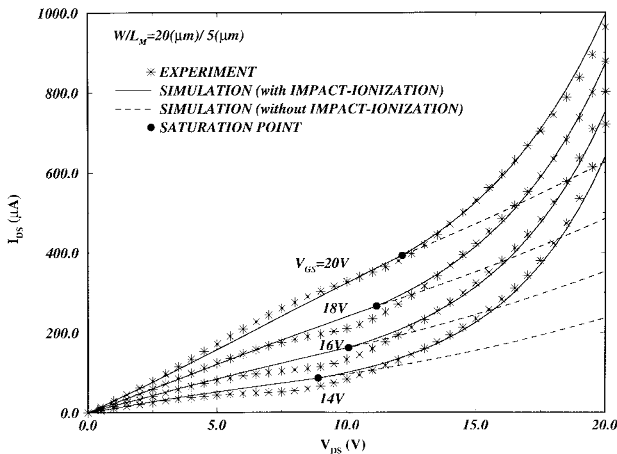

Fig. 4. Output characteristics of the intrinsic n-channel poly-Si TFT with $W/L_M = 20$ μm/5 μm.

B. $I-V$ Characterization

Fig. 3 shows the experimental and simulated transfer curves both with logarithmic and linear scales. Good agreement in the turn-on regime is obtained and the parameters extracted for the interfacial-layer thermionic-diffusion model are reasonable, as listed in Table I for devices with the mask-gate length (L_M) ranging from 5 μm to 40 μm. Due to the tilt etching-bias and the source(drain) dopant diffusion into the active poly-Si film, the effective channel length $(L_{\rm eff})$ will be less than

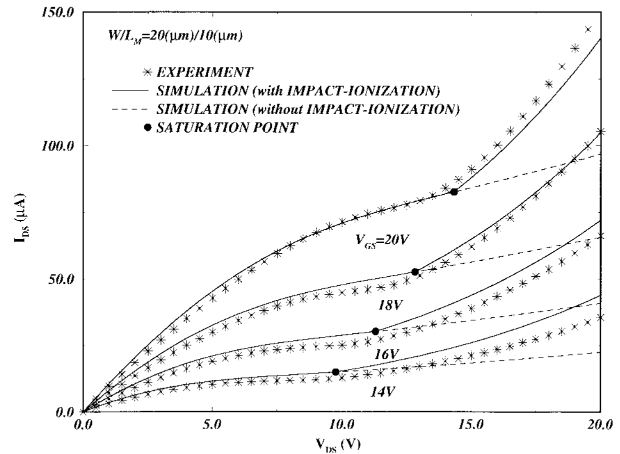

Fig. 5. Output characteristics of the intrinsic n-channel poly-Si TFT with $W/L_M = 20$ μm/10 μm.

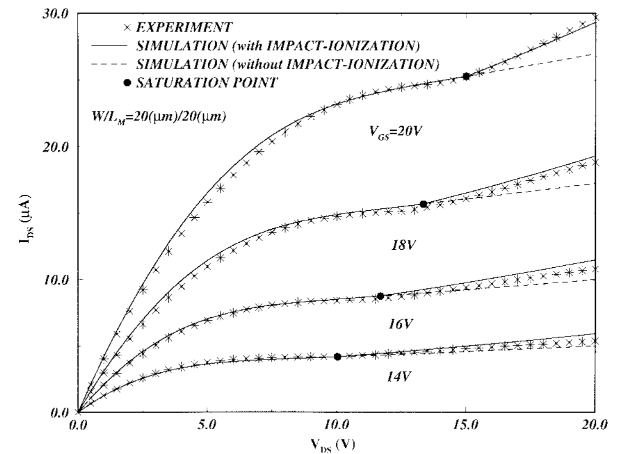

Fig. 6. Output characteristics of the intrinsic n-channel poly-Si TFT with $W/L_M = 20$ μm/20 μm.

the mask-gate length. The deviation between L_M and $L_{\rm eff}$ should be more carefully considered in determining the $I-V$ characteristics of the short-channel device. With optimization, the deviation of the effective channel length from the mask-gate length, $\Delta L = L_M - L_{\rm eff}$, is obtained to be 1 μm for the test devices used. Only one set of parameters is needed to accurately simulate the transfer $I-V$ characteristics. This consequence confirms the accuracy of the developed $I-V$ model with correctly resolving the physical parameters for the intrinsic poly-Si TFT's. The discrepancy in the subthreshold regime shown in the plot of logarithmic scale is due to the fact that the real distribution of the grain-boundary states is continuous within the bandgap. In the subthreshold regime, the sweep of the Fermi level over the continuous distribution of the grain-boundary states within the bandgap will result in the smoother variation of the current [6], [13], which is not considered in our model.

Figs. 4–8 show the experimental and simulated output curves and the solid and dashed lines represent the simulation results with and without considering the impact-ionization mechanism, respectively. With considering only the DIGBL effect, there will be large deviation presented in the kink

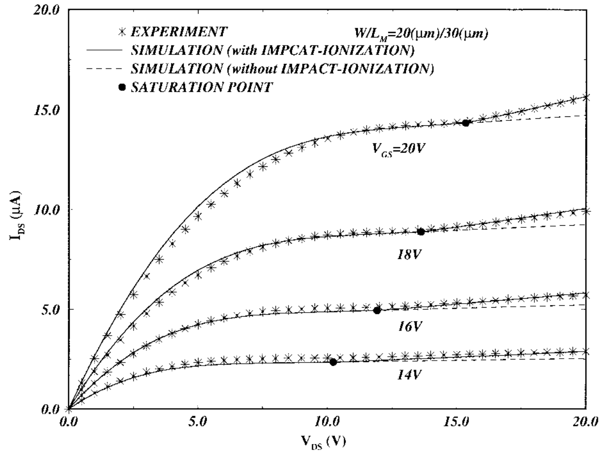

Fig. 7. Output characteristics of the intrinsic n-channel poly-Si TFT with $W/L_M = 20$ μm/30 μm.

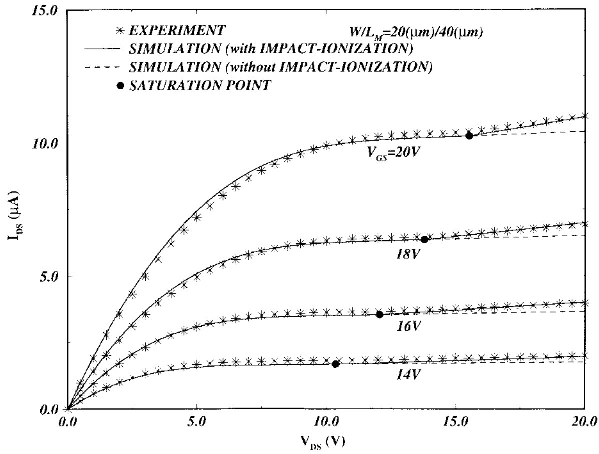

Fig. 8. Output characteristics of the intrinsic n-channel poly-Si TFT with $W/L_M = 20$ μm/40 μm.

regime between the measured and simulated output curves. On the other hand, by further considering the impact-ionization mechanism in the $I-V$ model, good agreements are obtained in both regimes dominated by the DIGBL effect (low $V_{\rm DS}$) and the kink effect (high $V_{\rm DS}$). The parameters used for simulation are listed in Table I. It is encouraged that excellent agreement is obtained even for the short-channel device with a mask-gate length of 5 μm. From these figures, it is shown that the impact-ionization of the carriers occurs in the high $V_{\rm DS}$ regime for the devices with various channel lengths. The degree of the impact-ionization increases with the decreased channel length, as expected. The nonlinear dependence factor of the electric field, γ, is zero for the devices with channel lengths being greater than or equal to 10 μm. For 5 μm mask-gate length, γ increases to unity. With the optical-phonon mean-free-path of carriers in Si at room temperature being used, the critical electric field for impact-ionization ($\mathcal{E}_{{\rm imp},C}$) extracted are within 10^5 V/cm regime, where the impact-ionization process normally occurs. $\mathcal{E}_{{\rm imp},C}$ also shows the decreasing dependence on the increased channel length. $\mathcal{E}_{{\rm imp},C}$ of a 5-μm device being smaller than that of a 10-μm one is due to the fact that γ of a 5-μm device is unity and its empirical formula of the electric field assumes larger magnitude and stronger dependence on the position than those of a 10-μm one with γ being zero. The complicatedly-behaved output characteristics of the intrinsic poly-Si TFT show strong contrast with the compact form of our analytical model for the impact-ionization current initiated by the DIGBL current.

IV. Conclusion

A new analytical model considering the impact-ionization mechanism initiated by the drain-induced-grain-barrier-lowering (DIGBL) current for the intrinsic n-channel poly-Si TFT has been established. The output characteristics of the intrinsic n-channel poly-Si TFT with the DIGBL effect and the impact-ionization mechanism in the low and high $V_{\rm DS}$ regimes, respectively, can be well simulated by the new $I-V$ model established. With these physical mechanisms for both the formation of the grain-barrier height and the transport mechanisms being correctly resolved, the model proposed will be able to well characterize the electrical properties of the intrinsic n-channel poly-Si TFT. The accuracy of this model is also supported by the reasonable values of the physical parameters extracted. Therefore, it can serve as a reliable analyzer to correlate the relationship between the fabrication conditions and the electrical characteristics and will be beneficial to further understand the underlying physics of the intrinsic n-channel poly-Si TFT.

References

[1] T. Tanaka, H. Asuma, K. Ogawa, Y. Shinagawa, and N. Konishi, "An LCD addressed by a-Si:H TFT's with peripheral poly-Si TFT circuits," in *IEDM Tech. Dig.*, 1993, pp. 389–392.

[2] T. Aoyama, K. Ogawa, Y. Mochizuki, and N. Konishi, "Inverse staggered poly-Si and amorphous Si double structure TFT's for LCD panels with peripheral driver circuit integration," *IEEE Trans. Electron Devices*, vol. 43, pp. 701–705, May 1996.

[3] S. D. S. Malhi *et al.*, "Characteristics and three-dimensional integration of MOSFET's in small-grain LPCVD polycrystalline silicon," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 258–281, Feb. 1985.

[4] M. Validinoci, L. Colalongo, G. Baccarani, G. Fortunato, A. Pecora, and I. Policicchio, "Floating body effects in polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 44, pp. 2234–2241, Dec. 1997.

[5] G. A. Armstrong, S. D. Brotherton, and J. R. Ayres, "A comparison of the kink effect in polysilicon thin film transistors and silicon on insulator transistors," *Solid-State Electron.*, vol. 39, no. 9, pp. 1337–1346, Sept. 1996.

[6] M. Hack, J. G. Shaw, P. G. Lecomber, and M. Willums, "Numerical simulations of amorphous and polycrystalline silicon thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 29, no. 12, pp. L2360–L2362, 1990.

[7] S. Yamada, S. Yokoyama, and M. Koyanagi, "Two-dimensional device simulation for polycrystalline silicon thin-film transistor," *Jpn. J. Appl. Phys.*, vol. 29, no. 12, pp. L2388–L2391, 1990.

[8] P. S. Lin, J. Y. Guo, and C. Y. Wu, "A quasi-two-dimensional analytical model for the turn-on characteristics of polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 666–674, Mar. 1990.

[9] C.-Y. Wu and W.-D. Ken, "A new computer-aided simulation model for polycrystalline silicon film resistors," *Solid-State Electron.*, vol. 26, no. 7, pp. 675–684, 1983.

[10] H. L. Chen and C. Y. Wu, "An analytical grain-barrier height model and its characterization for intrinsic poly-Si thin-film transistors," *IEEE Trans. Electron Devices,* vol. 45, pp. 2245–2247, Oct. 1998.

[11] S. Wang, *Solid-State Electronics*, New York: McGraw-Hill, 1966, p. 359.

[12] G.-S. Huang and C.-Y. Wu, "An analytic saturation model for drain and substrate currents of conventional and LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-37, p. 1667, July 1990.

[13] M. D. Jacunski, M. S. Shur, and M. Hack, "Threshold voltage, field effect mobility, and gate-to-channel capacitance in polysilicon TFT's," *IEEE Trans. Electron Devices*, vol. 43, pp. 1433–1440, Sept. 1996.

Hsin-Li Chen (S'95) was born in Tainan, Taiwan, R.O.C., on January 2, 1969. He received the B.S. degree in electrical engineering from National Tsing-Hua University, Taiwan, in 1991, and is currently pursuing the Ph.D. degree in the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.

His present research areas focus on the physical modeling and reliability issues of the amorphous and polycrystalline silicon thin-film transistors.

Ching-Yuan Wu (M'72), for a photograph and biography, see this issue, p. 695.