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Optimization of Multilayer Thin Film Passivation Processes for Improving Cache Memory Device Performance

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A multilayer thin film passivation structure based on alternating plasma-enhanced chemical vapor deposited (PECVD) SiO_x-SiN_x layers are prepared and characterized, in order to improve and optimize the electrical performance and hot carrier reliability of polyload resistors in 4-transistor (4-T) cache static random access memory devices. SiH_4-N_2O gas mixtures are utilized as precursors for oxide CVD process. Adopting a higher SiH_4/N_2O flow rate ratio during deposition renders the resulting oxide films more silicon rich, as manifested by their higher refractive index (RI) and wet etch rates. These modifications in film characteristics are also accompanied by enhanced resistance of polyload resistor and lower percentage hot-carrier linear drain current (I_{dlin}) degradation. An increase in RI from 1.46 to 1.67 translates to a rise in resistance of polyload resistor from 98 to 225 GΩ and a fall in I_{dlin} from 5.8 to 4.5%. Further improvement in device performance can be realized by modifying the stoichiometry of the overlying nitride passivation layer. This is achieved by increasing bias power while reducing the SiH_4/NH_3 gas flow rate ratio during the PECVD nitride deposition process. The nitride films thus deposited contain lower Si–H bond density, and exhibit lower buffered oxide etch rates and compressive stress. Passivation structures based on the combination of a high RI oxide and a low Si–H content nitride layers yield the most promising device performance and reliability. Defect species in the oxide passivation layer are identified and their charge trapping mechanisms clarified. Impact of moisture and hydrogen from the passivation on polygate and load resistor are both held responsible for device degradation. Interfacial defect reactions involving both hydrogen and moisture are proposed to account for the carrier trapping mechanisms responsible for device failure.
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Reliability and electrical characteristics of integrated circuit memory devices have been subjects of extensive research due to concerns over device yield and performance. During the past few years, growing attention has been paid to the impacts of material issues, such as interlayer dielectric (ILD) and passivation layers, rather than the active gate area alone, on device performance and reliability. For 4-transistor (4-T) cache static random access memory (SRAM) devices, reliability and performance issues such as hot-carrier-induced degradation,[1-2] time-dependent dielectric breakdown,[3] and polyload resistor,[4,5] have all seen influences from their passivation layers, whose material characteristics play a significant role.

Hot carrier reliability is a common device performance issue for all memory products. Although the exact mechanism is not yet clear, experimental data accumulated over the last ten years have led people to hypothesize that, during electrical biasing, hydrogen- or water-related species diffused in from ILD or passivation layers present extra mobile charges and induce impact ionization along the oxide/substrate interface, leading to hot carrier degradation. It is from this perspective have intensive research activities been focused on the enhancement of hot carrier lifetime through improvement in moisture resistance and reduction in hydrogen content of the ILD and passivation layers.

Specifically, for high speed cache SRAM, the electrical characteristics of poly-Si load resistor is one of the most critical issues to device performance and reliability. The resistance should be kept as low as possible during the programming cycle when a pull-up voltage passes through the polyload resistor. Conversely, on the other extreme, the resistance of a poly-Si load resistor should be as high as possible to prevent excessive power consumption. Therefore, the resistance shift of the poly-Si load resistor induced, for example, by mobile charges released from surrounding ILD layers will lead to fluctuation and degradation in device performance, manifested by speed slowdown, power consumption, and heat dissipation. Such phenomenon may also arise from hot carrier injection into the polyload resistor during the programming cycle, further degrading the device performance. Ion contamination[5] and humidity[8] have been held responsible as the charge loss mechanisms. Overall, the salvation for hot carrier and charge loss seems both to point to the modification in material characteristics of ILD and passivation layers for better moisture and ion resistance.

The introduction of a higher dangling bond density to intermetal oxide by incorporating more Si–H bonds into it during the plasma enhanced chemical vapor deposition (PECVD) process has been demonstrated to be an effective way of improving hot carrier lifetime.[9,10] The extra dangling bonds may act as trap centers for the hydrogen evolved from nitride passivation on the top. Alternatively, water diffusion from, for example, spin-on glass used as intermetal dielectric (IMD) layer may be responsible for hot carrier degradation.[7] Just recently, water diffusion is perceived to be the main cause of tunnel oxide degradation for flash memories.[11] Nevertheless, distinction between the two operating mechanisms (hydrogen or water diffusion) appears vague and further evidence is required to verify this point. In this investigation, we modified the stoichiometry, refractive index, stress, and other characteristics of PECVD SiO_x-SiN_x stacked passivation layers in order to improve hot carrier reliability and optimize memory device performances of 4-T cache SRAM. The trap centers in the oxides are identified and their trapping mechanisms are elucidated. Possible interfacial defect reactions are proposed to account for the hot carrier degradation mechanisms involving both hydrogen and moisture.

Experimental

Film deposition and characterization. The cross-sectional view of the 4-T SRAM device used in this study is depicted in Fig. 1a. Probable paths for hydrogen diffusion and moisture permeation are also shown here. The device consists of four 400 nm n-channel metal oxide semiconductor (NMOS) structures and two Al-based interconnection layers. The first layer of polysilicon serves as the gate electrode of the two storage transistors (C) and access transistors (T) while the second layer of polysilicon functions as the load resistors (L), as depicted in Fig. 1b. The spacing for metal-1 and metal-2 are 500 and 600 nm, respectively. Low-pressure chemical vapor deposited boron phosphorus silicon glass (BPSG) (500 nm) containing 4 wt % boron and 4 wt % phosphorus was used as the ILD layer with $SiH_4 + B_2H_6 + PH_3 + O_2$ chemistries. Figure 2a is the cross-sectional scanning electron microscope micrograph of the SRAM device fabricated using the process described above. The polygates,

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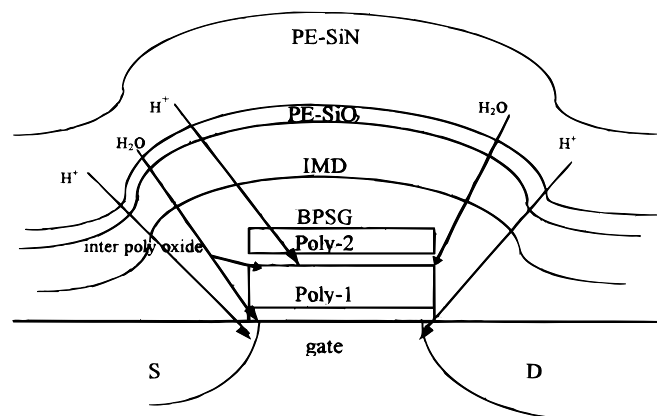
resistors, and metal-1 can be clearly seen. The double layer passivation structures laid on top of metal-2 are depicted in Fig. 2b. As shown, a thin (100 nm) PECVD oxide was deposited prior to a 400 nm nitride due to the narrow metal-2 line spacing.

PECVD SiO_x-SiN_x (100-400 nm) stacked layers were utilized as passivation. Both oxides and nitrides were deposited at 400°C in a modified dual frequency PECVD reactor, in which a low frequency (375 KHz) radio frequency (rf) bias power was applied onto the wafer to enhance ion bombardment for film quality improvement. Meanwhile high frequency (13.56 MHz) rf power was applied onto gas inlet for gas decomposition. For PECVD oxides, N_2O gas flow rate was maintained at 4.8 L/min, while SiH_4 gas flow rate and low/high frequency power ratio were varied in order to induce different stoichiometry in the oxide films. For comparison, 400 nm of subatmospheric (SA) CVD oxide layers based on ozone (O_3) and tetraethoxysilane (TEOS) chemistry were prepared at 400°C under a chamber pressure of 450 Torr. The SACVD oxide also serves as the gap-filling dielectric between narrow spacing of metal-2 lines. For nitrides, SiH_4 and NH_3 gases were mixed at different proportions with different low/high frequency power ratios to modify film characteristics. After passivation, the thin film stack was annealed in N_2 at 400°C for 30 min to stabilize the structure.

The impact of changes in film characteristics on device performance was evaluated. Fourier transform infrared spectroscopy (FTIR) and thermal desorption spectroscopy (TDS) were employed to measure film characteristics such as bond density, moisture, and hydrogen content. Bond densities were calculated from FTIR peak areas of the respective bond signals.



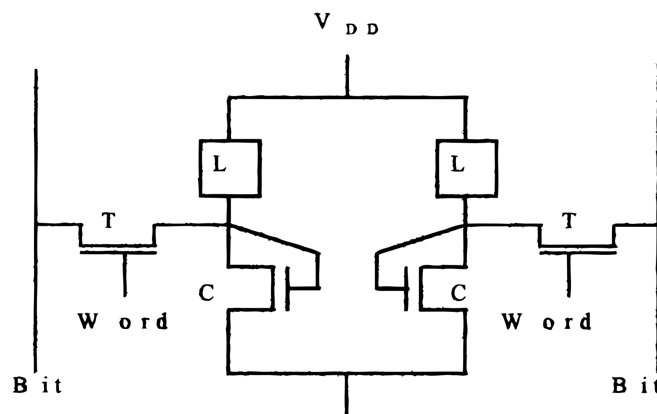
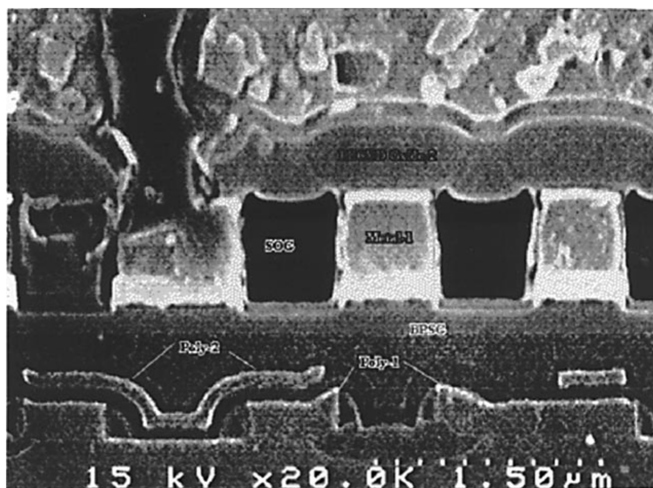


Figure 1. Schematic of (a, top) 4-T SRAM showing the paths of mobile ion diffusion to the poly-2 resistor and active device region. (b, bottom) Flip-flop 4-T SRAM showing the two load resistors (L), two storage transistors (C), and two access transistors (T).



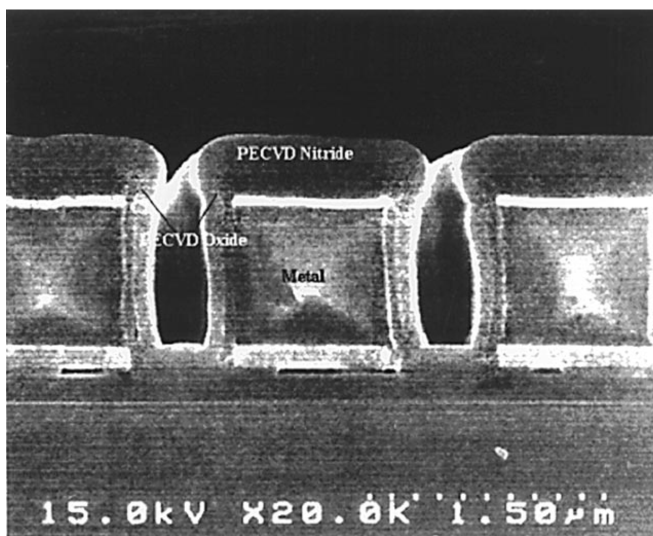


Figure 2. Cross-sectional view of (a, top) 0.4 μm double-poly-Si double-metal 4-T SRAM device using second poly silicon layer as the load resistor. (b, bottom) 0.4 μm 4-T SRAM multilayer passivation by using PECVD SiO_2 + SiN_x.

EPMA and EPR analyses.—Electron probe X-ray microanalyzer (EPMA) and electron paramagnetic resonance (EPR) techniques were employed, respectively, to further characterize the stoichiometry and dangling bond density of the oxides and nitrides. Thermally grown wet oxides were used as the reference for quantitative determination of atomic ratio and bond density. The EPMA analysis was conducted with a JEOL JXA-8800M analyzer. The EPR analysis was conducted using a Bruker EMX-10 spectrometer under a center field of 3489.9 G with width of 50 G. The microwave frequency is set at 9.779 GHz with a power of 19.971 mW. The receiver modulation frequency and its amplitude are 100 KHz and 1.6 G, respectively.

Device reliability tests.—Hot carrier (HC) degradation tests were carried out using an NMOS field effect transistor (FET) structure. The channel width and length are 20 μm and 400 nm, respectively, and the gate oxide thickness is 7.5 nm. The hot carrier stress is imposed at the bias condition giving the maximum substrate current. Typical stress conditions were V_d = 6.0 V and V_g = 3.3 V. After HC stressing, the source and drain terminals were reversed for I_d measurement again and the percentage of degradation of drain current in the linear portion, I_{dlin}, was calculated from the average of 5 measurements per experimental condition. For programming speed and power consumption concerns, the resistance of polyload resistor is

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Table I. Film characteristics of PECVD oxides used in this study.

SiH_4/N_2O ratio	rf power ratio (LF/HF)[a]	D/R (nm/s)	RI	EPMA atomic ratio (O/Si)	Normalized dangling bond ratio	Stress (MPa)	BOE E/R (nm/min)
0.05	0	12.10	1.46	2	1	530	223
0.06	0.67	6.90	1.51	1.46	1.07	−680	120.7
0.08	0.82	8.02	1.54	1.46	1.22	−44	156.5
0.10	1.00	8.39	1.56	1.43	1.61	62	179.8
0.13	1.22	9.20	1.67	1.28	1.67	137	186.6

[a] LF: low frequency; HF: high frequency.

measured and calculated also from the average of five measurements per experimental condition.

Results

Film Characteristics

PECVD oxides.—Results of material characterization for PECVD oxides used in this study are listed in Table I. Initially, the application of a low-frequency bias power densifies the oxide film and reduces porosity significantly through enhanced ion bombardment. This is manifested by the marked decrease in wet etch rate (223 to 120.7 nm/min) and a corresponding shift in stress from tensile (530 MPa) to compressive (−680 MPa). As both SiH_4 flow rate and rf bias power increase, however, deposition rate (D/R), refractive index (RI), and etch rate (E/R) all increase, while, in the mean time, the stress reverses from high compressive (−680 MPa) to medium tensile (137 MPa). The increase in etch rate suggests a reduction in film density, despite the intensified ion bombardment induced by the increase in bias power. Since a higher bias power corresponds to enhanced ion bombardment and therefore a higher film density, and compressive stress,[12] the changes in film characteristics should be mainly the consequence of stoichiometric (i.e., compositional) effects rather than physical ion bombardment. As the SiH_4 flow rate increases, more silicon is being introduced into the oxide network, modifying the film characteristics. The incorporation of additional adsorbed Si phases into the film tends to inhibit perfect growth locally leading to elongated bonds and/or extra silicon dangling bonds and hence a tensile stress component[13] and enhanced chemical activity. The etch rate, in turn, increases correspondingly. The change in stoichiometry and the increase in dangling bond density are both evident from results of EPMA and EPR analysis, as shown in Table I. Increasing the SiH_4/N_2O gas flow rate ratio over 0.06 renders the resulting silicon oxide films more silicon-rich (O/Si ratio is <2) with higher dangling bond density. These changes would be crucial in fine-tuning the device reliability, as is discussed later in more detail.

Based on the above-mentioned perspective, the continuous rise in RI from that near the stoichiometric oxide (1.46) to 1.67 with increasing silane flow rate should be the consequence of increased silicon richness, instead of the densification effect, in the resulting oxide films. This finding is similar to at least one previous study,[14] which attributed the change of RI in annealed PECVD oxides to the alteration in Si–O bond chemistry rather than densification in oxide network. Overall, the chemical (compositional) attributes seems to dominate over the physical bombardment and densification effects in the modification of film characteristics.

Changes in relative bond density and RI of oxides in Table I are plotted against SiH_4 flow rate in Fig. 3a. Normalized peak height for Si–O–Si (stretching), Si–H, and Si–O–H bonds are included to represent their respective bond densities. As more SiH_4 gas was added to the deposition process, both Si–O–Si and Si–O–H bond densities decreased while the Si–H bond concentration increases slightly. The additional Si atoms are incorporated in form of Si–H bonds. The existence of a higher Si–H bond density corresponds to a higher dangling bond density in the oxide.[9] The peak position also shifts due to this change in chemical composition. Table II summarizes the shifts in peak position and relative peak height of the three different bonds. Si–O–Si (stretch), Si–H, and Si–O–H bands all move to lower wave numbers as more Si is present. Note that for stoichiometric SiO_2, the Si–O–Si stretch band should be positioned around 1067 1/cm, corresponding to an RI of 1.452. The lower wavenumbers for Si–O–Si stretch band in the silicon-rich oxides (SRO) correlate well their higher RI as seen in Fig. 3a. The decrease in Si–O stretching frequency to lower wavenumbers with increasing silicon richness agrees well with the observation by Lucovsky et al.[15]

Buffered oxide etch (BOE) rate, RI, and moisture content of SRO are replotted against the SiH_4/N_2O flow rate ratio in Fig. 3b. The moisture content, expressed in weight percent, is determined by thermal deposition spectrometer. Etch rate and RI both increase monotonically with increasing silicon content except for the oxide with $SiH_4/N_2O = 0.05$, whose high etch rate is attributed to the lack of rf bias power and, hence, lower density. Regarding the moisture content, the incorporation of more Si–H bonds into the oxide drives the

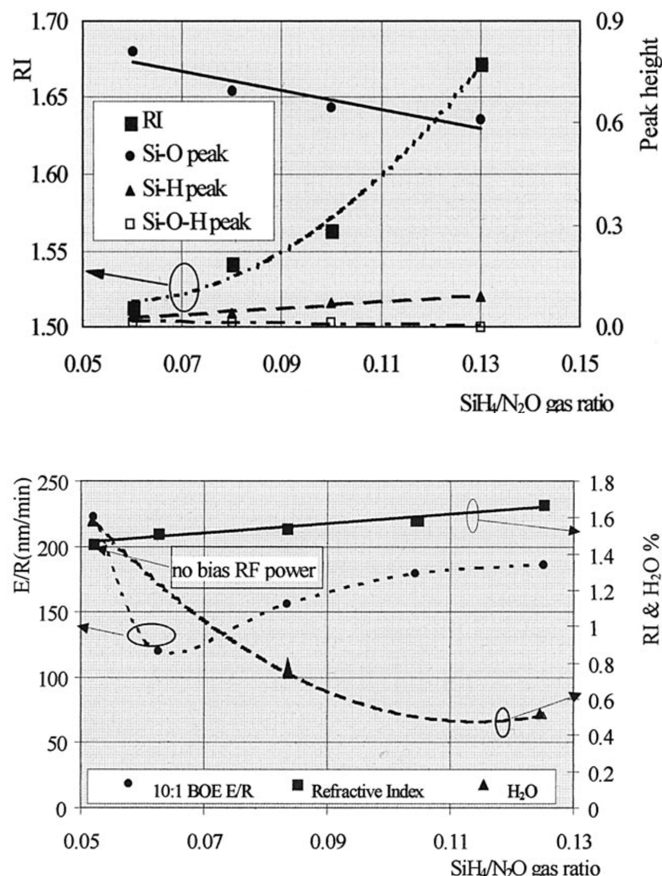

Figure 3. (a, top) RI and relative peak ratio of PECVD silicon-rich oxides. (b, bottom) The BOE etch rate, RI, and TDS H_2O release percentage vs. SiH_4/N_2O gas flow ratio in PECVD SRO.

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Table II. Shift in FTIR peak position and relative peak height for Si–O, Si–H, and Si–O–H bonds in PE-oxides as a function of SiH_4 flow rate.

SiH_4/N_2O ratio	Si–O stretch (1/cm)	Si–O peak height	Si–H (1/cm)	Si–H peak height	Si–O–H (1/cm)	Si–O–H peak height
0.06	1049	0.811	2272	0.029	3385	0.014
0.08	1041	0.693	2252	0.042	3383	0.013
0.10	1035	0.644	2245	0.073	3377	0.013
0.13	1032	0.609	2241	0.090	3372	0.001

Table III. Film characteristics of PECVD nitrides used for this study.

Item, sample	Unit	SIN1	SIN2	SIN3	SIN4	SIN5
SiH_4/NH_3 ratio	—	0.20	0.13	0.08	0.05	0.03
EPMA atomic ratio	Si/N		1.43	0.99	0.87	0.81
Si-H density	10^{22} cm^{-3}	1.48	1.39	0.87	0.049	0.0002
N-H density	10^{22} cm^{-3}	0.27	0.39	0.66	1.21	1.23
Si-H/N-H ratio	—	5.48	3.58	1.32	0.04	0.0002
Stress	MPa	490	64	−290	−940	−980
Film Density	g/cm^{-3}	1.94	2.45	2.56	2.73	3.04
10:1 BOE E/R	nm/min	40.4	23.9	23.3	23	18.8
CMP R/R	nm/min	211.9	165.8	−119.7	99.7	80

water molecules off because the reduction in Si–O–H bonds gives rise to increased hydrophobicity in the oxide.

PECVD nitrides.—Film characteristics of nitrides used for this study are summarized in Table III. Samples SIN1 to SIN5 represent nitrides with different silicon to nitrogen ratios. Both BOE etch rate and chemical mechanical polishing (CMP) removal rate (R/R) decrease with increasing NH_3/SiH_4 flow rate ratio used for deposition. Concurrently, the stress changes from medium tensile to high compressive as more hydrogen is being incorporated into the nitride. The high compressive stress and, very likely, high density contribute to the low etch and CMP rates. The increase in compressive stress and density with increasing nitrogen content (N–H bonds, to be specific) in silicon nitride agrees well with results of previous studies.[16,17]

Besides the Si_3N_4 tetrahedral that compose the three dimensional network, the structure of the nitride films which are nitrogen-deficient contains significantly more Si–H bonds, while the nitrogen-rich films have significantly more N–H type bonds.[17] All the nitrides in Table III are nitrogen deficient since a stoichiometric nitride should contain a N/Si ratio [approximated by FTIR absorption area ratio of (N–H + Si–N)/(Si–H + Si–N)] of 1.333 while the maximum N/Si ratio reaches only 1.05 in the SIN5 sample. This is supported by the EPMA results, which clearly indicate that the Si/N ratios for all nitrides analyzed are greater than the stoichiometric value of 0.77. Also observed in Table III is that the total hydrogen content (approximately, Si–H + N–H) decreases from SIN1 to SIN5, with decreasing SiH_4/NH_3 gas ratio. In these nitrogen deficient films, the existence of hydrogen in nitride may disrupt the tetrahedral Si–N configuration[18] and, hence, reduce the density.

As shown in Fig. 4a, the presence of more N–H bonds in the nitride structure apparently tunes the stress into high compressive, which is also an indicative of high film density. The shorter bond length and smaller bond angle of N–H (1.008 Å, 107°)[18] relative to those of Si–H (1.483 Å, 110°)[18] and Si–N (1.74 Å, 109°)[19] may have contributed to the high density and high compressive stress. From another perspective, the supply of more NH_3 gas into the reaction helps reduce SiH_4 partial pressure and, hence, the amount of gas phase reaction.[16] Such a gas phase reaction is said to cause particulates or haze, resulting in lower density and higher etch rates of the film. Therefore, nitride films deposited with lower SiH_4/NH_3 ratios would be denser. This is further supported by the results in Fig. 4b, which shows that as the N/Si ratio increases in nitride films, the BOE wet etch rate and CMP removal rate both decrease. The higher film density and compressive stress result in a decrease in water diffusion coefficient of the film,[20,21] leading to lower leaching and etching rates during chemical attack. Hence we demonstrated that by modifying the

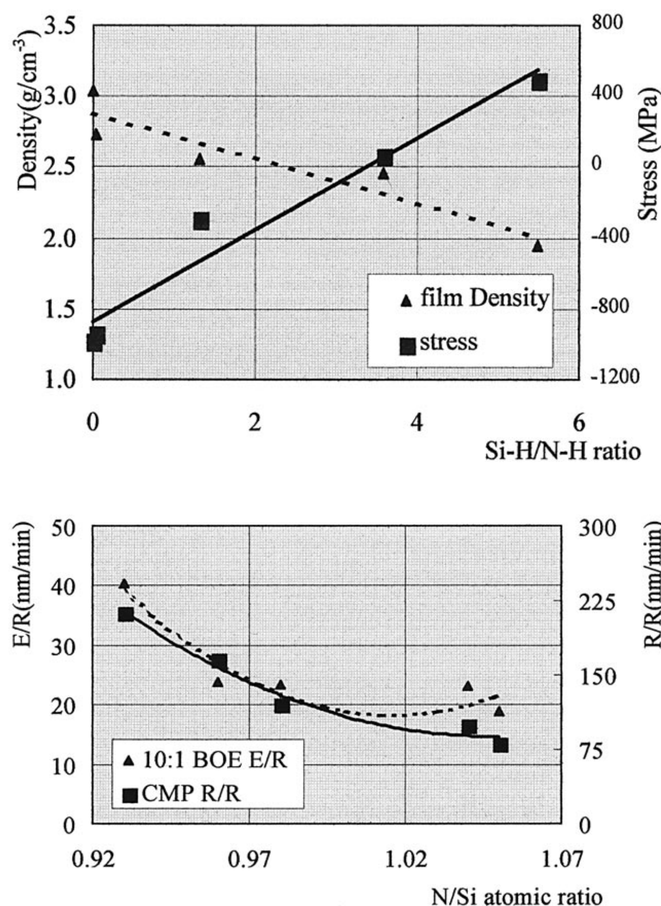

Figure 4. Effect of PECVD nitride film (a, top) Si–H/N–H bond ratio on film density and stress. (b, bottom) Nitride film nitrogen vs. silicon atomic ratio on chemical wet etch rate and CMP removal rate.

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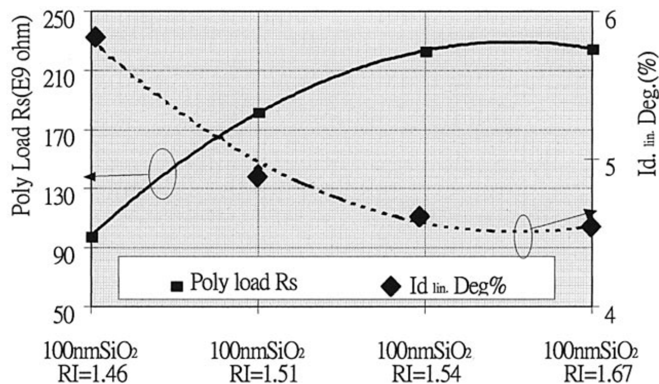

Figure 5. The variation in resistance of polyload resistor and degradation in linear drain current (I_{dlin}) of devices with SRO of different RI.

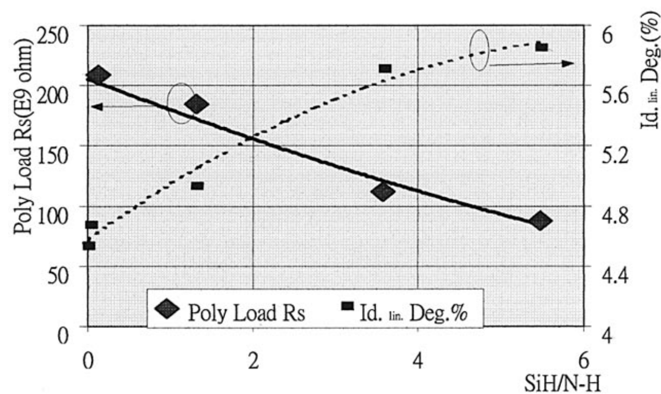

Figure 7. Variations in polyload R_s and I_{dlin} for SRAM devices with nitride passivation layers of different Si–H/N–H bond ratio.

deposition conditions, we can manipulate the film density, chemical resistance and mechanical strength of PECVD silicon nitride.

Device Reliability

Figure 5 shows the impacts of material characteristics of oxide passivation layers on device reliability. RI is chosen as the indication for oxide quality since it reflects the composition and dangling bond density.[22] In all cases, a nitride layer with medium hydrogen concentration (i.e., SIN3 in Table III, N–H + Si–H = 19.1×10^{21} cm^{-3}) was laid on top of the silicon-rich oxide. The results suggest that, as the RI of the SRO increases, the percentage of hot carrier linear drain current degradation decreases while the resistance of polyload resistor increases. With an increase in oxide RI from 1.46 to 1.60, I_{dlin} is reduced from 5.8 to 4.5%, and the polyload R_s increased from 98 to 225 GΩ. Such device electrical performance can be related to the superior moisture and mobile ion trapping capability of Si-rich oxide films.[22] This point is elaborated later. Effects of adding a SACVD gap-filling oxide layer on device performance are also included to evaluate the thickness effect of passivation layer. The gap-filling layer with a thickness of 400 nm was deposited on top of a 100 nm standard PECVD oxide (RI = 1.46) or silicon-rich (RI = 1.50) oxide based on ozone-TEOS chemistry. The results in Fig. 6 indicate that incorporation of this SACVD gap-filling layer into the passivation scheme has merely marginal influence on polyload resistance and linear region drain current degradation. Only minimal change in device performance can be realized, whether this SACVD oxide layer is deposited along with a standard PECVD oxide with RI = 1.46 or a PECVD SRO with RI = 1.50. Thus, changes in film stoichiometry rather than thickness, as reflected by variation in RI, have much more pronounced effects as shown in Fig. 5.

The effects of nitride film characteristics on I_{dlin} and resistor R_s are shown in Fig. 7. In this case, a 100 nm PECVD SRO layer with

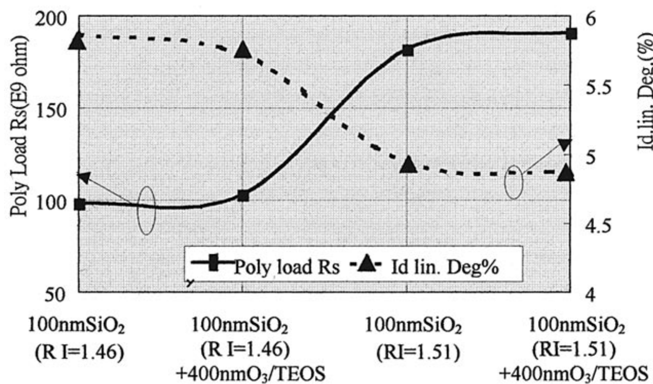

Figure 6. Variations in polyload R_s and I_{dlin} for SRAM devices with PECVD and SACVD oxide layers.

RI = 1.50 was deposited prior to the nitride passivation. As more Si–H bonds are incorporated into the nitrides, the device exhibits higher percent change in I_{dlin} and lower polyload resistance, signifying a degradation in device performance. An increase of Si–H/N–H bond ratio from nearly 0 to 5.5 corresponds to a drop in polyload resistance from 210 to 88 GΩ and a rise in I_{dlin} from 4.6 to 5.9%. The result suggests that the presence of Si–H bonds has an adverse effect on SRAM device performance. Note that a nitride with low Si–H bond density also exhibits high moisture and etching resistance due to the increase in film density and compressive stress. The PECVD nitride film material characteristics account for the mechanism of device electrical performance. A high Si–H bond density in the film corresponds to high porosity, tensile stress (high bond strain), and high hydrogen content. The high porosity in the film provides more vacancies and diffusion paths to accommodate moisture and mobile ions released from the loose bonded nitride film or from the ambient. The existence of tensile stress weakens the bond strength and enhances moisture and mobile ion diffusion through the film. Finally, the high hydrogen content in the film (e.g., SIN1) combined with the aforementioned high defectivity and diffusion rate probably leads to an enhanced hydrogen release rate during subsequent thermal processing (e.g., anneal), resulting in hydrogen accumulation along the gate oxide-Si interface and hence accelerated impact ionization and hot carrier degradation rate.

Discussion

The above-mentioned results indicate that passivation layers based on the combination of a silicon-rich oxide and a nitride with a low Si–H content give rise to the lowest NMOS linear region drain current and polyload resistance degradation. In addition, a rise in polyload resistance correlates well with the reduction in NMOS linear region drain current degradation, whenever a change in oxide or nitride film characteristics occurs. This observation implies that the two artifacts may share the same origin that leads to their respective operating mechanisms.

As mentioned in the introduction part of this paper, previous investigations on process-induced hot carrier degradation attributed the failure mechanisms to either hydrogen or water diffusion that causes carrier trapping and impact ionization. Results of the present study seem indicate that both hydrogen and moisture are responsible for device degradation. The moisture diffused from oxide and hydrogen released from nitride films would both impact the poly-Si, causing charge loss and device degradation.[8] These moisture and hydrogen (OH^- and H^+) radicals also provide mobile charges and lower the electrical resistance of the polyload resistor. The mean diffusion length, $2\sqrt{Dt}$, for H, H_2, and H_2O in silica at 400°C for 5 min is 740, 174, and 0.4 μm, respectively.[11] The moisture is more likely to be present in the form of hydroxyl groups (OH^-) instead of H_2O molecules, so that a faster diffusion rate is expected. In a recent study, Haque et al.[23] proposed that the bond strain of a PECVD oxide can be reduced through reaction with moisture to form near neighbor

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silanol (Si–O–H). Based on this scenario, moisture present in the oxide may react with the Si–O bonds and become trapped within the oxide. The trapping efficiency would be greater in silicon-rich oxides due to their higher Si–H bond density. In fact, these Si–H bonds are more likely to exist in form of $Si–H^+$ rather than Si–H, since the bonding energy of the former is much larger (~3.35 eV) than the latter (~2.50 eV).[19] As a consequence, the positively charged $Si–H^+$ radicals can easily attract the negative hydroxyl (OH^-) groups, reducing the moisture release during annealing and protecting the device from hot carrier degradation.

The fast diffusion of hydrogen atoms can certainly be held responsible in part for the electrical degradation caused by oxide and nitride passivation. Since oxide is inserted beneath the nitride layer, water diffusion may be the dominant device degradation mechanism in the case of a linear oxide. In addition, the silicon-rich oxide, with its abundant dangling bonds, can trap effectively the mobile hydrogen released from the top nitride, forming additional Si–H bonds along the oxide-nitride interface. On the other extreme, the incorporation of a stoichiometric oxide layer provides higher moisture content and poor trapping capability for hydrogen, both of which pose negative impact on hot carrier lifetime. Based on this study, a nitride film with a low Si–H bond concentration deposited on top of a high-RI SRO layer can improve both material reliability and device electrical performance.

The EPR spectra of the SRO samples used in this study are collected in Fig. 8. As the silicon content increases from SRO1 to SRO5, the type of dominant defect species present in the oxides also changes. For SRO1, SRO2, and SRO3, a peak with a g-factor equal to 2.0025 is clearly seen. This corresponds to the characteristic spin of E' centers ($\bullet Si{\equiv}O_3$), which are the dominant defect species in silicon oxide. For SRO4 and SRO5, however, the E' centers disappear and a new peak of g-factor 2.0065 emerges. This coincides with the peak of a-Si spin centers ($\bullet Si{\equiv}Si_3$) identified by Kamigaki et al.[24] This new peak can be attributed to the existence of Si microcrystals generated during the deposition. Overall, as the O/Si ratio reduces from the stoichiometric value of 2.0 down to 1.28 for the silicon-rich SRO5, the dominant defect spin centers change from the E' centers to a-Si spin centers, as extra silicon atoms are incorporated into the oxide network. In fact, the oxide in this case can be perceived as a mixture consisting of two phases: the oxide plus the Si microcrystals.[25] The former contains E' centers as the dominant traps, while the latter comprises the a-Si centers as the major defect. Since the $\bullet Si{\equiv}Si_3$ defects are found to be more effective hydrogen traps than $\bullet Si{\equiv}O_3$, according to one previous experimental study,[24] the SRO5 oxide, when incorporated as a passivation layer, would be more efficient in trapping the mobile ions released from the nitride on the top, protecting the active device below. The trapping mechanisms in the SRO containing the a-Si centers are shown schematically in Fig. 9.

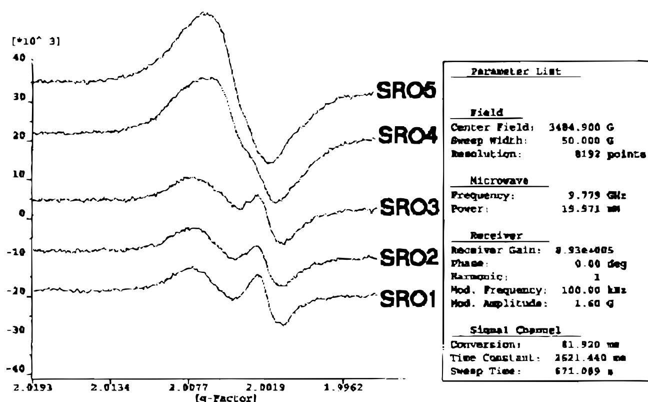


Figure 8. EPR spectra of SRO. The figure shows the increase in electron spin density and shift in g-factor, as Si content increases from SRO1 to SRO5.

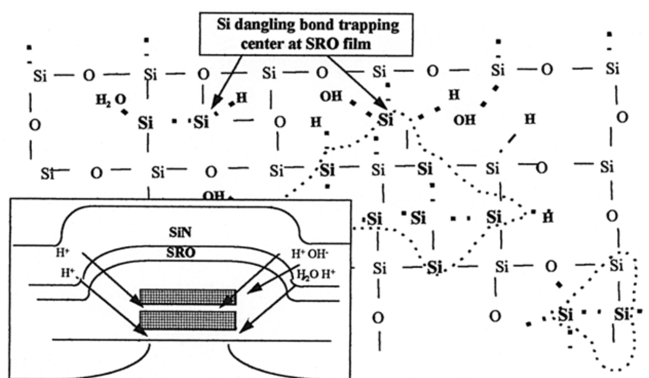


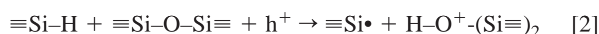
Figure 9. The hydrogen and moisture trapping mechanisms of silicon-rich oxides containing E' centers ($\bullet Si{\equiv}O_3$) and a-Si centers ($\bullet Si{\equiv}Si_3$). The areas enclosed by the dotted lines represent the a-Si microcrystals.

Once the moisture and hydrogen radicals reach the vicinity of the gate oxide-Si interface, defect reactions occur to generate interfacial carrier traps. Several possible reactions can take place. For example, H-atoms transported to the $Si\text{-}SiO_2$ interface can extract H-atoms from Si–H bonding sites thereby creating a dangling bond that acts as an interfacial trap

$$\equiv Si\text{–}H + H \rightarrow \equiv Si\bullet + H_2 \quad [1]$$

where $\equiv Si\bullet$ denotes a Si dangling bond. The driving force for reaction 1 is the large difference between the bond energies of Si–H, 3.4 eV, and H–H, 4.5 eV. The Si–H bond that is attacked can be at the interface having at least one Si-atom neighbor, or in the oxide having three O-atom neighbors. Since the density of interfacial traps depends on the concentrations of all reagents in reaction 1 and, hence, on the supply of H-atoms, the reaction rate may be directly associated with the diffusion rate of H-atoms. There has been experimental data suggesting that reaction 1 does indeed occur.[26]

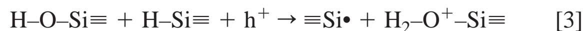
Alternative interfacial trap generating reaction may proceed as follows



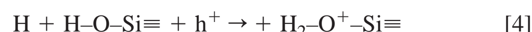
$$\equiv Si\text{–}H + \equiv Si\text{–}O\text{–}Si\equiv + h^+ \rightarrow \equiv Si\bullet + H\text{–}O^+\text{-}(Si\equiv)_2 \quad [2]$$

In this reaction, the $\equiv Si\text{–}H$ radicals can be formed, for example, by the transport of H-atoms from the passivation nitrides into the interface. The injection of holes (h^+) into the interface shifts the reaction to the right and generates Si dangling bonds ($\equiv Si\bullet$) which trap more holes, leading to a perpetuating reaction and accelerating failure. Unlike in reaction 1, the H-atom motion in reaction 2 is displacive rather than diffusive so that its reaction rate may be related to the structure and defect concentration at the interface. Again, reaction 2 has been experimentally verified.[26]

Lucovsky et al.[27] proposed two interfacial defect reactions with hydroxyl groups involved. These can be the probable failure mechanisms for moisture-related hot-carrier degradation



$$H\text{–}O\text{–}Si\equiv + H\text{–}Si\equiv + h^+ \rightarrow \equiv Si\bullet + H_2\text{–}O^+\text{–}Si\equiv \quad [3]$$



$$H + H\text{–}O\text{–}Si\equiv + h^+ \rightarrow + H_2\text{–}O^+\text{–}Si\equiv \quad [4]$$

In the above scenarios, the hydroxyl groups can be converted to charged defects; i.e., Si dangling bonds and O_3^+ in reaction 3, and O_3^+ in reaction 4. Like reaction 2, reactions 3 and 4 are self-generating by hole trapping mechanism. Reaction 4 involves both OH groups and H-atoms and can, thus, be perceived as the mechanism in case both the species combined to initiate the carrier trapping events. The supply of hydroxyl groups at the interface can be replenished by the indiffusion of moisture from passivation layers, as discussed previously.

Note that the trapping reactions of the oxide as discussed above can be viewed as the reversal of reactions 1, 2, and 3, occurring in the oxide passivation layer. In this case, the dangling bond $\equiv Si\bullet$ would be either the E' centers or a-Si spin centers.

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In this study, the role of BPSG ILD layer on device performance is not yet investigated. The high moisture permeation of this layer may have provided easy access for water diffusion from the top. In a recent study, Shuto et al.[11] proposed a mechanism that, during annealing, the moisture in BPSG may diffuse inward to the active device region and cause failure, if a nitride with high moisture resistance was laid on the top. In that case, the effects of hydrogen release from nitride is overwhelmed by the moisture diffusion from BPSG. However, in this study, a high temperature (850°C) BPSG flow process is performed following the BPSG deposition process. Further study is required to clarify this point.

Overall, process integration of passivation, IMD, and ILD layers is a potentially important issue for building memory devices reliability. Thin film characteristics should be modified in order to be compatible with subsequent processes so that they can meet the final device performance goal. For example, the similar oxide-nitride scheme used in this study can be applied to the implementation of shallow trench isolation through CMP. In this case, fine tuning the film characteristics in order to achieve an appropriate polish selectivity, while maintaining device hot carrier resistance would be an important task. Further work is in progress to pursue this issue.

Conclusions

Suppression of hot carrier degradation and increase in polyload resistance for cache memory devices can be fulfilled by fine-tuning the characteristics of oxide-nitride double layer passivation. Higher refractive index, higher density, lower etch rates and lower moisture content can be achieved for the oxides by incorporating more Si-H bonds into the structure. Meanwhile, high density, high compressive stress, and low hydrogen concentration can be fulfilled in the nitrides by adjusting the CVD gas chemistry. Water diffused from oxide and hydrogen released from nitride are both responsible for hot carrier drain current degradation and poly load resistance decrease. In addition to the E´ centers in the oxides, the presence of a-Si trap centers in silicon-rich oxide passivation layer are effective traps for hydrogen and other mobile ions, hence, providing a more thorough protection for the device against hot carrier degradation.

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