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Effective Improvement on Barrier Capability of Chemical Vapor Deposited WSi_x Using N_2 Plasma Treatment

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This work studies the thermal stability of $Cu/WSi_x/p^+$-n and $Cu/WSiN/WSi_x/p^+$-n diodes in which the WSi_x barrier layers were deposited by chemical vapor deposition to a thickness of about 50 nm using SiH_4/WF_6 chemistry with the SiH_4/WF_6 flow rates of 6/2 sccm, while the WSiN layers were formed by in situ N_2 plasma treatment on the chemically vapor deposited WSi_x (CVD-WSi_x) surfaces. Without N_2 plasma treatment, the thermal stability of Cu/WSi_x (50 nm)/p^+-n junction diodes was found to reach 500°C; with N_2 plasma treatment, the resultant $Cu/WSiN/WSi_x$ (50 nm)/p^+-n junction diodes were able to retain integrity of electrical characteristics up to at least 600°C. Failure mechanism of the $WSiN/WSi_x$ bilayer in the $Cu/WSiN/WSi_x/Si$ structure was closely related to the WSi_x/Si interface reaction and the tungsten silicide formation of the WSi_x layer. Thus, barrier capability of the $WSiN/WSi_x$ bilayer can be further improved by suppressing the WSi_x/Si interface reaction and the silicidation of the WSi_x layer. The thermal stability of Cu/barrier/p^+-n diodes was further raised to 650°C by using a multilayer barrier structure of $WSiN/WSi_x$ (50 nm)/$WSiN/WSi_x$ (10 nm) or a $WSiN/WSi_y$ ($y > 1$) barrier. We conclude that the post-CVD-WSi_x treatment with in situ N_2 plasma is a simple, practical, and efficient method of improving the WSi_x-based barrier capability for Cu metallization.
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Copper (Cu) has been extensively studied as a potential interconnect material for deep submicron integrated circuit (IC) applications because of its low electrical resistivity and superior electromigration resistance as compared with the conventionally used Al and its alloys.[1-3] Moreover, Cu can be deposited using chemical vapor deposition (CVD).[4,5] Unfortunately, Cu diffuses fast in Si and forms Cu–Si compounds at low temperatures (about 200°C).[6] It causes deep-level traps in Si.[7] In addition, it has poor adhesion to interlevel dielectric and drifts through oxide under field acceleration.[8] Therefore, the use of a diffusion barrier between Cu and its underlying layers is considered a prerequisite for Cu to be useful in silicon IC applications.

Various materials have been studied as diffusion barriers between Cu and Si substrates as well as Cu and dielectric layers. Refractory metals are generally regarded as potential barrier materials because of their high thermal stability and good electrical conductivity.[9-13] Sputter-deposited, nitride-based diffusion barriers, such as WN, [10,14-16] TaN, [15,17-20] MoN, [21] and TiWN, [22] have attracted extensive attention for a long time. Most recently, the use of a WSiN layer as a diffusion barrier has also been intensively studied.[23-27] It was reported that the WSiN film has low film stress, low electrical resistivity, excellent thermal stability, good adhesion to insulator and copper films, and a well-matched thermal expansion coefficient with Si.[24,28] It was also reported that a very thin (4 nm) WSiN layer can be formed on the surface of WSi_x by electron cyclotron resonance (ECR) N_2 plasma nitridation and that it functioned as an excellent barrier to dopant diffusion.[29] Moreover, it was found that a uniform ultrathin (<1 nm) WSiN barrier layer can be formed at the interface of WN/poly-Si by thermal annealing and that the WSiN layer was able to suppress the silicidation reaction between W and poly-Si up to 800°C.[30] Although these studies have provided much valuable information regarding WSiN films as a diffusion barrier, no study has been made on the WSiN layer with respect to its barrier effectiveness between Cu and Si substrates using electrical measurement as well as material analysis.

In this study, we use the $WSiN/WSi_x$ bilayer as a diffusion barrier between Cu and Si substrates in which the WSi_x layer was deposited by CVD using the SiH_4/WF_6 chemistry, while the WSiN layer was formed by an in situ N_2 plasma treatment on the WSi_x surface. According to this scheme, a very thin WSiN (about 5 nm) layer was formed on the surface of the WSi_x layer. We found that the $WSiN/WSi_x$ bilayer possesses a much improved barrier capability against Cu diffusion.

Experimental

The thermal stability of barrier layers was evaluated by measuring leakage current of thermally annealed Cu/barrier/p^+-n junction diode. The starting materials for the diodes fabrication were n-type, (100)-oriented silicon wafers with 4–7 Ω cm nominal resistivity. After RCA standard cleaning, the wafers were thermally oxidized to grow a 500 nm thick oxide layer. Diffusion areas with sizes of 500 × 500 and 1000 × 1000 μm were defined on the oxide-covered wafers using conventional photolithographic technique. The p^+-n junctions with junction depth of 0.3 μm were formed by BF_2^+ implantation at 40 keV to a dose of 3×10^{15} cm^{-2} followed by furnace annealing at 900°C for 30 min in N_2 ambient.

After the junctions were formed, the wafers were divided into five groups for the preparation of the following devices: (a) Cu/p^+-n; (b) Cu/WSi_x (50 nm)/p^+-n; (c) $Cu/WSiN/WSi_x$ (50 nm)/p^+-n; (d) Cu/WSiN/WSi*y* ($y > 1$)/p^+-n; and (e) $Cu/WSiN/WSi_x$ (50 nm)/WSiN/WSi_x (10 nm)/p^+-n junction diodes. Schematic cross sections of the former four differently metallized p^+-n junction diodes are illustrated in Fig. 1. The WSi_x layer was deposited by CVD to a thickness of about 50 nm using the SiH_4/WF_6 chemistry. The subsequent thermal annealing of the WSi_x/Si sample occurred at 700°C for 30 min in N_2 ambient so that the WSi_x layer became a Si-rich WSi*y* ($y > 1$) layer. The $WSiN/WSi_x$ and $WSiN/WSi_y$ barrier bilayers were formed by N_2 plasma treatment on the surface of WSi_x and WSi_2 layers, respectively. The last barrier of the $WSiN/WSi_x/WSiN/WSi_x$ multilayer was accomplished by a double-step processing of WSi_x deposition and N_2 plasma treatment: a 10 nm WSi_x deposition followed by N_2 plasma treatment plus another 50 nm WSi_x deposition followed by N_2 plasma treatment. Figure 2 shows the process flow for the $Cu/WSiN/WSi_x$ (50 nm)/$WSiN/WSi_x$ (10 nm)/p^+-n junction diode.

Prior to the WSi_x deposition, the wafers were dipped in dilute HF (50:1) for 30 s, followed by a rinse in DI water for 5 min and a spin dry. The wafers were then loaded into a load-locked coldwall CVD system within 5 min and transferred by a robot arm to the deposition chamber without exposure to the atmosphere. The base pressure of the CVD chamber was 1×10^{-6} Torr. In this study, the CVD-WSi_x was deposited with the following conditions: substrate temperature 250°C, total gas pressure 12 mTorr, WF_6 flow rate 2 sccm, and SiH_4 flow rate 6 sccm. For the formation of WSiN, a very thin (about

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5 nm) layer of WSiN was formed by in situ N_2 plasma treatment on the surface of the WSi_x layer without exposure to the air, or by N_2 plasma treatment on the surface of the WSi_y ($y > 1$) layer with air exposure. The N_2 plasma treatment was performed at 100 W plasma power with N_2 flow rate of 80 sccm and a gas pressure of 25 mTorr; the plasma treating time was 300 s.

Finally, Cu metallization was applied to all samples using a dc magnetron sputtering system with a base pressure of 1–2 $\times$ 10^{-6} Torr and with no intentional substrate heating and bias. A 200 nm thick Cu film was sputter deposited using a 99.999% purity Cu target in Ar ambient at a pressure of 7.6 mTorr. Cu patterns were defined and etched using dilute (5 vol %) HNO_3, while the barrier layers were etched using SF_6/N_2 plasma. For comparison, Cu/p^+-n junction diodes without barrier layers were also fabricated.

To investigate thermal stability of the diodes, samples were thermally annealed in an N_2 flowing furnace for 30 min at various temperatures from 200 to 800°C. Reverse-bias leakage-current measurement on the thermally annealed diodes was used to evaluate the barrier capability of various barrier layers. An HP-4145B semiconductor parameters analyzer was used for the measurement, and at least 30 diodes were measured in each case. Unpatterned samples with multilayer structures of Cu/WSi_x (50 nm)/Si, Cu/WSiN/WSi_x (50 nm)/Si, and Cu/WSiN/WSi_x (50 nm)/SiO_2/Si were also prepared for material analysis. Sheet resistance of the multilayer structures was measured using a four-point probe. Auger electron spectroscopy (AES) was used to determine the composition of WSi_x films. X-ray diffraction (XRD) analysis was used for phase identification. Scanning electron microscopy (SEM) was employed to observe surface

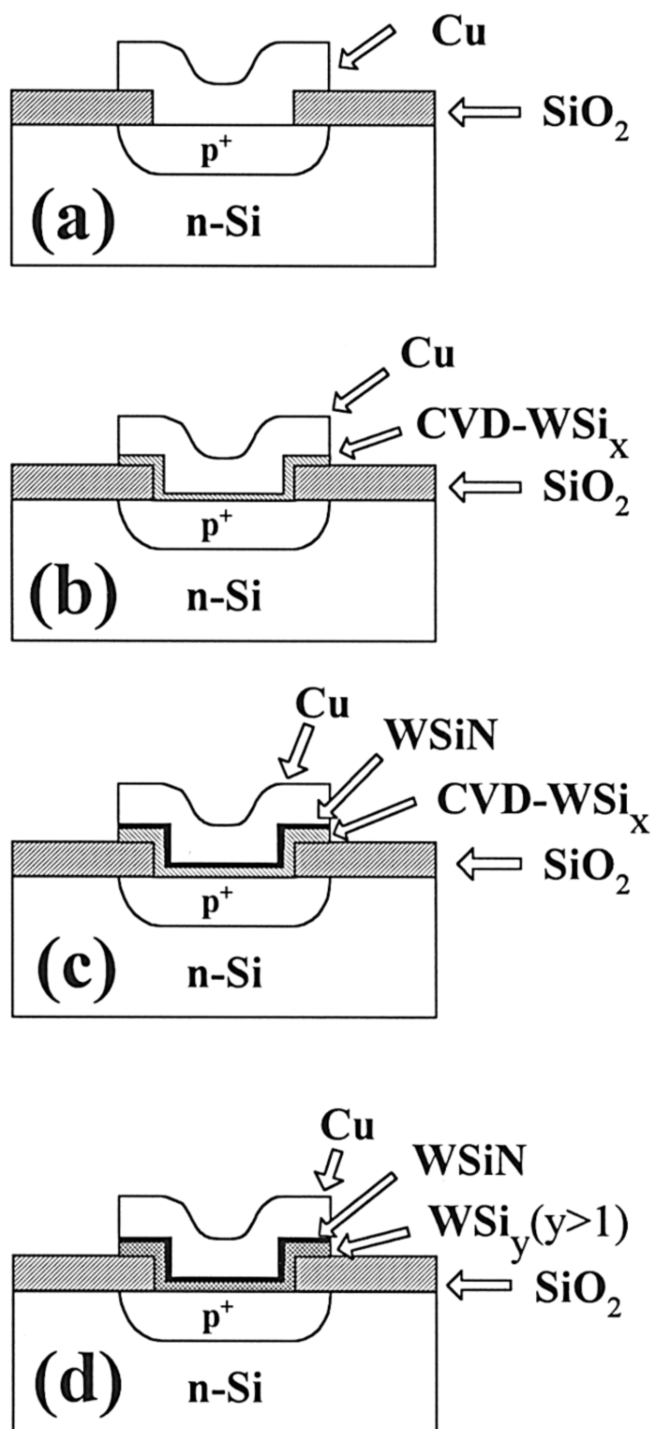

Figure 1. Schematic cross sections of (a) Cu/p^+-n; (b) Cu/WSi_x (50 nm)/p^+-n; (c) Cu/WSiN/WSi_x (50 nm)/p^+-n; and (d) Cu/WSiN/WSi_y ($y > 1$)/ p^+-n junction diodes.

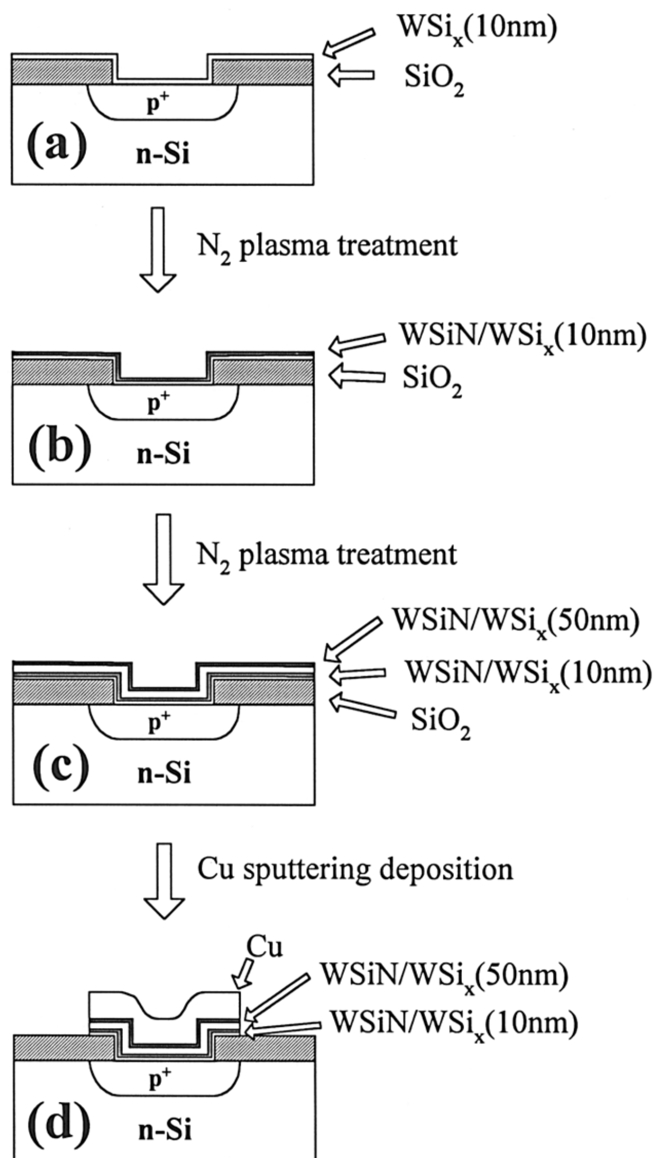

Figure 2. Process flow of Cu/WSiN/WSi_x (50 nm)/WSiN/WSi_x (10 nm)/p^+-n junction diodes: (a) WSi_x (10 nm) deposition, (b) in situ N_2 plasma treatment, (c) second layer of WSi_x (50 nm) deposition and in situ N_2 plasma treatment, and (d) Cu deposition and patterning.

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morphology and microstructure, and secondary ion mass spectroscopy (SIMS) was used to determine the elemental depth profiles.

Results and Discussion

Thermal stability of WSi_x (50 nm) and WSiN/WSi_x (50 nm) barriers.—Figure 3 shows the statistical distributions of reverse bias leakage-current density for the Cu/p^+-n, Cu/WSi_x (50 nm)/p^+-n, and Cu/WSiN/WSi_x (50 nm)/p^+-n junction diodes annealed at various temperatures. For the diodes without any barrier layer between the Cu and Si substrate, the Cu/p^+-n junction diodes failed after 200°C annealing (Fig. 3a). With a 50 nm thick WSi_x barrier between the Cu and Si substrate, the Cu/WSi_x/p^+-n junction diodes were able to retain the devices integrity up to 500°C (Fig. 3b). For the diodes with an N_2-plasma-treated barrier layer, the Cu/WSiN/WSi_x/p^+-n diodes were able to remain stable after annealing at temperatures up to 600°C (Fig. 3c). Even after annealing at 650°C, about 85% of the annealed diodes survived with leakage current density less than 100 nA/cm^2. It is clear that the barrier capability of the WSi_x layer was significantly improved by in situ N_2 plasma treatment.

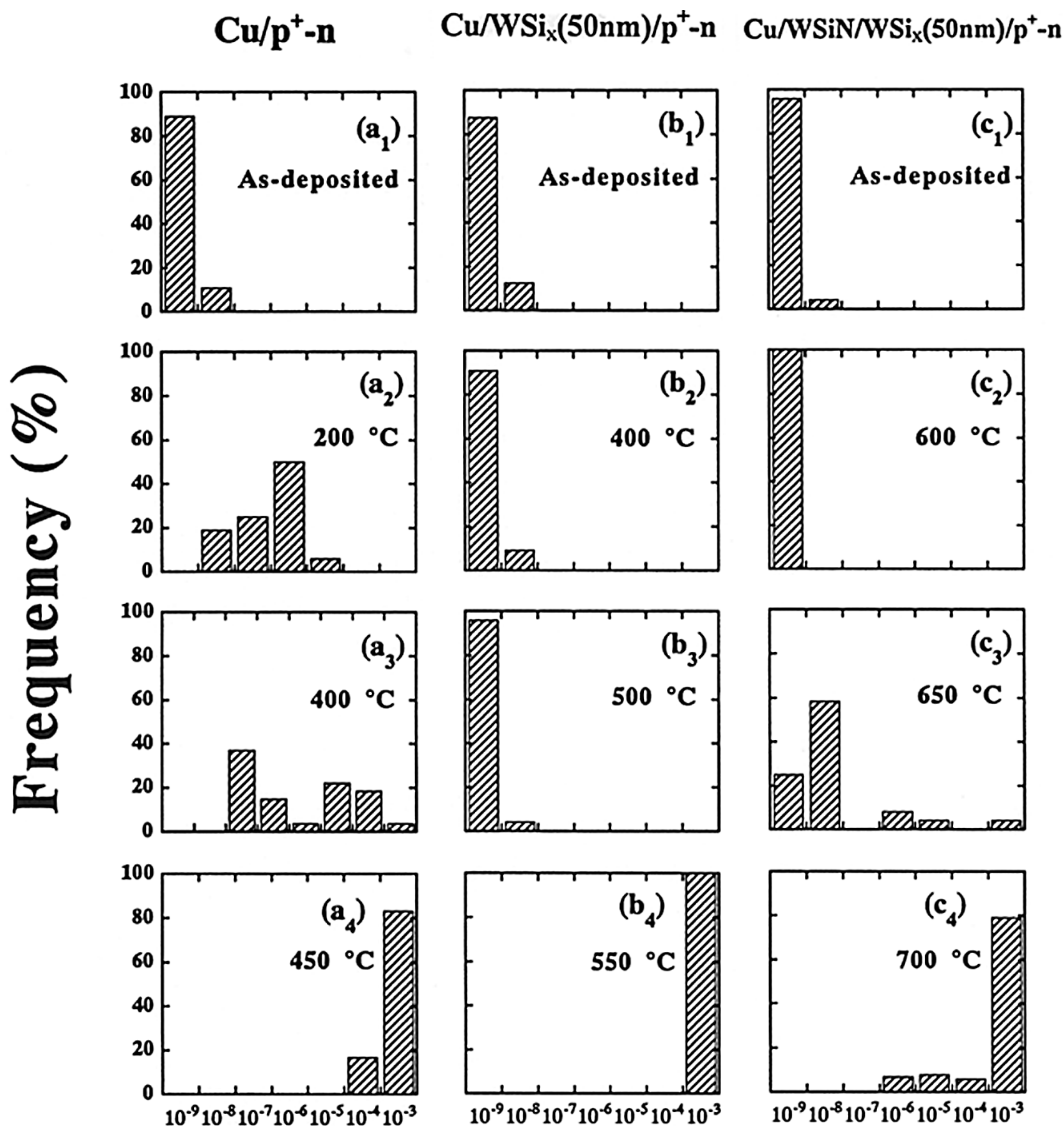

Figure 3. Histograms showing statistical distributions of reverse-bias leakage-current density for (a) Cu/p^+-n, (b) Cu/WSi_x (50 nm)/p^+-n, and (c) Cu/WSiN/ WSi_x (50 nm)/p^+-n junction diodes annealed at various temperatures.

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The significant improvement of barrier capability for the N_2-plasma-treated WSi_x layer is attributed to a very thin WSiN layer formed on the WSi_x surface, as confirmed by AES depth profile analysis shown in Fig. 4. Without N_2 plasma treatment, only a very weak signal of nitrogen was detected near the WSi_x surface (Fig. 4a), presumably due to adsorption of nitrogen gas on the WSi_x surface prior to loading the test sample into the AES chamber. After an N_2 plasma treatment at 100 W for 300 s, a very thin (about 5 nm) WSiN layer was definitely formed (Fig. 4b). The N/W ratios in the WSiN layer were determined to be about 3/2 at the sample's surface and about 1/1 at 3 nm depth from the sample's surface. In addition, the as-deposited WSi_x layer has a Si/W atomic ratio of about unity, as determined by Rutherford backscattering (RBS) measurement.

Figure 5 shows the SIMS depth profiles for the as-deposited and 600°C-annealed Cu/WSi_x/Si and Cu/WSiN/WSi_x/Si samples. With the WSi_x barrier without N_2 plasma treatment, the interdiffusion among Cu, W, and Si resulted in severe degradation of the Cu/WSi_x/Si structure after annealing at 600°C, as shown in Fig. 5b (compared with Fig. 5a for the as-deposited sample). On the other hand, with the barrier layer treated with N_2 plasma, the Cu/WSiN/WSi_x/Si sample was able to keep the W and Si profiles nearly unchanged, with only a slight diffusion of Cu into the barrier layer, as shown in Fig. 5d (compared with Fig. 5c). The results of SIMS depth profile analysis further confirm that thermal stability of the Cu/WSi_x/Si structure can be improved effectively by forming a very thin layer of the WSiN on the surface of the WSi_x layer via N_2 plasma treatment.

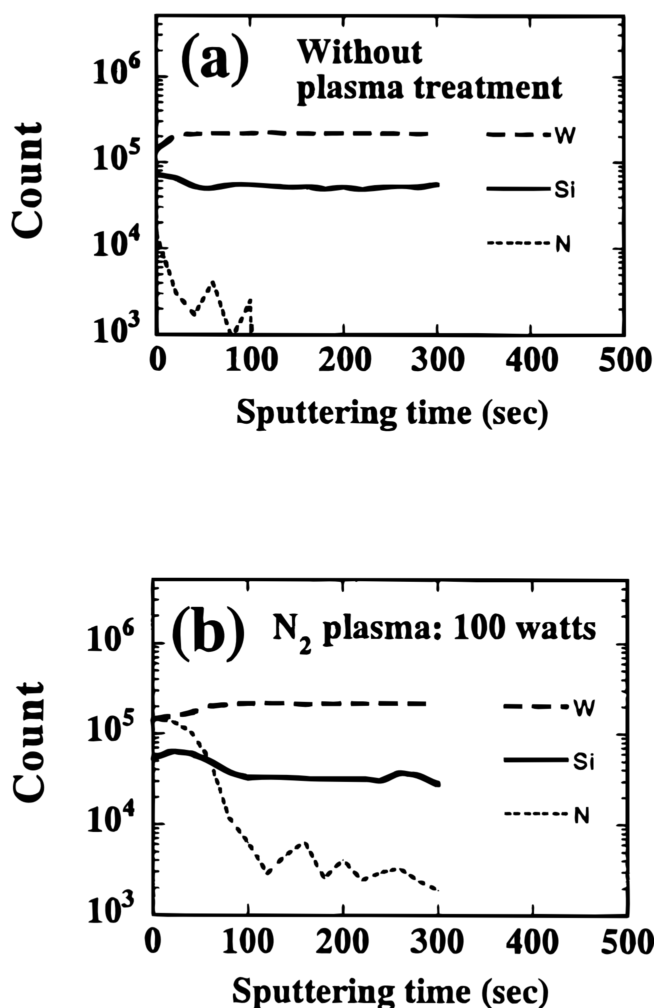

Figure 4. AES depth profiles of as-deposited WSi_x/Si samples (a) without N_2 plasma treatment and (b) with N_2 plasma treatment at 100 W for 300 s.

The sheet resistance change of thermally annealed samples, normalized to the as-deposited sheet resistance value, is denoted as $\Delta Rs/Rs$ percent and defined as follows

$$\frac{\Delta Rs}{Rs}\% = \frac{Rs_{\text{after anneal}} - Rs_{\text{as-deposited}}}{Rs_{\text{as-deposited}}} \times 100\%$$

Figure 6 shows the percentage change of sheet resistance vs. annealing temperature for the samples of Cu/WSi_x (50 nm)/Si, Cu/WSiN/WSi_x (50 nm)/Si, and Cu/WSiN/WSi_x (50 nm)/SiO_2/Si. For the Cu/WSi_x/Si sample, the sheet resistance remained constant up to 550°C; it increased drastically after annealing at 600°C. For the samples with a barrier layer treated with N_2 plasma, the sheet resistance of Cu/WSiN/WSi_x/Si samples remained stable up to 650°C, and only a slight degradation was observed after annealing at 700°C. This is a significant improvement of barrier effectiveness. Compared with the results of leakage-current measurement shown in Fig. 3, we found that the electrical measurement is a much more sensitive technique for barrier failure detection. Nevertheless, the results of sheet resistance measurement further confirm that thermal stability of the Cu/WSi_x/Si structure can be significantly improved by forming a thin layer of WSiN on the surface of the WSi_x layer via N_2 plasma treatment.

Failure mechanism of WSiN/WSi_x (50 nm) barriers.—There are two interfaces, Cu/WSi_x and WSi_x/Si, in the Cu/WSi_x/Si structure. Barrier effectiveness of the WSi_x layer can be retained up to a certain temperature only if these two interfaces and the WSi_x layer itself are thermally stable up to that temperature.[9] Our previous findings revealed that thermal stability of the Cu/WSi_x interface can be improved by inserting a WSiN layer between Cu and WSi_x. However, reaction at the WSi_x/Si interface might affect thermal stability of the Cu/WSiN/WSi_x/Si structure. To investigate the effect of the WSi_x/Si interface reaction on the thermal stability of the Cu/WSiN/WSi_x/Si structure, we examined the thermal stability of the Cu/WSiN/WSi_x/SiO_2/Si structure. The presence of the SiO_2 layer in this structure prevented interdiffusion between WSi_x and the substrate Si at elevated temperatures. We found no obvious change in sheet resistance for the Cu/WSiN/WSi_x/SiO_2/Si sample after annealing at temperatures up to 750°C (Fig. 6). This indicates that the degradation in the electrical characteristics of Cu/WSiN/WSi_x/p^+-n junction diodes was due to the reaction that occurred at the WSi_x/Si interface at 700°C, as was confirmed further by XRD analysis shown in Fig. 7. This result also suggests that thermal stability of the Cu/WSiN/WSi_x/p^+-n diodes could be further improved if a scheme can be developed to suppress or retard the WSi_x/Si interface reaction at elevated temperatures.

Figure 7 illustrates the XRD spectra for the as-deposited and thermally annealed Cu/WSi_x/Si, Cu/WSiN/WSi_x/Si, and Cu/WSiN/WSi_x/SiO_2/Si samples. The formation of Cu_3Si, W_5Si_3, and/or WSi_2 phases for the Cu/WSi_x/Si sample annealed at 600°C and above, as shown in Fig. 7a, resulted in drastic increase in sheet resistance. Similarly, the increase in sheet resistance for the Cu/WSiN/WSi_x/Si sample after annealing at 700°C reflects the formation of both Cu_3Si and WSi_2 phases, as shown in Fig. 7b; in fact, weak peaks of WSi_2 already appeared when the sample was annealed at 650°C. It should be noted that no diffraction peak relating to the formation of WSi_2 was detected for the Cu/WSiN/WSi_x/Si sample annealed at 600°C (Fig. 7b), while a strong peak of copper silicide and weaker peaks of tungsten silicides were detected for the Cu/WSi_x/Si sample annealed at the same temperature (Fig. 7a). It has been reported that the amorphous state of WSiN can be preserved even after annealing at 850°C.[29] For the Cu/WSiN/WSi_x/Si sample, the thin but chemically and thermally stable WSiN layer contributed to retard the diffusion of copper; thus, the barrier effectiveness was improved. For the Cu/WSiN/WSi_x/Si sample annealed at 650°C, although weak diffraction peaks of WSi_2 appeared, no signal relating to Cu_3Si phase was detected. This indicates that Cu diffusion remained suppressed by the WSiN layer, though interface reaction at the WSi_x/Si interface had occurred. However, annealing at 700°C resulted in silicidation

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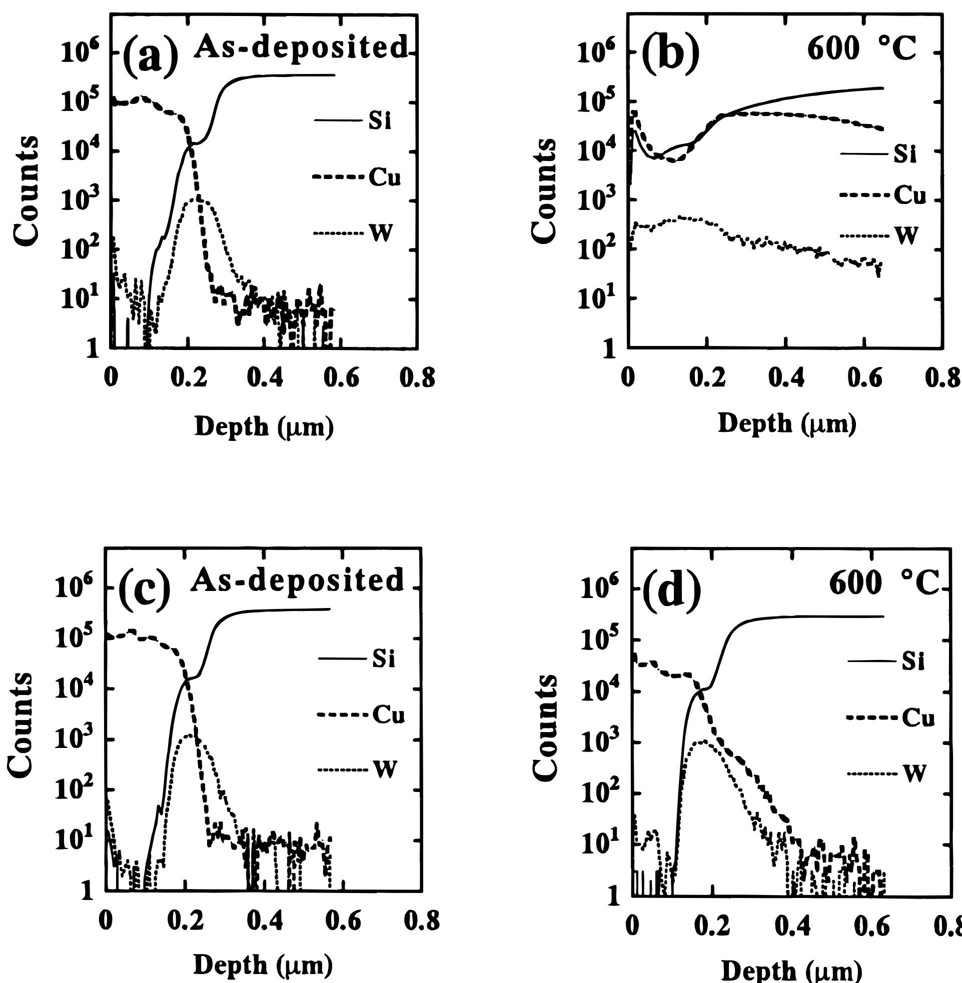

Figure 5. SIMS depth profiles: (a) as-deposited and (b) 600°C annealed Cu/WSi_x/Si samples; and (c) as-deposited and (d) 600°C annealed Cu/WSiN/ WSi_x/Si samples.

and grain growth of the WSi_x layer, leading to a net volume change and localized defect formation (such as columnar seams and stress-induced microcracks), which in turn broke the continuity of the WSiN layer. Thus, barrier capability of the WSiN/WSi_x bilayer was degraded. As for the structure of the Cu/WSiN/WSi_x/SiO_2/Si, the diffraction peak of copper silicide was not detected after annealing at temperatures up to 750°C, though weak peaks relating to W_5Si_3 phase were found (Fig. 7c). This implies that the reaction occurring at the WSi_x/Si interface played an important role in the failure of the Cu/WSiN/WSi_x/Si structure. Comparative results of thermal stability for the multilayer structures studied in this work based on XRD analysis are summarized in Table I.

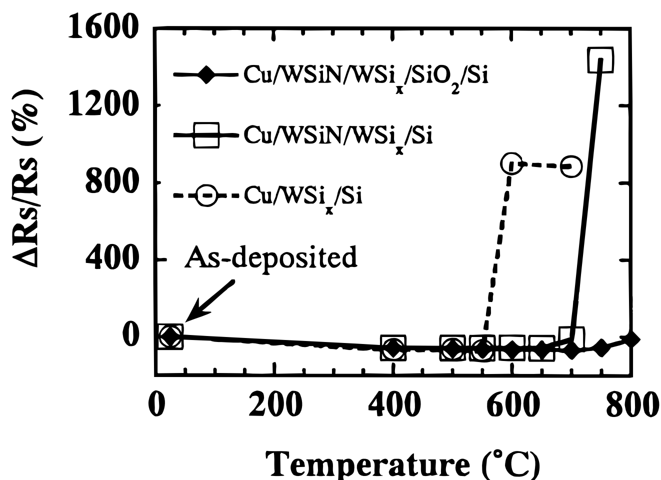

Figure 6. Percentage change of sheet resistance vs. annealing temperature for the samples of Cu/WSi_x/Si, Cu/WSiN/WSi_x/Si, and Cu/WSiN/WSi_x/SiO_2/Si.

Figure 8 shows the SEM micrographs for the Cu/WSi_x (50 nm)/p^+-n junction diodes. The barrier structure remained unchanged after annealing at 500°C (Fig. 8b); however, large Cu_3Si precipitates (silicide) were formed after annealing at 600°C (Fig. 8c). For the Cu/WSiN/WSi_x (50 nm)/p^+-n diode structure, SEM micrographs show that this multilayer structure remained stable after annealing at 600°C, as shown in Fig. 9. After annealing at 650°C, some of the diodes showed degradation while the others remained intact (Fig. 3c). For the diodes that remained intact after annealing, the SEM micrograph shows that integrity of the barrier structure was retained (Fig. 9c). For the degraded diodes, highly localized protrusions were found (Fig. 9d). Thus, failure of the WSiN/WSi_x (50 nm) bilayer barrier is likely associated with these highly localized protrusions, which were presumably caused by diffusion of Cu through the localized weak points (such as grain boundaries, columnar seams, and stress-induced microcracks) in the barrier layer. These highly localized defects also reveal a common feature of a protrusion at their center, surrounded by a ring of Cu film depletion. After annealing at 700°C, defects were found with larger size as well as higher density (not shown).

Further improvement of barrier capability.—To further improve barrier capability of the WSiN/WSi_x bilayer, two schemes were designed to either eliminate reaction at the WSi_x/Si interface or suppress interdiffusion between WSi_x and Si substrate. According to these schemes, we proposed the following two barrier structures.

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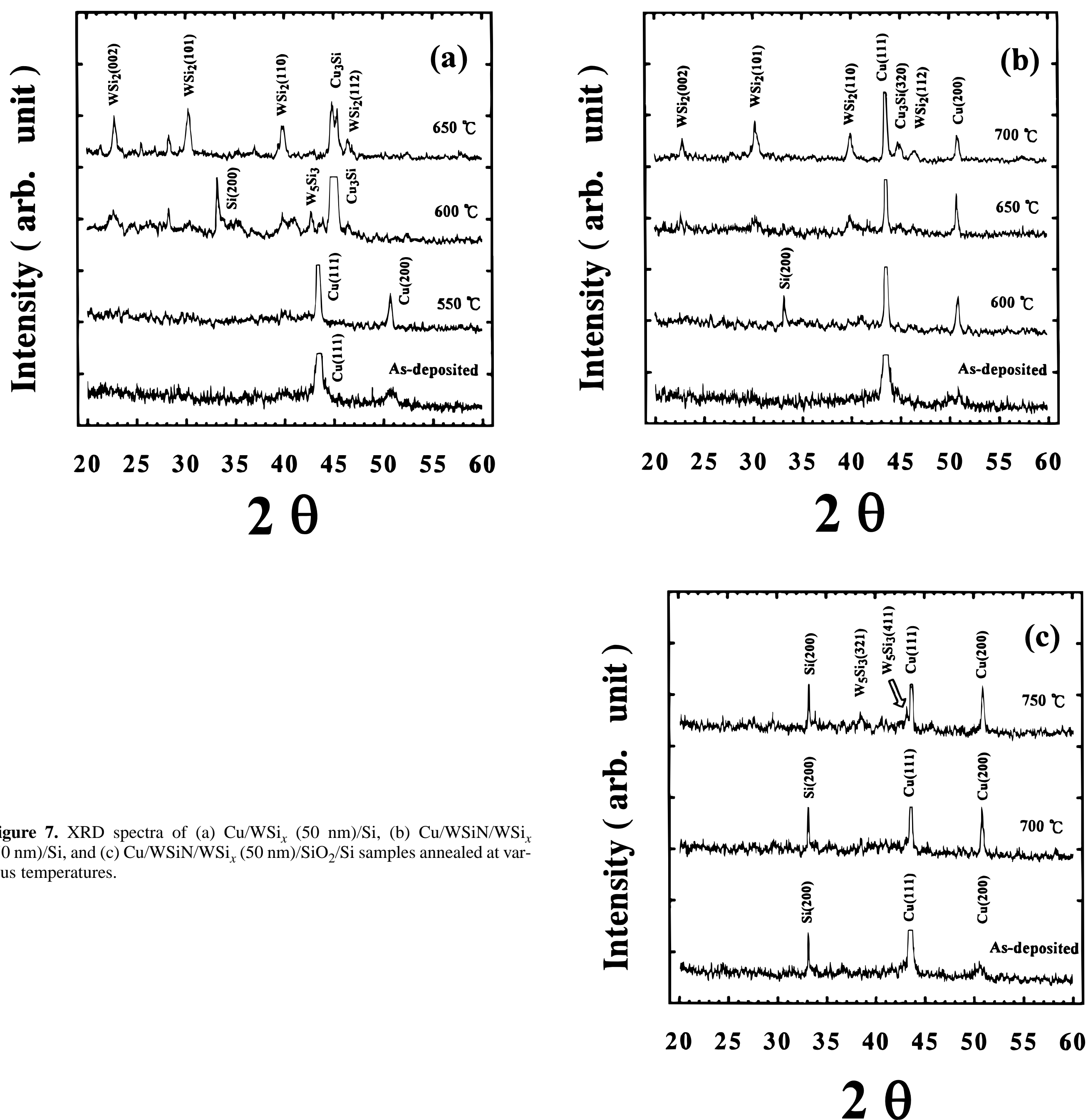

Figure 7. XRD spectra of (a) Cu/WSi$_x$ (50 nm)/Si, (b) Cu/WSiN/WSi$_x$ (50 nm)/Si, and (c) Cu/WSiN/WSi$_x$ (50 nm)/SiO$_2$/Si samples annealed at various temperatures.

First, we annealed the WSi$_x$ layer to stabilize the barrier structure, followed by N$_2$ plasma treatment prior to Cu metallization to make a Cu/WSiN/WSi$_y$ ($y > 1$)/p$^+$-n junction diode. Second, we inserted an extra thin WSiN/WSi$_x$ (10 nm) bilayer between the original WSi$_x$

Table I. Compound phases detected by XRD analysis for various multilayer structures studied in this work.[a]

Annelaing temperatures	Multilayer structure		
	Cu/WSi$_x$/Si	Cu/WSiN/WSi$_x$/Si	Cu/WSiN/WSi$_x$/SiO$_2$/Si
550°C	×	×	×
600°C	Weak WSi$_2$, W$_5$Si$_3$, Cu$_3$Si	×	×
650°C	WSi$_2$, Cu$_3$Si	Weak WSi$_2$	×
700°C	*WSi$_2$, Cu$_3$Si	WSi$_2$, weak Cu$_3$Si	×
750°C		*WSi$_2$, Cu$_3$Si	W$_5$Si$_3$

[a] × indicates no observation of compound phase; * indicates XRD spectra not shown in Fig. 7.

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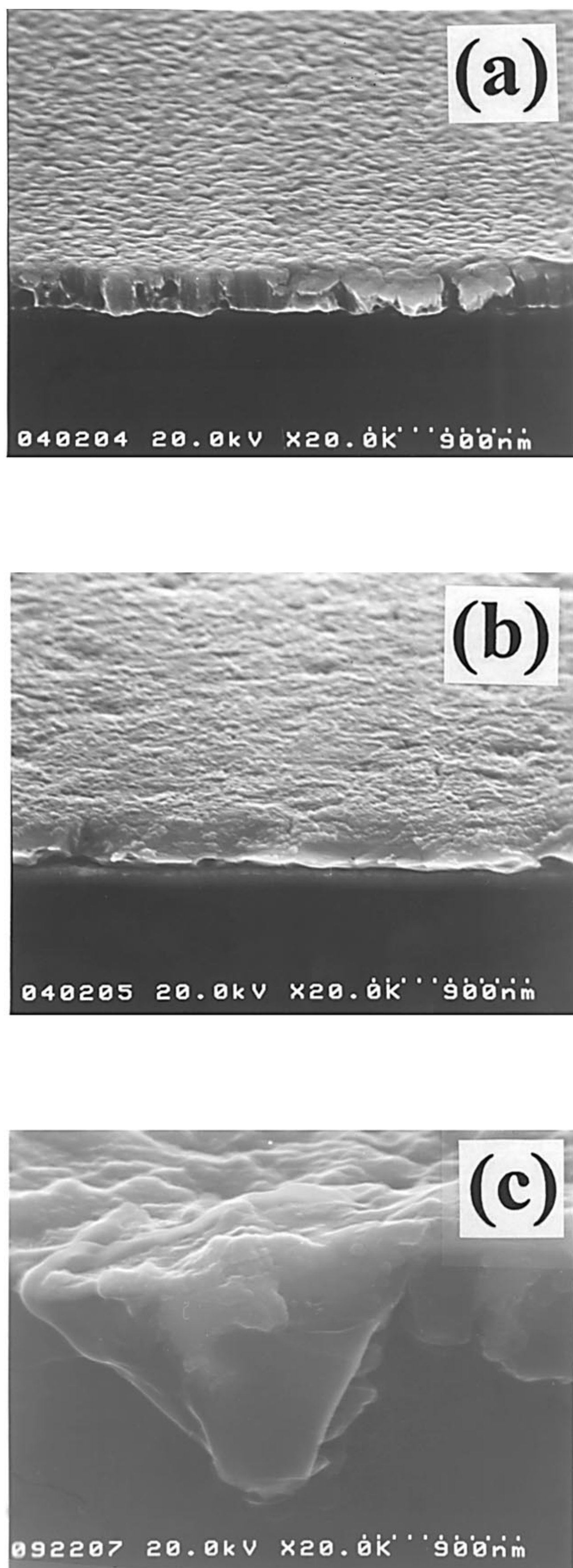

Figure 8. SEM micrographs for the Cu/WSi_x (50 nm)/p^+-n junction diodes (a) as-deposited (oblique view), (b) annealed at 500°C (oblique view), and (c) annealed at 600°C (cross-sectional view).

(50 nm) layer and Si substrate to make a Cu/WSiN/WSi_x (50 nm)/WSiN/WSi_x (10 nm)/p^+-n junction diode so as to suppress interdiffusion between the 50 nm WSi_x and Si substrate.

Cu/WSiN/WSi_y (y > 1)/p^+-n junction diodes.—We thermally annealed the WSi_x (50 nm)/p^+-n junction diodes at 700°C in N_2 ambient for 30 min so that the WSi_x layer became a Si-rich WSi_y (y > 1) layer. After the formation of the Si-rich WSi_y layer, N_2 plasma treatment was performed on the Si-rich WSi_y surface to produce a WSiN/WSi_y bilayer. Figure 10 shows the statistical distributions of reverse-bias leakage-current density for the Cu/WSiN/WSi_y/p^+-n junction diodes annealed at various temperatures. All junction diodes retained the integrity of their electrical characteristics up to 600°C. After annealing at 650°C, they were slightly degraded; however, even after annealing at 700°C, about 60% of the diodes survived with leakage current density less than 100 nA/cm^2. Compared with the results of electrical measurement for the Cu/WSiN/WSi_x/p^+-n junction diodes shown in Fig. 3c, we found that the barrier capability of WSiN/WSi_y bilayer is superior to that of WSiN/WSi_x. This indicates that the annealing before nitridation stabilized the barrier structure, presumably due to the formation of Si-rich WSi_y, and thus efficiently improved the barrier capability.

Cu/WSiN/WSi_x (50 nm)/WSiN/WSi_x (10 nm)/p^+-n junction diodes.—We found that the Cu/WSiN/WSi_x (50 nm)/p^+-n junction diodes degraded after annealing at 650°C (Fig. 3c). It is possible that Si out-diffusion took place at the WSi_x/Si interface at such a temperature. Presumably, the Si out-diffusion together with formation and grain growth of tungsten silicide (as confirmed by XRD analysis shown in Fig. 7b) generated local defects and thus led to degradation of the diodes electrical characteristics. To prevent the undesirable interdiffusion between WSi_x and Si, a thin WSiN/WSi_x (10 nm) bilayer was introduced between the WSiN/WSi_x (50 nm) bilayer and Si substrate to make a four-layer barrier structure of WSiN/WSi_x (50 nm)/WSiN/WSi_x (10 nm). Figure 11 shows the statistical distributions of reverse-bias leakage-current density for the Cu/WSiN/WSi_x/WSiN/WSi_x/p^+-n junction diodes annealed at various temperatures. The junction diodes retained their integrity after annealing at temperatures up to 650°C. This is an obvious improvement over the Cu/WSiN/WSi_x/p^+-n junction diodes. It appeared that the out-diffusion of Si substrate at WSi_x (50 nm)/Si interface was suppressed by the presence of WSiN/WSi_x (10 nm). The WSiN/WSi_x (10 nm) underlayer blocked the Si out-diffusion and thus retarded the formation of WSi_2 and suppressed the grain growth of the WSi_x (50 nm) layer, which in turn resulted in the improvement of junction diodes thermal stability. However, all the diodes were severely degraded after annealing at 700°C, presumably due to the crystallization and grain growth of the WSi_x (50 nm) layer. The reaction at the WSi_x (10 nm)/Si interface at such a high temperature was also responsible for the degradation of electrical characteristics.

Figure 12 shows the surface morphology of the Cu/WSiN/WSi_y (y > 1)/p^+-n junction diodes. No obvious defect was found on the diodes annealed at 650°C (Fig. 12b) as compared with the as-deposited sample (Fig. 12a). For the diodes annealed at 700°C, some of the diodes retained their integrity with very low leakage current while others were severely degraded (Fig. 10). A number of small openings were found on the diodes that have a low leakage-current density (not shown), while dense and large openings were found for the diodes with degraded electrical characteristics (Fig. 12c). Figure 13 shows SEM micrographs for the Cu/WSiN/WSi_x (50 nm)/WSiN/WSi_x (10 nm)/p^+-n junction diodes annealed at 650 and 700°C. No obvious defect was found on the diodes annealed at 650°C (Fig. 13a). This is consistent with the results of electrical measurement shown in Fig. 11. After annealing at 700°C, a highly localized trapezoidal section precipitate was found throughout our SEM inspection (Fig. 13b). Thermal stability temperatures of WSi_x-based barrier layers determined by various techniques of measurement or analysis are summarized in Table II.

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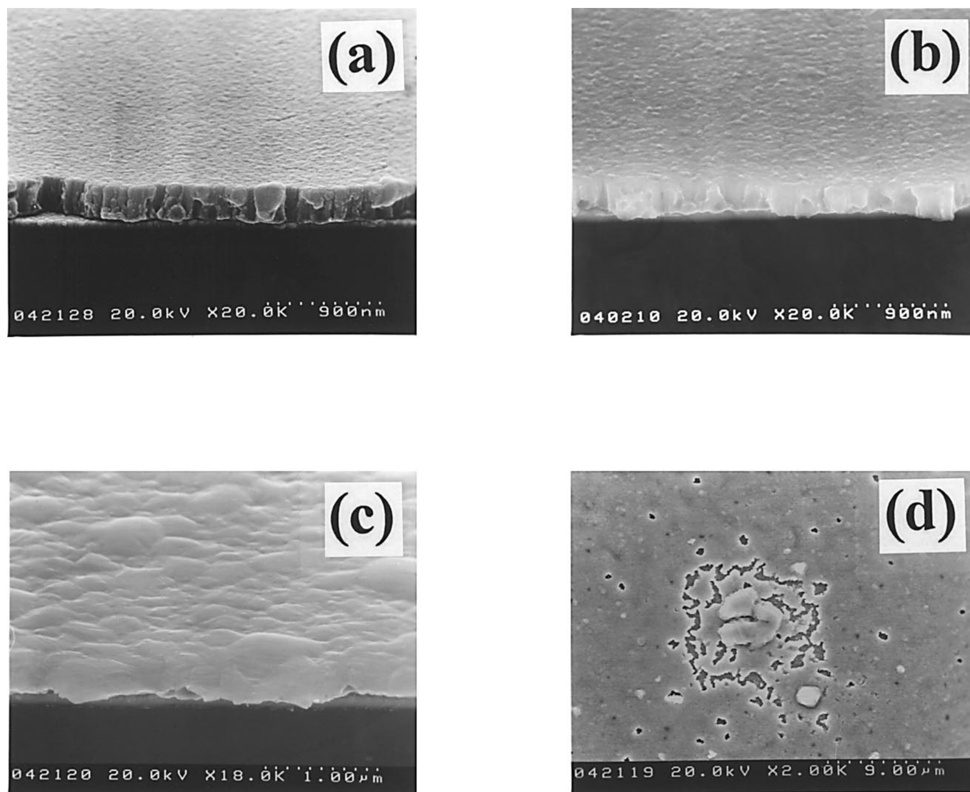

Figure 9. Oblique and top-view SEM micrographs for the Cu/WSiN/ WSi_x/p^+-n junction diodes (a) as-deposited, (b) annealed at 600°C, and (c) and (d) annealed at 650°C.

Conclusion

Thermal stability of CVD amorphous WSi_x layers, with and without N_2 plasma treatment, was investigated with respect to the diffusion barrier capability between Cu and Si substrates. We found that the barrier capability of WSi_x films can be efficiently improved by N_2 plasma treatment. Without N_2 plasma treatment, the thermal stability

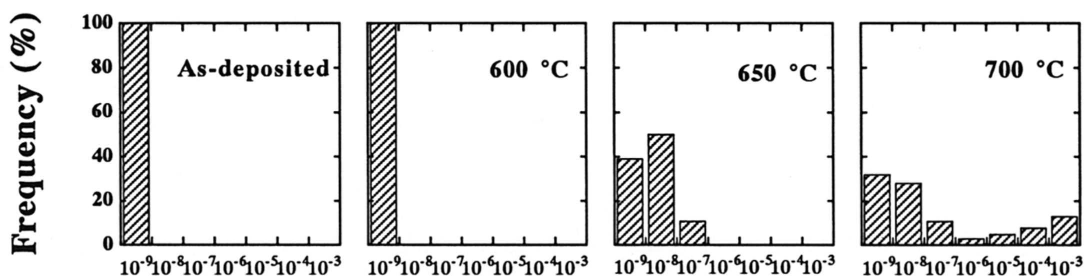

Figure 10. Histograms showing statistical distributions of reverse-bias leakage current density for the Cu/WSiN/WSi_y ($y > 1$)/p^+-n junction diodes annealed at various temperatures.

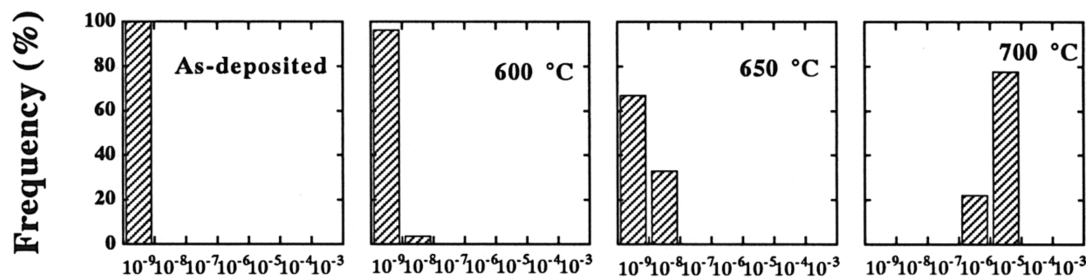

Figure 11. Histograms showing statistical distributions of reverse-bias leakage-current density for the Cu/WSiN/WSi_x (50 nm)/WSiN/WSi_x (10 nm)/ p^+-n junction diodes annealed at various temperatures.

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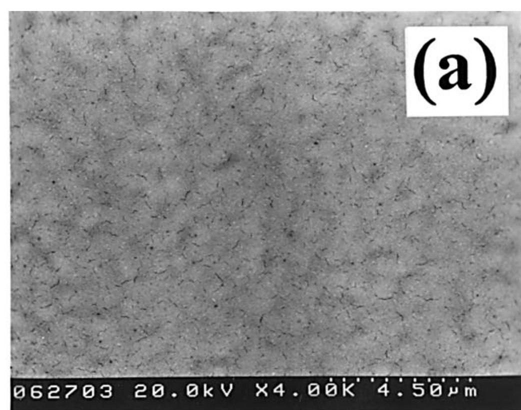
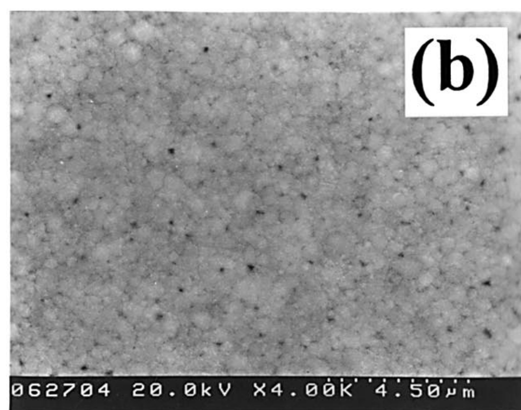




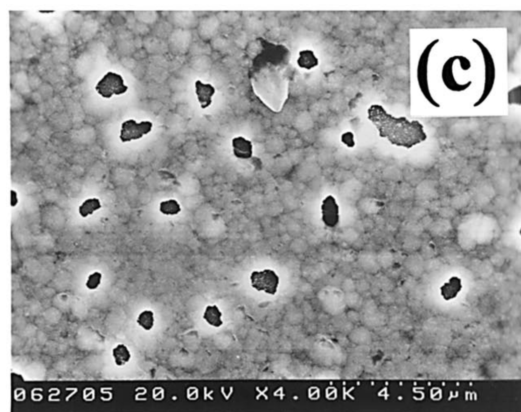
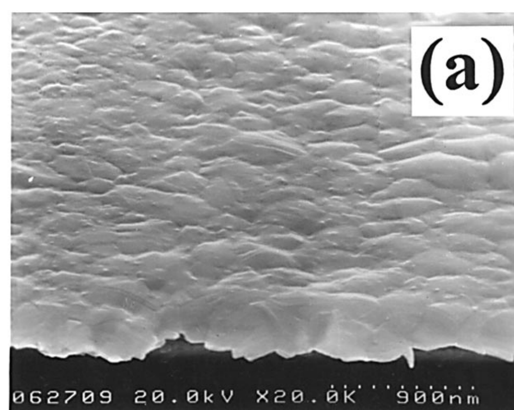


Figure 12. Top-view SEM micrographs for the Cu/WSiN/WSi_y/p^+-n junction diodes (a) as-deposited, (b) annealed at 650°C, and (c) annealed at 700°C.

of Cu/WSi_x (50 nm)/p^+-n junction diodes was found to reach 500°C. With N_2 plasma treatment applied to the WSi_x barrier, a nitrogen-containing thin layer of WSiN was formed on the surface of WSi_x, and the Cu/WSiN/WSi_x (50 nm)/p^+-n junction diodes were able to remain intact up to at least 600°C. Barrier failure mechanism for the WSiN/WSi_x bilayer was closely related to the WSi_x/Si interface reaction and the crystallization of the WSi_x layer. The thermal stability was further raised to 650°C by using a multilayer barrier structure of WSiN/WSi_x (50 nm)/WSiN/WSi_x (10 nm) or a WSiN/WSi_y ($y > 1$) barrier. We conclude that the post-CVD-WSi_x treatment with in situ N_2 plasma is a simple, practical, and efficient method of improving the WSi_x-based barrier capability for Cu metallization.



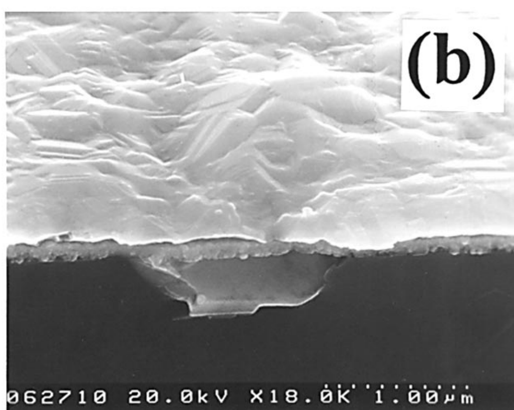


Figure 13. Oblique-view SEM micrographs for the Cu/WSiN/WSi_x/WSiN/WSi_x/p^+-n junction diodes annealed at (a) 650 and (b) 700°C.

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Table II. Thermal stability temperatures of WSi_x-based barrier layers determined by different techniques of measurement/analysis.

Measurement/analysis methods	Barrier structure: WSi_x (°C)	WSiN/WSi_x (°C)	WSiN/WSi_y ($y > 1$) (°C)	WSiN/WSi_x/WSiN/WSi_x (°C)
Leakage current	500	600	650	650
SEM	500	600	650	650
XRD	550	650		
Sheet resistance	550	650		

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References

1. S. P. Murarka, R. J. Gutmann, A. E. Kaloyeros, and W. A. Lanford, *Thin Solid Films*, **236**, 257 (1993).
2. N. Awaya, H. Inokawa, E. Yamamoto, Y. Okazaki, M. Miyake, Y. Arita, and T. Kobayashi, *IEEE Trans. Electron Devices*, **ED-43**, 1206 (1996).
3. C.-K. Hu, B. Luther, F. B. Kaufman, J. Hummel, C. Uzoh, and D. J. Pearson, *Thin Solid Films*, **262**, 84 (1995).
4. D. H. Kim, R. H. Wentorf, and W. N. Gill, *J. Electrochem. Soc.*, **140**, 3273 (1993).
5. J. C. Chiou, Y. J. Chen, and M. C. Chen, *J. Electron. Mater.*, **23**, 383 (1994).
6. C. A. Chang, *J. Appl. Phys.*, **67**, 566 (1990).
7. S. D. Brotherton, J. R. Ayres, A. Gill, H. W. V. Kesteren, and F. J. A. M. Greidanus, *J. Appl. Phys.*, **62**, 1826 (1987).
8. Y. S. Diamand, A. Dedhia, D. Hoffstetter, and W. G. Oldham, *J. Electrochem. Soc.*, **140**, 2427 (1993).
9. M.-A. Nicolet, *Thin Solid Films*, **54**, 415 (1978).
10. T. Nakano, H. Ono, T. Ohta, T. Oku, and M. Murakami, in *Proceedings of the VLSI Multilevel Interconnection Conference,* VMIC, p. 407, June (1994).
11. H. Ono, T. Nakano, and T. Ohta, *Appl. Phys. Lett.*, **64**, 1511 (1994).
12. K. Holloway and P. M. Fryer, *Appl. Phys. Lett.*, **57**, 1736 (1990).
13. S. Q. Wang, *J. Appl. Phys.*, **73**, 2301 (1993).
14. P. J. Pokela, C.-K. Kwok, E. Kolawa, S. Raud, and M.-A. Nicolet, *Appl. Surf. Sci.*, **53**, 364 (1991).
15. W. K. Yeh, T. T. Wu, M. H. Tsai, S. C. Sun, J. C. Chuang, and M. C. Chen, in *Proceedings of the VLSI Multilevel Interconnection Conference,* VMIC, p. 541, June (1996).
16. H. Ono, T. Nakano, and T. Ohta, *Jpn. J. Appl. Phys.*, **34**, 1827 (1995).
17. M. Wittmer, *Appl. Phys. Lett*., **36**, 456 (1980).
18. X. Sun, E. Kolawa, J. S. Chen, J. S. Reid, and M. A. Nicolet, *Thin Solid Films*, **236**, 347 (1993).
19. M. Takeyama, A. Noya, T. Sase, and A. Ohta, *J. Vac. Sci. Technol*., **B14**, 674 (1996).
20. K. Holloway, P. M. Fryer, C. Cabral, Jr., J. M. E. Harper, P. J. Bailey, and K. H. Kelleher, *J. Appl. Phys.,* **71**, 5433 (1992).
21. J. Y. Lee and J. W Park, *Jpn. J. Appl. Phys.*, **35**, 4280 (1996).
22. J. C. Chiou, K. C. Juang, and M. C. Chen, *J. Electrochem. Soc.*, **142**, 2326 (1995).
23. Y. Shimooka, T. Iijima, S. Nakamura, and K. Suguro, *Jpn. J. Appl. Phys*., **36**, 1589 (1997).
24. G. Minamihaba, T. Iijima, Y. Shimooka, H. Tamura, T. Kawanoue, H. Hirabayashi, N. Sakurai, H. Ohkawa, T. Obara, and K. Suguro, *Jpn. J. Appl. Phys.*, **35**, 1107 (1996).
25. P. M. Smith, J. S. Custer, J. G. Fleming, E. R. Osmun, M. Cohn, and R. V. Jones, in *Proceedings of the VLSI Multilevel Interconnection Conference,* VMIC, p. 162, June (1996).
26. T. Iijima, Y. Shimooka, G. Minamihaba, T. Kawanoue, H. Tamura, H. Hirabayashi, N. Sakurai, H. Ohkawa, T. Kubota, Y. Mase, M. Koyama, J. Ooshima, J. Wada, and K. Suguro, in *Proceedings of the VLSI Multilevel Interconnection Conference,* VMIC, p. 168, June (1996).
27. J. S. Reid, E. Kolawa, R. P. Ruiz, and M. A. Nicolet, *Thin Solid Film*s, **236**, 319 (1993).
28. A. Lahav and K. A. Grim, *J. Appl. Phys*., **67**, 734 (1990).
29. A. Hirata, T. Hosoya, K. Machida, H. Takaoka, and H. Akiya, *J. Electrochem. Soc.*, **143**, 3747 (1996).
30. Y. Akasaka, S. Suehiro, K. Nakajima, T. Nakasugi, K. Miyano, K. Kasai, H. Oyamatsu, M. Kinugawa, M. Takagi, K. Agawa, F. Matsuoka, M. Kakumu, and K. Suguro, in *Proceedings of the VLSI Multilevel Interconnection Conference,* VMIC, p. 168, June (1995).

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