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Microelectronics Reliability 39 (1999) 357–364

MICROELECTRONICS RELIABILITY

Oxide thickness dependence of plasma charging damage

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Received 18 August 1998; received in revised form 16 November 1998

Abstract

Charging damage induced in oxides with thickness ranging from 8.7 to 2.5 nm is investigated. Results of charge-to-breakdown (Q_{bd}) measurements performed on control devices indicate that the polarity dependence increases with decreasing oxide thickness at both room and elevated temperature (180°C) conditions. As the oxide thickness is thinned down below 3 nm, the Q_{bd} becomes very sensitive to the stressing current density and temperature. Experimental results show that severe antenna effect would occur during plasma ashing treatment in devices with gate oxides as thin as 2.6 nm. It is concluded that high stressing current level, negative plasma charging, and high process temperature are key factors responsible for the damage.

1. Introduction

The plasma charging effect, which may lead to severe oxide degradation during processing, has become one of major reliability concerns in ULSI manufacturing since the late 1980 s [1–7]. This can be ascribed to several reasons: (1) oxide becomes very susceptible to charging damage as its thickness (T_{ox}) is scaled below 10 nm. (2) Number of plasma steps employed in a chip fabrication increases significantly as the chip functionality and complexity advance. (3) In order to increase the throughput or to meet the critical requirements of deep-submicron manufacturing, process tools with high plasma current density, such as high current implantor and high-density plasma (HDP) reactors for etching and deposition applications, are increasingly used. These process steps may potentially aggravate the extent of charging.

When entering sub-quarter micron era ($T_{ox} < 6$ nm), the oxide thickness dependence of plasma charging damage presents an important and controversial topic. Park and Hu studied the damage induced in oxides (2.2 nm < T_{ox} < 7.7 nm) during metal and contact etching processes and showed that thinner oxide has superior immunity [3]. Alavi et al. showed that, as oxide is thinned down, the damage increases up to certain thickness (~4 nm), and then decreases due to direct tunneling [4]. Similar results were also found by Noguchi et al. in investigating the electron shading effect [5]. On the other hand, the results of Bayoumi et al. ([6], T_{ox} range: 8–4 nm), Krishinan et al. ([7], T_{ox} range: 6–3.5 nm) and Chien et al. ([8],T_{ox} range: 8–4 nm) showed that susceptibility of oxide to damage increases with decreasing oxide thickness. More recently, Krishinan et al. further showed that severe damage could be induced in gate oxide as thin as 2.1 nm under certain inductively coupled plasma (ICP)

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0026-2714/99/ - see front matter
PII: S0026-2714(98)00247-9

metal etch process conditions [9]. These different findings are understandable since the process conditions and equipment configurations can be very different from one study to another. For example, the down-stream reactor and process temperature (200°C) used in our studies could be very different from that used in others. As a consequence, results of plasma charging damage could also be very different. Meanwhile, degradation characteristics of oxide under high field stressing may change significantly as T_{ox} is thinned down, thus different kinds of indicators, e.g. charge-to-breakdown (Q_{bd}), breakdown field, threshold voltage (V_{th}), etc., used to characterize the damage may lead to a very different outcome.

When the oxide is thinner than 6 nm, an anomalous failure mode named 'soft-breakdown' (SB) or 'quasi-breakdown' [10–13] may be *frequently* induced during high electric field stressing. Albeit the *I–V* characteristics of SB are leaky, some residue oxide may remain on the soft-breakdown site, which is very different from that of the hard-breakdown (HB) mode. Such degradation has also been observed in characterizing the charging damage induced in gate oxides (4 nm) [8]. The appearance of SB events may further complicate the analysis of characterizing charging damage.

This study is intended to make the picture of T_{ox}-dependent charging damage clearer. Important factors including stress polarity, temperature and stress current level are investigated. Device parameter measurements are also performed on *n*-channel transistors with T_{ox} ranging from 8.7 to 2.5 nm. Charging damage induced during photoresist (PR) removal step in a down-stream reactor is also studied and analyzed.

2. Device fabrication

n-Channel transistors with n^+ poly-Si gate were fabricated on 6 in. Si wafers. The oxides were grown in an O_2/N_2 (1/6) furnace ambient at temperature ranging from 800° to 900°C. Oxide thickness ranging from 2.5 to 8.7 nm was determined by the ellipsometry and TEM methods on monitor wafers. For fabricated samples, the oxide thickness was also checked by the F–N *I–V* fitting [14, 15] method, which takes the poly-depletion effect into account, on the fabricated devices. Consistent results are obtained among these methods [16].

Metal pads with various surface areas were connected to the poly-Si gate electrode of these *n*-channel transistors and acted as the antenna. These metal patterns were defined with wet processing and then the PR layers were stripped off with the O_2 plasma in a down-stream asher. The process temperature was 200°C during ashing. Charging damage could be induced in this treatment and is analyzed by use of antenna devices. The antenna area ratio (AAR) is defined as the area ratio between the metal pad and the active region. In this study, the 'control devices' are referred to those with small AAR values (e.g. AAR < 20), assuming the induced damage is negligible in these samples.

3. T_{ox} dependence on Q_{bd} characterization

Constant current stressing was employed in this work to explore the time-dependent-dielectric breakdown (TDDB) characteristics of ultra-thin oxides. This method is appropriate for characterizing the charging damage since it has been pointed out that the plasma charging is likely to act as a non-ideal current source [17]. Fig. 1 shows typical *V–t* curves during the measurements with a current density of -0.2 A/cm^2. The abrupt drop in voltage at certain time indicates the occurrence of oxide breakdown. Nevertheless, the magnitude of post-breakdown voltages for SB and HB events are different. This difference has been pointed out in a recent report [18] that the post-breakdown voltage after HB is around 1 V or less, while that after SB can be 1 V in magnitude higher (e.g. > 2 V). In addition, the post-SB *V–t* curves show noisy characteristics. For oxides of 8 nm, only HB was observed, while both SB and HB can be induced in 4 nm-thick oxides, as shown in Fig. 4. When oxide is further scaled to 2.5 nm, it is found that SB exclusively dominates the breakdown events. Such a finding is also consistent with previous results [18], and could be ascribed

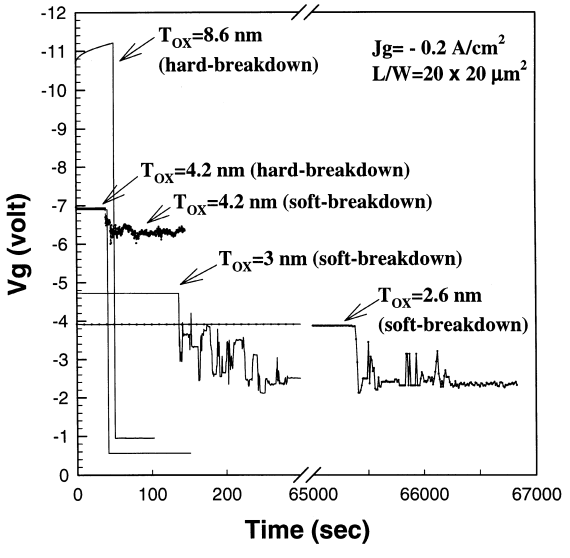

Fig. 1. Typical voltage–time curves of charge-to-breakdown measurements.

to the reduced trap generation rate under high field stressing as oxide thickness is reduced.

Fig. 2 shows the effect of stress polarity on the Q_{bd} results measured at 25 and 180°C, respectively. The definition of Q_{bd} used in this work is the amount of charge reached at the moment when either HB or SB is induced. The magnitude of stressing current density is fixed at 1 A/cm^2. The polarity dependence means the difference in Q_{bd} values between that obtained by gate injection ($V_g < 0$) and substrate injection ($V_g > 0$). It has been well documented in previous reports [19, 20] that the polarity dependence increases with decreasing T_{ox} for oxides thicker than 4 nm, and this is ascribed to the different properties between the poly-Si/oxide and oxide/Si interfaces. In this study, we observe that, as oxide is further scaled down, the polarity dependence becomes even stronger at both 25° and 180°C, as shown in Fig. 2. This is mainly due to the rise in Q_{bd} under substrate injection condition as oxide is thinned down, while the Q_{bd} under gate injection stressing remains relatively unchanged.

Fig. 3 shows the effects of stress current density and temperature on Q_{bd} under gate injection stressing. It is found that Q_{bd} of 2.6 nm-thick oxides is about three orders of magnitude higher than those of thicker oxides under current density of –0.2 A/cm^2 ($V_{ox}\approx$2.9 V for T_{ox} = 2.6 nm) at room temperature, indicating the higher tolerance to high field under DT process. However, when temperature is raised from room temperature to 180°C, Q_{bd} of 2.6 nm-thick oxides ($J = -0.2$ A/cm^2) is only about one order of magnitude higher than that of thicker oxides. This implies that the temperature acceleration effect is very significant for ultra-thin oxides under direct tunneling (DT) stressing. Such an effect is not clearly understood, and could possibly be related to the properties of oxide/Si interface, since it has been pointed out that the injected electrons may release energy at the interface [21].

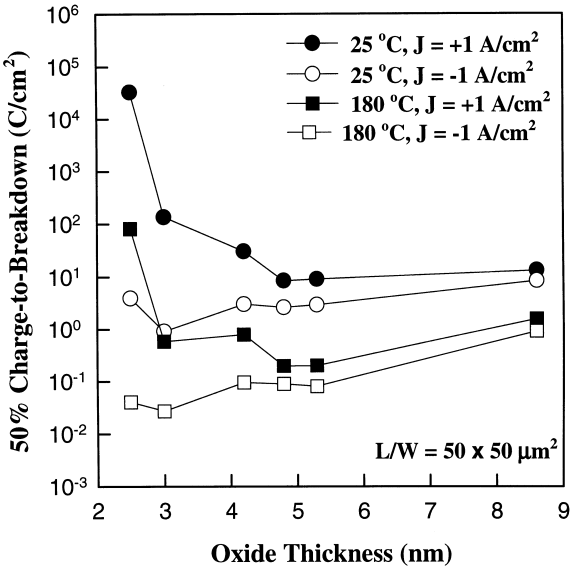

Fig. 2. 50% charge-to-breakdown measured at 25° and 180°C as a function of stress polarity and oxide thickness. AAR of the test samples is 4.

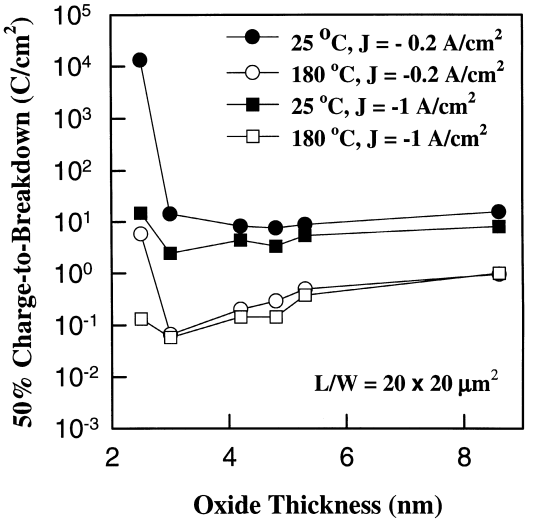

Fig. 3. 50% charge-to-breakdown measured at 25° and 180°C under gate injection of –0.2 and –1 A/cm^2, respectively, as a function of oxide thickness. AAR of the test samples is 16.

By increasing the current density to –1 A/cm^2 ($V_{ox}\approx$3.4 V), the thickness dependence on Q_{bd} shown in Fig. 3 is not significant at room temperature, while a drop in Q_{bd} is observed at 180°C as T_{ox} is scaled down. This indicates that, under the F–N stressing, thinner oxides may suffer more damage as temperature is raised. In addition, current density dependence of Q_{bd} is also reduced at high temperature. For oxide thinner than 3 nm, although not as strong as that in DT stressing, the temperature acceleration effect is also very significant. The temperature effect has been reported previously [22, 23]. In this study, however, we find that its role would be even more important as oxide is scaled below 4 nm, thus more attention should be paid in this aspect.

4. Charging damage induced during ashing

In this work, we characterized the charging damage induced in oxides during a photoresist (PR) stripping step in an RF down-stream O_2 plasma asher. Previously, we have investigated this system and found

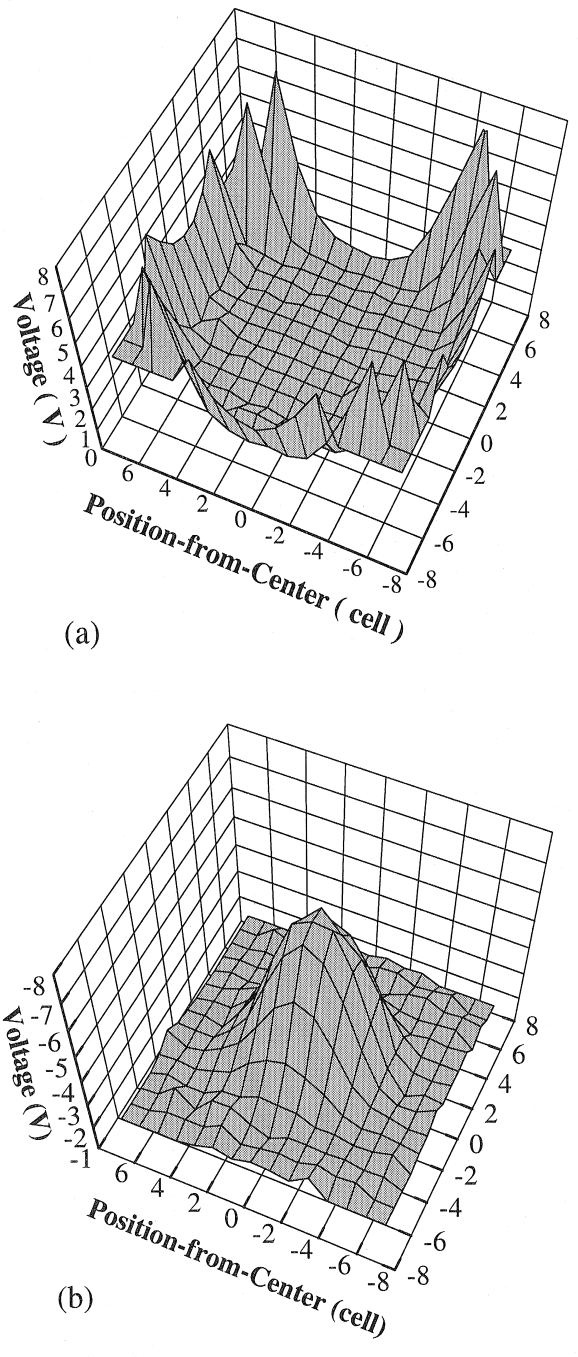

Fig. 4. Wafer maps of (a) positive and (b) negative potential values recorded by CHARM-2 sensors.

that severe antenna effect could occur at the wafer center [8, 24]. The cause of damage is presumably due to the non-uniform plasma generation resulted from the gas injection mode of the asher [25]. This is supported by the results of CHARM-2 monitor wafers, which contain a number of EEPROM sensors on the wafer surface used to measure the surface potential developed during plasma processing. Details of the measurement procedure can be found in [26]. As can be seen in Fig. 4(a) and (b), the CHARM-2 sensors recorded large positive and negative potential values at

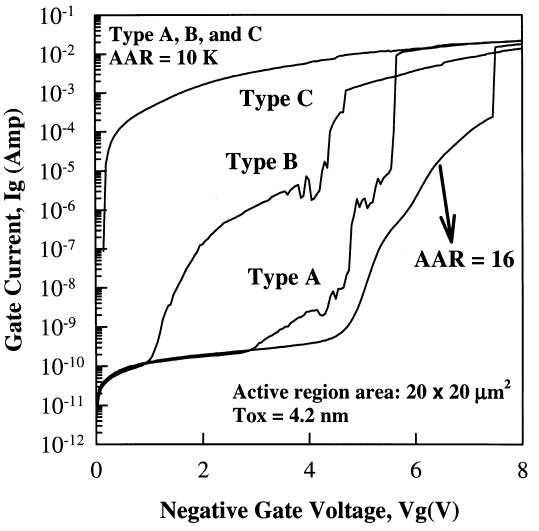

Fig. 5. Current–voltage characteristics of large (AAR = 10,000) and small (AAR = 16) antenna devices with T_{ox} of 4.2 nm.

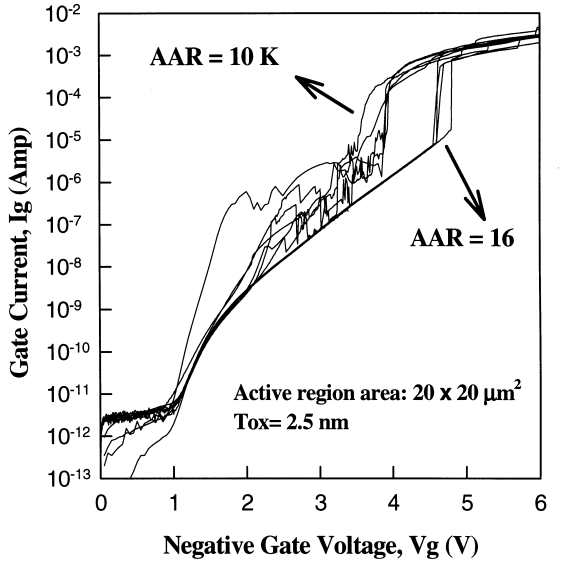

Fig. 6. Current–voltage characteristics of large (AAR = 10,000) and small (AAR = 16) antenna devices with T_{ox} of 2.5 nm.

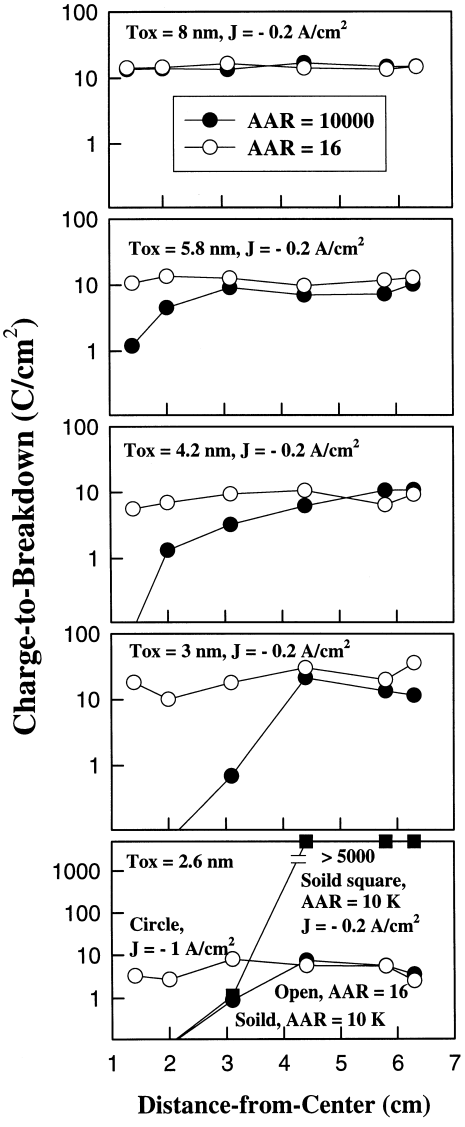

Fig. 7. Position dependence of charge-to-breakdown (Q_{bd}) as a function of oxide thickness and antenna area ratio. For samples with 2.6-nm-thick oxide, stress current densities of –0.2 (square symbol) and –1 A/ cm^2 (circle symbol) were used. Q_{bd} values are all over 5000 C/cm^2 for small AAR (16) samples under –0.2 A/cm^2 stressing (not shown).

the wafer edge and center, respectively. In the experiments, however, no significant damage was found in devices located at the wafer edge where positive charging is incurred. This can be ascribed to the strong polarity dependence shown in Fig. 2.

Figs. 5 and 6 show typical *I–V* characteristics of antenna devices with T_{ox} of 4 and 2.5 nm, respectively. Several devices located at the wafer center with a large AAR of 10,000 were chosen to illustrate the damage types, while devices with a small AAR of 16 were employed as control samples. In Fig. 5, it is seen that there are basically three types of damage, as represented by types A, B and C, respectively. The former two can be regarded as the SB degradation, since the voltage–time curve under constant current stressing performed on these samples exhibits noisy characteristics similar to that of SB events shown in Fig. 1. The difference between the two types could be related to the number of SB events already taken place in one sample [12, 13]. Type C represents the HB mode. As T_{ox} is thinned down to 2.5 nm, however, only SB events appear in large antenna devices, as shown in Fig. 6. This indicates that the oxide degradation processes could be different as oxide is scaled down.

Fig. 7 shows the Q_{bd} as a function of device location and antenna area ratio for oxides with thickness ranging from 2.6 to 8.7 nm. Each datum represents the average result of several measurement sites with identical distance-from-center. Constant current stressing was performed with current density of –0.2 A/cm^2. For efficient characterization, these devices were stressed either to breakdown or to a value of 5000 C/cm^2 if the oxides do not fail with stress current density

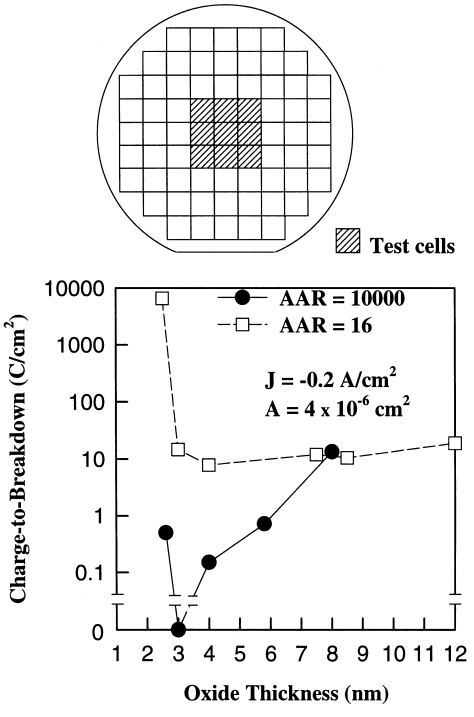

Fig. 8. Charge-to-breakdown results of antenna devices as a function of oxide thickness. The test cells where the large antenna devices (AAR = 10,000) are located are shown in the top portion of the figure. Each datum represents the average result of several measurements.

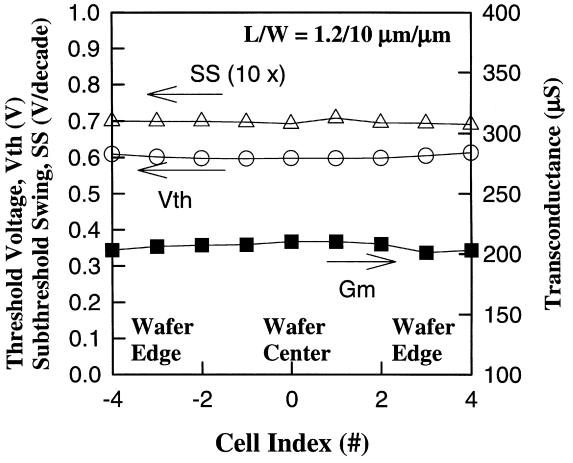

Fig. 9. Threshold voltage, subthreshold swing, and transconductance as a function of cell position. Antenna area ratio of the devices is 20,000. Oxide thickness is 2.5 nm.

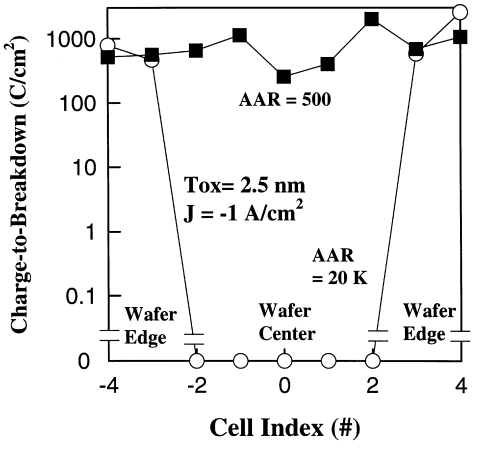

Fig. 10. Charge-to-breakdown values as a function of cell position. Channel length and width of the measured transistor are 1.2 and 10 μm, respectively.

of –0.2 A/cm^2. Stressing with –1 A/cm^2 was also performed on the devices with 2.6 nm-thick oxide. It is noted that the Q_{bd} of devices with small AAR of 16 is essentially independent of position and, therefore, can indeed be regarded as a damage-free reference, confirming our assumption made in previous section. For devices with large AAR (10,000), significant damage begins to appear at the wafer center as oxides are scaled below 6 nm and, for oxides thinner than 4 nm, oxide breakdown is induced at the wafer centre. As oxide is thinned down to 2.6 nm, Q_{bd} higher than 5000 C/cm^2 is observed for samples with small AAR of 16 (not shown) and also for samples with AAR of 10,000, but away from the center region under –0.2 A/cm^2 stress condition. In these devices, the abrupt increase in Q_{bd} as compared to that obtained under –1 A/cm^2 stress condition is explained by the higher tolerance to tunneling current stressing in DT (–0.2 A/cm^2) process. Nevertheless, the results shown in Fig. 7(e) clearly indicate that a severe antenna effect is induced at the wafer center.

Oxide thickness dependence on Q_{bd} is illustrated in Fig. 8, in which the average results obtained from control and damaged (AAR = 10,000) samples are shown and compared. The damaged samples are located in the nine cells (shown in this figure) at the wafer center. Constant current stressing of –0.2 A/cm^2 current density is performed on these devices. It is seen that, for oxides thicker than 3 nm, Q_{bd} of control samples is relatively independent of T_{ox}, while that of damage samples decreases with decreasing T_{ox}. For samples with T_{ox} of 3 nm, only SB was measured, as indicated by the '0' value of Q_{bd} in Fig. 8. When T_{ox} is thinned down to 2.6 nm, Q_{bd} of control devices rises significantly due to the transition of stress condition from F–N ($T_{ox} \geqslant 3$ nm) to DT process, as mentioned earlier. Nevertheless, the remaining Q_{bd} measured from the damage samples is much smaller. From the results shown in Figs. 2 and 3, it is understood that the damage characteristics of thinner oxides are very sensitive to stress polarity, current density (or oxide field), and temperature. The antenna effect shown in Figs. 6–8 can thus be mainly ascribed to the strong negative plasma charging (supported by the results of CHARM-2 monitors shown in Fig. 4), and elevated process temperature (200°C). The latter factor could be

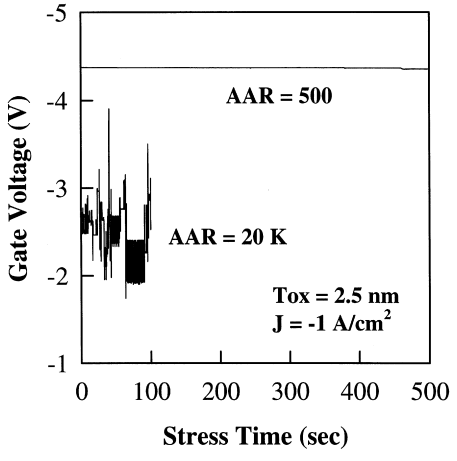

Fig. 11. Gate voltage variation during constant current stressing for devices located at the wafer center with small (AAR = 500) and large (AAR = 20,000) antenna.

even more important since the associated acceleration effect is very significant under both F–N and DT charging stress conditions.

The above analysis is mainly based on the Q_{bd} characterization. When other indicators are used, the feature of outcome might be different. This is shown in Fig. 9, in which V_{th}, subthreshold swing (SS), and transconductance (G_m) of transistors with T_{ox} of 2.5 nm and AAR of 20,000 are plotted as a function of device location. There seems to be no degradation in this plot. However, when Q_{bd} is used to characterize these devices, as shown in Fig. 10, significant antenna effect is identified. Such finding is ascribed to the significant decrease in the rates of trap creation and interface state generation under high-field stressing as oxide is scaled down (see Fig. 1) [20]. It is noted that the breakdown events found in the measurements of Fig. 10 all belong to the soft-breakdown type, consistent with the findings shown previously [18] and in the previous section. Typical V_g–t curves during constant current stressing are illustrated in Fig. 11. It is seen that soft breakdown with noisy characteristics [18] appears for large antenna device from the beginning of stressing. Interestingly, subthreshold characteristics of a transistor with such thin oxide depict little changes even after the charge-to-breakdown test. An example is shown in Fig. 12, in which the V_{th}, SS and G_m remain almost unchanged after oxide is stressed to soft-breakdown. Similar results were also reported recently [18,27]. The only parameter that depicts significant change shown in the figures is the gate leakage (I_g), which increases significantly after oxide breakdown. This could explain the different outcomes between Figs. 9 and 10 in monitoring the antenna effect.

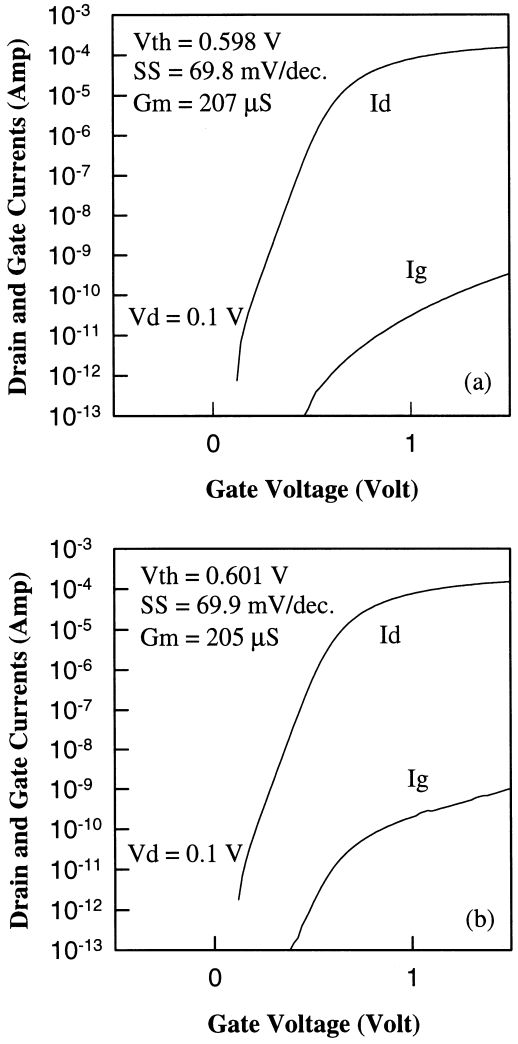

Fig. 12. Drain and gate currents as a function of gate voltage measured (a) before and (b) after charge-to-breakdown test. Channel length and width of the measured transistor are 1.2 and 10 μm, respectively.

5. Discussion and conclusions

Effects of gate oxide scaling on the plasma charging damage could be very complicated based on results obtained in this work. First of all, the occurrence of SB failure mode in the ultra-thin oxide regime has certain impacts on the device degradation caused by plasma charging. Even though the increase in gate leakage after SB does not exceed the drain current, and thus may not significantly affect the I–V characteristics of a transistor, it does impose certain concerns on circuit applications, such as the power consumption, data retention characteristics of memory devices, as well as the noise performance.

Regarding the plasma process conditions, three important factors should be carefully considered, namely, plasma current density, charging polarity and wafer temperature during processing. Among them, potentially enhanced damage effect caused by high plasma current presents an emerging concern, since more and more HDP tools are being implemented in modern production lines. The magnitude of charging current the antenna devices may encounter in an HDP environment could be of the order of 10 A/cm^2 [28], which is two orders higher than that in a conventional diode reactor. Such high current level would aggressively damage ultra-thin oxides in a short period.

It is also shown that the stress polarity dependence increases with decreasing oxide thickness down to 2.5 nm. This indicates that negative plasma charging may produce far more severe damage than positive plasma charging as oxide is thinned down, as is evi-

denced by the experimental results. Consequently, more attention should be paid on the regions of wafer surface where negative charging is identified.

The temperature acceleration effect is very significant for ultra-thin oxides. It is noted that any conclusion based on the extrapolation of Q_{bd} may not be reliable. In fact, one of the main purposes of this paper is to emphasize the accelerated degradation under high temperature and high stressing current, thus extrapolation would be unreliable. However, in this paper we also emphasize that these high-temperature, high-stressing current conditions do occur in real wafer processing steps (such as ashing and CVD), and therefore careful attention should be paid to ensure the resultant gate oxide integrity.

Finally, we have also compared the usefulness of several indicators in revealing the antenna effect. It is found that traditional methods of monitoring transistor parameters, including V_{th}, SS and G_m, may not be appropriate for detecting the charging damage in ultra-thin gate oxides. Consequently, some destructive methods, such as the charge-to-breakdown measurement, or the noise characterization techniques [9, 18], are necessary to evaluate plasma damage in ultra-thin oxides.

Acknowledgements

The authors would like to thank the staff of National Nano Device Laboratories and Dr B. Y. Tsui (ITRI/ERSO) for their technical assistance during the course. This work was supported by National Science Council of the Republic of China under contract no. NSC-87-2721-2317-200.

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