PERGAMON

Microelectronics Reliability 39 (1999) 415–424

MICROELECTRONICS RELIABILITY

New layout design for submicron CMOS output transistors to improve driving capability and ESD robustness

M.-D. Ker [a,*], T.-Y. Chen [b], H.-H. Chang [b]

[a] *VLSI Design Division, Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), U400, 195 ~ 11, Section 4, Chung-Hsing Road, Chutung, Hsinchu, Taiwan 310, Republic of China*

[b] *Integrated Circuits and Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, Republic of China*

Received 12 January 1998; received in revised form 16 July 1998

Abstract

New layout design to effectively reduce the layout area of CMOS output transistors but with higher driving capability and better ESD reliability is proposed. The output transistors of large device dimensions are assembled by a plurality of the basic layout cells, which have the square, hexagonal or octagonal shapes. The output transistors realized by these new layout styles have more symmetrical device structures, which can be more uniformly triggered during the ESD-stress events. With theoretical calculation and experimental verification, both higher output driving/sinking current and stronger ESD robustness of CMOS output buffers can be practically achieved by the proposed new layout styles within a smaller layout area in the non-silicided bulk CMOS process. The output transistors assembled by a plurality of the proposed layout cells also have a lower gate resistance and a smaller drain capacitance than that realized by the traditional finger-type layout.

1. Introduction

In submicron low-voltage CMOS technology, VDD was scaled down to reduce power consumption and to sustain better device reliability. To offer enough output driving/sinking current as well as to provide stronger electrostatic discharge (ESD) reliability, the W/L ratios of output transistors are often enlarged up to several hundreds, but in the high-integration applications, especially in the high-pin-count and pad-limited CMOS VLSI, the layout area available for each output pad with output buffer including latchup guard rings is critically limited. So, an area-efficient output buffer with high driving capability and high ESD robustness is strongly required in submicron CMOS technology.

In 1989, Baker proposed a *waffle-type* layout to enhance ESD hardness of NMOS output transistor [1]. In the waffle-type layout, the poly gate of the output transistor has a waffle structure to separate the drain and the source regions of an output transistor. A schematic waffle-type layout of an output NMOS is shown in Fig. 1, where the drain and the source have the same layout spacing from the contact to the poly gate. The waffle-type layout had been shown to offer better ESD robustness than that in the traditional finger-type layout within the same layout area. In 1992, Vemuru made a comparison between the finger-type and the waffle-type layout [2]. He reported that the waffle-type layout contributes about 10% area reduction to that of the finger-type layout, as well as producing lower gate resistance suitable for wide-band and low-noise applications [2].

Recently, some efforts have contributed to the investigation of the relations between the layout parameters and ESD hardness of submicron CMOS devices. It had been found that the spacing from the drain contact to the edge of gate oxide has an important impact on ESD robustness of CMOS devices [3–5], but the spacing from the source contact to the gate-oxide edge has no effect on the ESD robustness of output transis-

* Corresponding author. Fax: +866-3-5820025; e-mail: mdker@vlsi.ccl.itri.org.tw.

0026-2714/99/$ - see front matter
PII: S0026-2714(98)00203-0

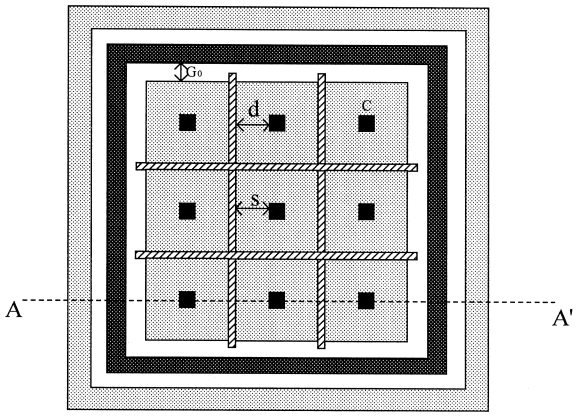


Fig. 1. The schematic diagram of the waffle-type layout.

tors in bulk CMOS ICs [6]. The typical spacing from the drain contact to poly gate of an output NMOS was suggested to be about 5 μm in the bulk CMOS technologies without the silicided diffusion to sustain better ESD protection without much increasing the layout area [6]. In the traditional finger-type layout, the spacing from the drain contact to the gate-oxide edge can be different from that from the source contact to the gate-oxide edge, but in the waffle-type layout, the spacings from both the source contact and the drain contact to the gate-oxide edge are equal. Due to this spacing constraint for ESD consideration, the output transistor realized by the waffle-type layout occupies more layout area than that realized by the traditional finger-type layout.

In this paper, three new layout styles (square [7, 8], hexagon [9], and octagon [10–12]) are proposed to realize CMOS output transistors within smaller layout area but with both higher driving capability and better ESD robustness.

2. Traditional finger-type layout

The traditional finger-type layout for an output NMOS is illustrated in Fig. 2. Its cross-sectional view along the line A–A′ in Fig. 2 is shown in Fig. 3, which

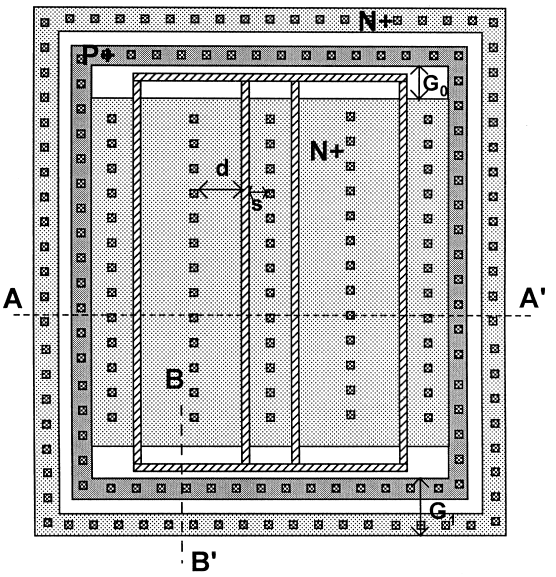


Fig. 2. A schematic diagram of the traditional finger-type layout.

is demonstrated in a p-substrate bulk CMOS process. In Fig. 2, the large-dimension NMOS device is separated as four parallel small-dimension NMOS devices. The spacing from the drain contact to the poly gate is marked '*d*'. The spacing from the source contact to the poly gate is marked '*S*'. For better ESD robustness, this spacing *d* is specified as 5 μm in a typical 0.6-μm CMOS process, but the spacing *S* has no important effect on ESD reliability of CMOS output buffers in grounded substrate CMOS technologies [6]. This spacing *S* is often drawn as 1 μm in practical layout. Outside the source region, there are two latchup guard rings surrounding the whole NMOS device. One is a *P*+ diffusion connected to ground (GND) to supply the substrate bias. The other is an *N*+ diffusion connected to VDD as a dummy collector to prevent CMOS latchup.

However, in the traditional finger-type layout, there is an important spacing denoted as 'G_0' in Fig. 2, which often degrades ESD robustness of CMOS output buffer. To explain this 'G_0' spacing, a schematic

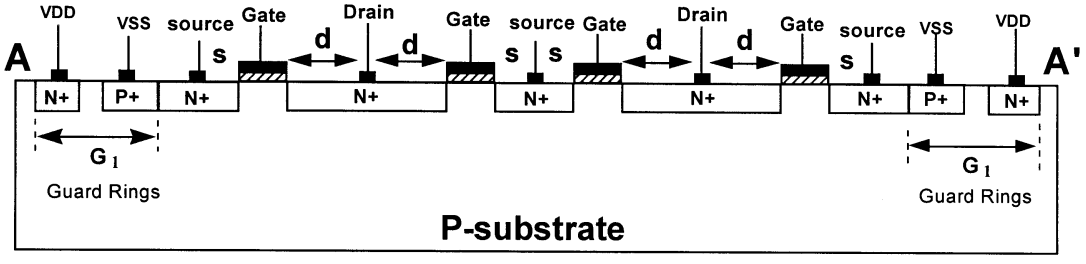


Fig. 3. The cross-sectional view of the NMOS device along the line A–A′ in Fig. 2.

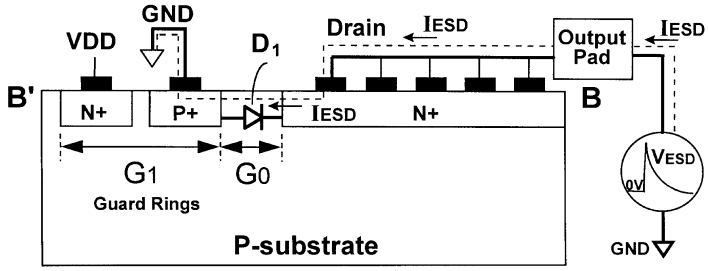


Fig. 4. The cross-sectional view along the line B–B′ in Fig. 2 to show the ESD peak-discharging effect of the finger's end of the finger-type layout.

cross-sectional view along the line B–B′ in Fig. 2 is shown in Fig. 4. In Fig. 4, there exists a parasitic diode D1 between the $P+$ diffusion (connected to GND) and the $N+$ diffusion of the drain. The spacing from the edge of $P+$ diffusion to the edge of drain $N+$ diffusion is marked as 'G_0'. If this spacing is smaller than that from the drain contact to its source contact, the diode D1 will be first broken down due to the ESD peak-discharging effect before the NMOS drain is broken down. Because the drain edge at this side has a finger structure, this diode D1 is vulnerable to ESD stress if G_0 is too small. Even if the spacing from the drain contact to this drain edge (D1) is larger than the spacing d in the finger-type NMOS device, the ESD hot spot may still occur at this drain edge due to the peak structure at the finger's end of the finger-type layout. A typical EMMI photograph of ESD damage on the finger's end (diode D1) of a finger-type output buffer is shown in Fig. 5, where a hot spot occurs only at the end of a drain finger. In Fig. 5, the spacing from the drain contact to the drain edge (in the B–B′ direction of Fig. 2) is 5.5 μm. The drain contact to the poly gate (in the A–A′ direction of Fig. 2) is 5 μm. The spacing G_0 is drawn as 4 μm. The ESD failure in Fig. 5 is due to the machine-model (MM) PS-mode ESD stress. The machine-model ESD stress of 200 V has a higher and faster ESD current than that of the human-body-model (HBM) ESD stress of 2000 V. In the fast ESD transition, not only the spacing effect but also the peak-discharging effect can cause the ESD damage located on the drain finger's end in Fig. 5. Thus, with the consideration on ESD reliability, this G_0 spacing had better be greater than the spacing from the drain contact to the source contact.

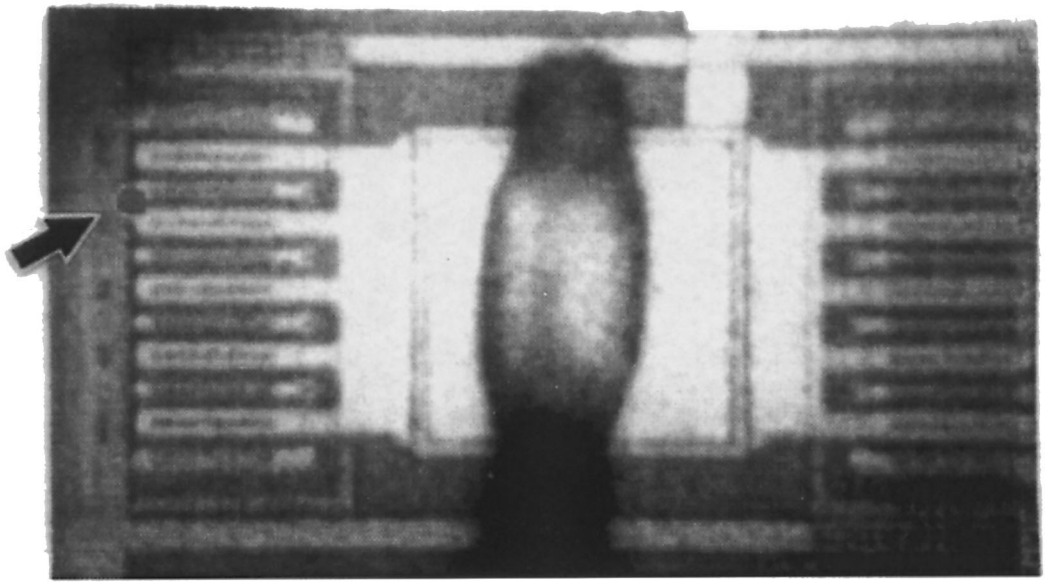


Fig. 5. An EMMI microphotograph of ESD damage on a finger-type CMOS output buffer after a PS-mode ESD stress. Only a hot spot is observed at the end of a drain finger, which is indicated by an arrow.

The total layout area of an NMOS transistor in the finger-type layout including two latchup guard rings can be calculated by the following equations. In the TSMC (Taiwan Semiconductor Manufacturing Company) 0.6-μm SPDM (single-poly–double-metal) design rules, the channel width 'w' of each finger in the finger-type layout is specified to be between 25 and 50 μm. The total layout area of a finger-type NMOS transistor with double guard rings is

$$A_{\text{finger}} = \left[(d + L + S + c) \cdot \frac{W}{w} + 2G_1\right] \cdot [w + 2(G_0 + G_1)] \quad (1)$$

where L is the channel length; W is the total channel width; w is the channel width of each poly-gate finger; d is the spacing from the drain contact to the poly-gate edge; S is the spacing from the source contact to the poly-gate edge; c is the width of a contact; G_1 is the spacing of the double guard rings; and G_0 is the spacing from the drain $N+$ diffusion to the $P+$ diffusion guard ring.

The total number of poly gate fingers in the whole NMOS layout is $W/w = N$, where N must be an integer. The total layout area of the drain diffusion can be obtained as

$$AD_{\text{finger}} = W \cdot (d + c/2) \quad (2)$$

The total perimeter of the drain region ($N+$ diffusion) in the whole NMOS layout is

$$PD_{\text{finger}} = W + 2\frac{W}{w} \cdot (d + c/2) \quad (3)$$

The layout area and the perimeter of the drain diffusion have an effect on the drain capacitance of the NMOS device. Thus, the total drain diffusion capacitance is

$$CD_{\text{finger}} = C_J \cdot AD_{\text{finger}} + C_{JGATE} \cdot W + C_{JSW} \cdot (PD_{\text{finger}} - W) \quad (4)$$

where C_J is the bulk junction capacitance; C_{JGATE} is the gate-edge sidewall bulk junction capacitance; and C_{JSW} is the sidewall bulk junction capacitance. From the above equations, the layout area and drain junction capacitance in the finger-type layout can be accurately calculated.

3. New layout design

To reduce layout area for saving silicon cost and to overcome the peak-discharging effect in the traditional finger-type layout, three new layout styles for output transistors are proposed.

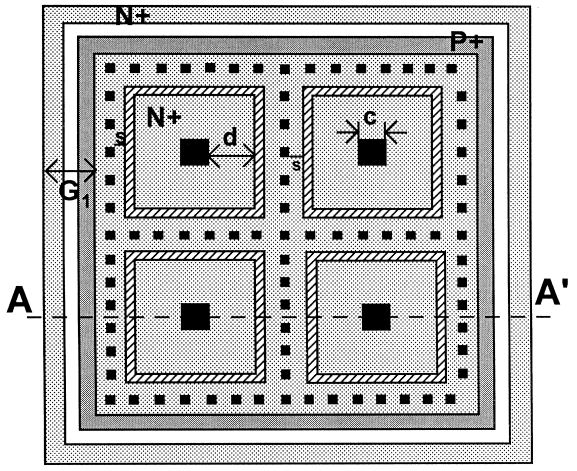


Fig. 6. The schematic diagram of the proposed square-type layout.

3.1. Square-type layout

The schematic square-type layout of an output NMOS is shown in Fig. 6. The schematic cross-sectional view along the line A–A′ in Fig. 6 is also the same as that shown in Fig. 3. In Fig. 6, there are four small-dimension square cells to form a large-dimension NMOS device. Each small-dimension square cell is identical to the other. The black square region in the center of a square cell is the drain contact of the NMOS device. The poly gate in each square cell is drawn in a square ring. The $N+$ diffusion of the source region is drawn in a square shape which surrounds the gate and the drain regions. The contacts at the source region are placed in a square-shape arrangement. Outside the NMOS device, there is a $P+$ diffusion connected to ground to offer the substrate bias. This $P+$ diffusion surrounds the whole NMOS device. Besides, an $N+$ diffusion surrounding this $P+$ diffusion and connected to VDD works as latchup guard ring. All the layout elements in a square cell, including the contacts, have to be placed as symmetrically as possible to ensure uniform ESD current flow in the NMOS device to increase its ESD reliability. An NMOS device with a larger device dimension can be assembled by a plurality of the square cells.

By using this proposed square-type layout design, there is no G_0 spacing in the square-type output transistors. The layout area due to the wider G_0 spacing in the traditional finger-type layout can be saved. Moreover, no parasitic diode directly closes to the drain edge in the square-type layout, so the ESD robustness of output transistors is not degraded by the ESD peak-discharging effect as shown in Fig. 5 with the finger-type layout.

In the square-type layout, the total layout area of the output NMOS transistor can be calculated as:

$$A_{\text{square}} = \left[\left(\frac{w}{4} + 2L + 2S\right) \cdot M + 2G_1\right] \cdot \left[\left(\frac{w}{4} + 2L + 2S\right) \cdot N + 2G_1\right] \quad (5)$$

where $w = 4(2\,d + c)$ is the channel width of a single square cell; c is the width of the square drain contact in the square cell; M is the number of square cells in the column direction of the whole NMOS layout; and N is the number of square cells in the row direction of the whole NMOS layout.

The total number of the square cells in a whole NMOS layout is $M \times N$. The total diffusion area of the drain region ($N+$ diffusion) is

$$AD_{\text{square}} = \frac{wW}{16} \quad (6)$$

The total diffusion perimeter of the drain region ($N+$ diffusion) is

$$PD_{\text{square}} = W. \quad (7)$$

The total drain junction capacitance can be calculated as

$$CD_{\text{square}} = C_{\text{J}} \cdot AD_{\text{square}} + C_{\text{JGATE}} \cdot W \quad (8)$$

There is no C_{JSW} term in Eq. (8), because the drain regions of the output transistor in the square-type layout is fully surrounded by the poly gate.

3.2. Hexagon-type layout

The schematic diagram of the hexagon-type layout of an output NMOS is shown in Fig. 7. The schematic cross-sectional view along the line A–A′ in Fig. 7 is also the same as that shown in Fig. 3. In Fig. 7, there are four small-dimension hexagon cells to form a large-dimension NMOS device. The poly gate in each hexagon cell is also drawn in a hexagon ring. The $N+$ diffusion of the source is also drawn in the hexagonal shape and surrounds the gate and drain regions. The contacts at the source region are also placed in a hexagon-shape arrangement. All the layout elements in the hexagon cell, including the placement of contacts, are drawn as symmetrically as possible to ensure uniform current flow in the NMOS device to increase its ESD reliability. An NMOS device with a larger dimension can be assembled as a plurality of the hexagon cells.

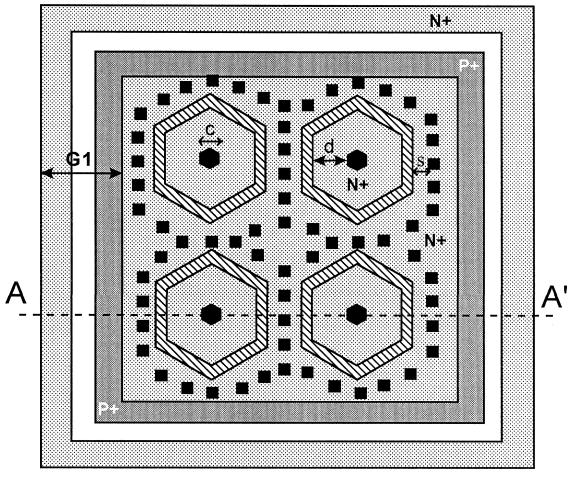


Fig. 7. The schematic diagram of the proposed hexagon-type layout.

In the hexagon-type layout, the total layout area of an NMOS output transistor can be calculated by following equations. The total layout area is

$$A_{\text{hexagon}} = \left[\left(\frac{\sqrt{3}}{6}w + 2L + 2S\right) \cdot M + 2G_1\right] \cdot \left[\left(\frac{1}{3}w + \frac{4}{\sqrt{3}}L + \frac{4}{\sqrt{3}}S\right) \cdot N + 2G_1\right] \quad (9)$$

where $w = (6(2d + c))/\sqrt{3}$, which is the channel width of a single hexagon cell (μm); c is the diameter of the hexagon drain contact in the hexagon cell (μm); M is the number of hexagon cells in the column direction of the whole NMOS layout; N is the number of hexagon cells in the row direction of the whole NMOS layout.

The total number of the hexagon cells in a whole NMOS layout is $M \times N$. The total layout area of the drain diffusion can be obtained as

$$AD_{\text{hexagon}} = \frac{\sqrt{3}}{24}w \cdot W \quad (10)$$

The total perimeter of the drain diffusion in the whole NMOS layout is

$$PD_{\text{hexagon}} = W \quad (11)$$

The total drain junction capacitance can be calculated as

$$CD_{\text{hexagon}} = C_{\text{J}} \cdot AD_{\text{hexagon}} + C_{\text{JGATE}} \cdot W \quad (12)$$

3.3. Octagonal-type layout

The schematic diagram to assemble an output NMOS transistor by the octagon cells is shown in Fig. 8. Its schematic cross-sectional view along the line A–A′ of Fig. 8 is the same as that in Fig. 3. In Fig. 8, the black octagonal region in the center of an octagon cell is the drain contact of the NMOS device. The poly gate in the octagon cell is drawn in an octagonal ring The $N+$ diffusion of source is also drawn in an octagonal shape. The source contacts of the octagon cell are

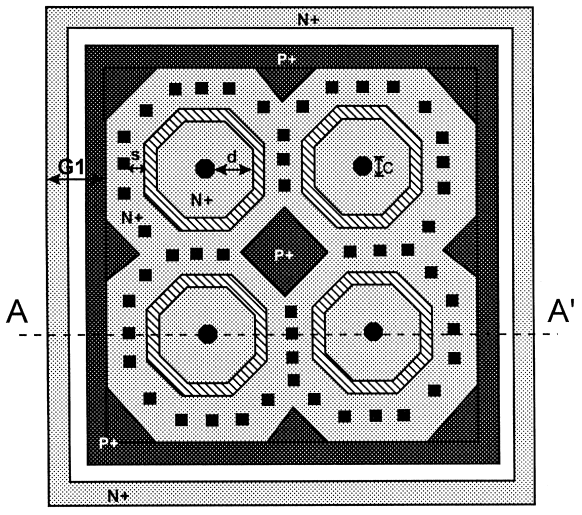


Fig. 8. The schematic diagram of the proposed octagon-type layout.

arranged in an octagonal pattern around the ring gate. All the layout elements in the octagon cell, including the contacts, are drawn as concentric and symmetrical as possible to ensure uniform current flow in the output transistor to increase its ESD robustness. An NMOS device with larger dimension can be assembled by a plurality of the octagon cells.

The total layout area of an NMOS transistor in the octagon-type layout is

$$A_{\text{octagon}} = \left\{\left[\left(\frac{1+\sqrt{2}}{8}\right)w + 2L + 2S\right]\cdot N + 2G_1\right\} \cdot \left\{\left[\left(\frac{1+\sqrt{2}}{8}\right)w + 2L + 2S\right]\cdot M + 2G_1\right\} \tag{13}$$

where $w = (16d + 8c)/(1+\sqrt{2})$, which is the channel width of a single octagon cell (μm); c is the diameter of the octagonal drain contact in the octagon cell (μm); M is the number of octagon cells in the column direction of the whole NMOS layout; and N is the number of octagon cells in the row direction of the whole NMOS layout.

The total layout area of the drain diffusion is

$$AD_{\text{octagon}} = \left(\frac{1+\sqrt{2}}{32}\right)w^2 \tag{14}$$

The total perimeter of the drain diffusion is

$$PD_{\text{octagon}} = W \tag{15}$$

The total drain capacitance is

$$CD_{\text{octagon}} = C_J \cdot AD_{\text{octagon}} + C_{\text{JGATE}} \cdot W \tag{16}$$

3.4. Comparison and discussion

To verify the layout efficiency, comparison on the total layout area of an NMOS transistor among the traditional finger-type layout and the proposed new layout styles under the same spacing d of 5 μm is shown in Fig. 9. The total layout area includes the spacing G_1 of 10.3 μm (the spacing of double latchup guard rings) in both the traditional finger-type layout and the proposed new layout styles. The channel length in Fig. 9 is kept as 0.8 μm. The square-type, hexagon-type, and octagon-type layouts provide about 30%, 25% and 20% reduction on the layout area, respectively, as compared with the finger-type layout. If the spacing d or the channel width are increased, the proposed new layout styles can save much more layout area. It has obviously been shown that the NMOS (or PMOS) transistor realized by the square-type layout can save more layout area than those by the other layout styles.

Moreover, the drain-to-bulk junction capacitance at the output node is also reduced by the proposed layout styles. Fig. 10 shows the dependence of the drain capacitance ratio on the layout spacing d among the finger-type and the proposed layout styles. The drain junction capacitance in the square-type, hexagon-type, and octagon-type layouts is about 62.5% of that in the finger-type layout, as the spacing d is 5 μm. When the spacing d is varied from 3 to 10 μm, the drain capacitance of an NMOS device realized by the proposed new layout styles can be significantly reduced about 30–45%, as compared with that by the finger-

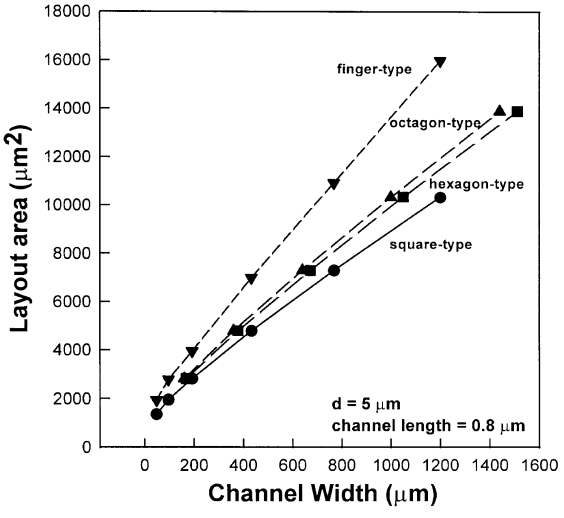


Fig. 9. Comparison of layout area among the four different layout styles with the spacing d of 5 μm.

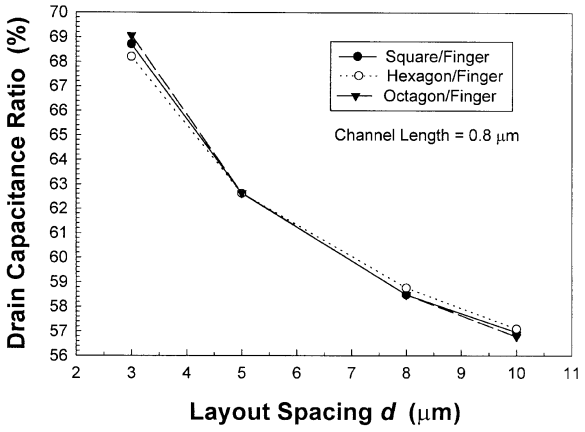


Fig. 10. The dependence of drain capacitance ratio on the layout spacing d among the three new layout styles, as compared with the traditional finger-type layout style.

type layout. With a lower drain capacitance, the proposed new layout styles are more suitable for CMOS output buffers in high-speed or high-frequency applications.

In the new layout design, there is no G_0 spacing in the square-type, hexagon-type and octagon-type layouts. The layout area occupied by the spacing G_0 in the traditional finger-type layout can be saved. Moreover, the peak-discharging effect on the end of the drain fingers can be avoided, because no parasitic diode directly closes to the edge of the drain region in the new layout design. For ensuring the most uniform ESD current flow, a circle-type layout is theoretically the best choice, but in the present CAD tools used to generate the IC layouts and the masks for IC fabrication are still unable to make a real circle-type device. The proposed square-type, hexagon-type and octagon-type layout styles are not the only choice to implement output transistors. The layout style can be implemented in any regular polygon of n sides [10]. For $n \to \infty$, the layout is nearly a real circle type. But, a polygonal layout with a large n becomes more difficult and complex to be drawn.

4. Experimental results

One set of output buffers with different W/L ratios in the finger-type layout and the proposed new layout styles has been designed and fabricated in 0.6-μm bulk CMOS processes without silicided diffusion. The microphotographs of the fabricated CMOS output buffer in the square-type, hexagon-type, and the octagon-type layouts are shown in Fig. 11.

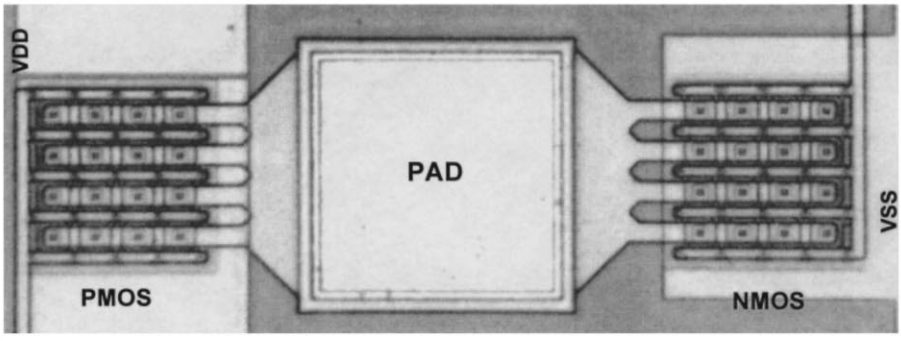
4.1. Output driving/sinking capability

The driving/sinking capability of a CMOS output buffer can be monitored by measuring the I–V curves of the output NMOS and PMOS. The drain current of the output NMOS (PMOS) is measured under the bias of $V_{ds} = 3$ V (-3 V) and $V_{gs} = 3$ V (-3 V) with its source grounded. The measured sinking/driving currents of the fabricated output buffers in the square-type and hexagon-type layouts versus the total layout area, as compared with the finger-type layout, are shown in Fig. 12. Fig. 12(a) shows the dependence of the drain current on the layout area of the output PMOS. The drain current of the square-type and hexagon-type layouts almost linearly increases while the layout area of the output PMOS is increased. The maximum driving current per layout area is about 8.5 (6.5) μA/μm^2 for the output PMOS in the square-type (hexagon-type) layout, whereas the output PMOS in the finger-type layout has a maximum driving current of 5.1 μA/μm^2. The maximum driving capability per layout area of the output PMOS in the square-type (hexagon-type) layout is improved about 67% (27%) more than that in the finger-type layout. Fig. 12(b) shows the relation between the drain current and the layout area of the output NMOS among the finger-type, the square-type and the hexagon-type layouts. The maximum sinking current per layout area is about 17.6 (13.4) μA/μm^2 for the output NMOS in the square-type (hexagon-type) layout, whereas the output NMOS in the finger-type layout has a maximum sinking current of 12.2 μA/μm^2. The maximum sinking capability per layout area of the output NMOS in the square-type (hexagon-type) layout is improved about 44% (9.8%) more than that in the finger-type layout.

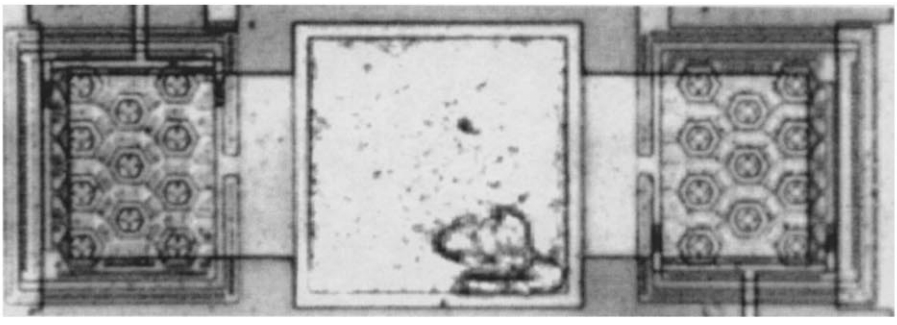
The output driving/sinking capability of the octagon-type CMOS output buffer is summarized in Table 1 to verify the area efficiency. This octagon-type layout is realized in another single-poly triple-metal 0.6-μm CMOS process. The maximum output sinking (driving) current per layout area of the octagon-type output NMOS (PMOS) device is 13.12 (6.59) μA/μm^2, but that in the finger-type device is only 9.77 (4.46) μA/μm^2. So, the octagon-type NMOS (PMOS) device provides an increase of 34.3% (47.7%) on the output sinking (driving) current per layout area, as compared to the finger-type device. This practically confirms the higher driving capability of the proposed new layout design for output transistors.

4.2. Output ESD robustness

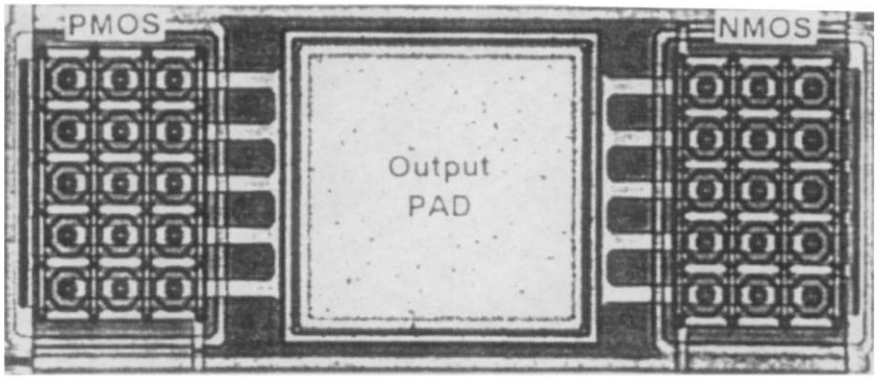
The HBM (human-body-model) ESD levels of the output PMOS in the finger-type and square-type lay-



(a)



(b)



(c)

Fig. 11. The microphotographs of the fabricated CMOS output buffers in (a) the square-type, (b) the hexagon-type, and (c) the octagon-type, layout styles.

outs are shown in Fig. 13(a). The HBM ESD robustness per layout area of the output PMOS in the square-type layout is about 0.65 V/μm^2, but that in the finger-type layout is only 0.53 V/μm^2. Thus, the output PMOS in the square-type layout provides an increase of 22.6% in the HBM ESD robustness, as compared with the finger-type layout. The HBM ESD levels of the output NMOS in the finger-type, square-type and hexagon-type layouts are shown in Fig. 13(b). The HBM ESD robustness per layout area of the output NMOS in the square-type (hexagon-type) layout is about 0.57 (0.69) V/μm^2, but that in the finger-type layout is only 0.5 V/μm^2. Thus, the output NMOS in the square-type (hexagon-type) layout provides an increase of 14% (38%) on the HBM ESD robustness, as compared to the finger-type layout. This has verified

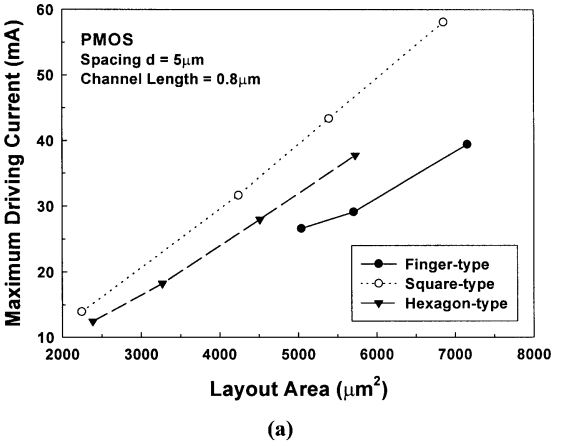


Fig. 12. Experimental results of the maximum (a) driving current, (b) sinking current, of the CMOS output buffer in the finger-type, the square-type, and the hexagon-type layouts with a 3 V power supply.

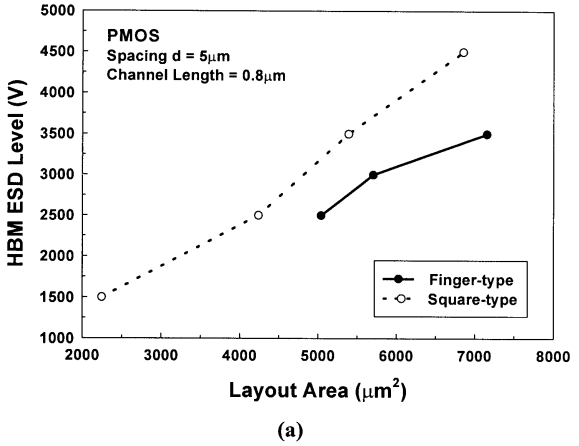


Fig. 13. Testing results of the HBM ESD-sustaining voltage of (a) the output PMOS, (b) the output NMOS, in the finger-type, the square-type, and the hexagon-type layouts.

that the proposed square-type and hexagon-type layouts can provide the output transistor with higher ESD robustness per layout area.

The ESD level of the octagon-type layout realized in the single-poly triple-metal 0.6-μm CMOS process is also tested and compared to the finger-type layout. The ESD test results including the HBM, MM and CDM (charged-device-model) ESD events on the octagon-type and the finger-type layouts are listed in Table 2. The HBM (MM) ESD robustness per layout area of the octagon-type output buffer is 0.74 (0.12) V/μm^2, but that in the finger-type output buffer is only 0.53 (0.065) V/μm^2. This octagon-type layout design

Table 1
Comparison on the driving/sinking current between the octagon-type and the finger-type CMOS output buffers

	Finger-type layout	Octagon-type layout
Device dimension for NMOS and PMOS W/L (μm)	720/0.8	804/0.8
Layout area (μm^2)	112×110	110×74
NMOS drain current I_{ds} ($V_{ds} = V_{gs} = 3$ V)	120.4 mA	106.8 mA
PMOS drain current I_{ds} ($V_{ds} = V_{gs} = -3$ V)	−54.95 mA	−53.69 mA
NMOS I_{ds} of per unit layout area	9.77 μA/μm^2	13.12 μA/μm^2
PMOS I_{ds} of per unit layout area	−4.66 μA/μm^2	−6.59 μA/μm^2

Table 2
Comparison on the ESD robustness between the octagon-type and the finger-type CMOS output buffers

	Finger-type layout	Octagon-type layout
Device dimension for NMOS and PMOS W/L (μm)	720/0.8	804/0.8
Layout area (μm^2)	112×110	110×74
HBM ESD pass voltage	6500 V	6000 V
MM ESD pass voltage	800 V	950 V
CDM ESD pass voltage	$> \pm 2000$ V	$> \pm 2000$ V
HBM pass voltage of per unit layout area	0.53 V/μm^2	0.74 V/μm^2
MM pass voltage of per unit layout area	0.065 V/μm^2	0.12 V/μm^2

provides an increase of 41.5% (84.6%) on the HBM (MM) ESD robustness per layout area. The CDM ESD robustness per layout area of an octagon-type output buffer can be greater than 0.25 V/μm^2. As seen in Table 2, the CMOS output buffer in the octagon-type layout can pass the HBM ESD stress of 6000 V, but that in the finger-type layout can pass the HBM ESD stress of 6500 V. However, in the MM ESD testing, the CMOS output buffer in the octagon-type layout can pass the MM ESD stress of 950 V, but that in the finger-type layout can only pass the MM ESD stress of 800 V. This is due to the $P+$ diffusion connected to VSS (the $N+$ diffusion connected to VDD) as the substrate (n-well) bias among the multiple octagon cells of an NMOS (PMOS) device in the octagon-type layout. In the finger-type layout, the $P+$ diffusion (or $N+$ diffusion) for substrate bias often surrounds the whole NMOS (or PMOS) device only at the outside, but the internal fingers of the finger-type device are far from the substrate (n-well) bias. This easily leads to non-uniform turn-on behavior among the multiple fingers of a finger-type device during the ESD stress and causes a low ESD reliability.

Because there are many P+ islands ($N+$ islands) connected to VSS (VDD) among the multiple cells of the octagon-type output NMOS (PMOS) to uniformly provide the p-substrate (n-well) bias, the uniform turn-on behavior among the multiple cells of the output buffer is further enhanced by the octagon-type layout. Thus, the octagon-type layout performs a much better ESD robustness per layout area than the square-type and the hexagon-type layouts, especially in the MM ESD events with fast ESD transition. However, the $P+$ islands ($N+$ islands) in the octagon-type output NMOS (PMOS) occupy some extra layout area, and they need a CMOS process with three metal layers to realize the output buffers in such octagon-type layout structure.

5. Conclusion

With theoretical calculation and experimental verification, three new layout styles (square-type, hexagon-type, and octagon-type layouts) have been successfully used to realize the output transistors in bulk CMOS processes. This new layout design has the advantages of higher driving/sinking capability, higher ESD robustness, smaller layout area, smaller drain junction capacitance, more symmetrical device structure, but without the peak structure at the finger's end. This area-efficient layout design can be used to realize the devices in both the output buffers and the input ESD protection circuits for submicron CMOS ICs to save silicon area for the high-density and high-speed applications.

References

[1] Baker L et al. EOS/ESD Symposium Proceedings 1989;EOS-11:175.
[2] Vemuru R. Electronics Letters 1992;28:2327.
[3] Daniel S, Krieger G. EOS/ESD Symposium Proceedings 1990;EOS-12:206.
[4] Stricker A, Gloor D, Fichtner W. EOS/ESD Symposium Proceedings 1995;EOS-17:205.
[5] Beebe SG. EOS/ESD Symposium Proceedings 1996;EOS-18:265.
[6] Amerasekera A, Duvvury C ESD in silicon integrated circuits. Chichester: Wiley, 1995. p. 67.
[7] Ker M-D et al. A close-looped electronic device. ROC patent no. 077645, 1996.
[8] Ker M-D, Wu C-Y, Huang C-C, Chen T-Y. Solid-State Electronics 1998;42:1007.
[9] Ker M-D et al. Realization of CMOS devices by hexagon-type layout. ROC patent no. 079834, 1996.
[10] Ker M-D, Wu T-S, Wang K-F N-sided polygonal cell layout for multiple cell transistor. ROC patent no. 076087, 1996.
[11] Ker M-D, Wu T-S. IEDM Technical Digest 1996;889.
[12] Ker M-D, Wu C-Y, Wu T-S. IEEE Transactions on Electron Devices 1997;44:635.