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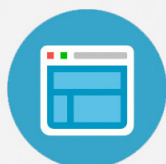
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Properties and thermal stability of chemically vapor deposited W-rich WSi_x thin films*

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The tungsten-rich (Si/W atomic ratio less than 2.0) chemical vapor deposition (CVD)- WSi_x layer was found to be an efficient diffusion barrier against Cu diffusion. In this study, the properties and thermal stability of the W-rich WSi_x films chemically vapor deposited at various deposition temperatures, pressures, and SiH_4/WF_6 reactant gas flow ratios were investigated. With SiH_4/WF_6 flow rates of 6/2 sccm and a total gas pressure of 12 mTorr, the activation energy of the CVD process was determined to be 3.0 kcal/mole, and the film deposited at 250 °C has a Si/W atomic ratio of unity. The WSi_x films have a low residual stress, low electrical resistivity, and excellent step coverage. For the WSi_x layers deposited on Si substrates, the residual stress varies from 7 to 9×10^8 dynes/cm² depending on the deposition temperature. The resistivity of the WSi_x films varies from 200 to 340 $\mu\Omega$ cm; higher deposition temperatures and SiH_4/WF_6 flow ratios resulted in higher film resistivities. The as-deposited amorphous WSi_x layer is thermally stable up to 600 °C; however, crystallization of the deposited film takes place at 650 °C and WSi_x was transformed into WSi_2 phase when the WSi_x/Si structure was thermally annealed at temperatures above 650 °C.

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I. INTRODUCTION

It was found recently that a tungsten-rich (Si/W atomic ratio less than 2.0) chemical vapor deposition (CVD)- WSi_x layer served efficiently as diffusion barrier against Cu diffusion.^{1,2} The thermal stability of Cu/ WSi_x (50 nm)/ $p^+ - n$ junction diodes was found to reach 500 °C; with an *in situ* N_2 plasma treatment on the surface of WSi_x layers, the resultant Cu/ WSiN/WSi_x (50 nm)/ $p^+ - n$ junction diodes were able to retain integrity of their electrical characteristics up to at least 600 °C.² Moreover, the tungsten-rich CVD- WSi_x films were found to have a low residual stress, low electrical resistivity, and excellent step coverage. This indicates that the tungsten-rich CVD- WSi_x films possess great potential in application to Cu metallization system. Thus, a systemic study of tungsten-rich CVD- WSi_x films is vital to their applications in ultralarge scale integration (ULSI) circuits.

Refractory metal silicides have been intensively studied for potential use as interconnection in ULSI circuits.^{3,4} These materials offer good thermal stability and good electrical conductivity. Among them, tungsten silicide (WSi_x) is one of the most promising materials because of its good compatibility with conventional ULSI fabrication processes.⁵⁻²¹ Sputter deposited WSi_x films have been widely used in integrated circuits (ICs) manufacture.^{4,6} In general, the sputter deposited WSi_x used in ICs manufacture has a Si/W atomic

ratio larger than 2.0, and is often referred to as “silicon-rich WSi_x .” The as-sputtered WSi_x films have a resistivity of 600–900 $\mu\Omega$ cm, which decreases to about 50 $\mu\Omega$ cm after annealing at 1000 °C.⁶ However, it is difficult to deposit WSi_x films, with acceptable step coverage, into contact holes of deep subhalf micron dimensions using physical vapor deposition (PVD) method. In contrast, CVD method generally offers superior step coverage of conformal deposition; thus chemically vapor deposited WSi_x (CVD- WSi_x) layer is becoming very attractive in ULSI application.⁵

The first systemic study of CVD- WSi_x , to our knowledge, was done by Brors *et al.*,⁷ they proposed to deposit WSi_x films in a cold wall reactor using SiH_4/WF_6 as reactive gas mixtures and obtained a good quality silicide films with a resistivity as low as 30 $\mu\Omega$ cm after a postdeposition annealing treatment. It was reported that the residual stress in CVD- WSi_x films decreased linearly with increasing silicon content in the WSi_x film.^{2,22} In addition, it was found that the resistivity of as-deposited CVD- WSi_x film increased with increasing deposition temperature.^{7,13,22} Although many studies have been dedicated to the properties and thermal stability of silicon-rich (Si/W atomic ratio larger than 2.0) nonstoichiometric CVD- WSi_x films, little work has been done on the tungsten-rich CVD- WSi_x layers.

In this study, the properties and thermal stability of tungsten-rich nonstoichiometric CVD- WSi_x thin films were systemically investigated. The WSi_x thin layers were depos-

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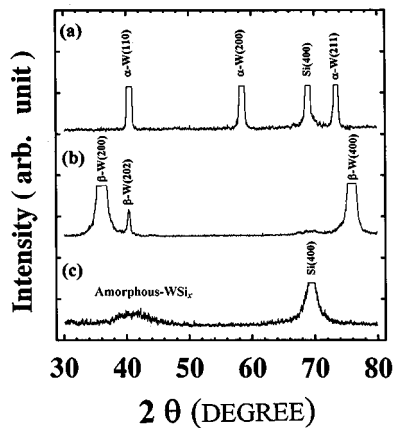


FIG. 1. XRD spectra of WSi_x films deposited on bare Si substrate with SiH₄/WF₆ flow ratio of (a) 0.25, (b) 1.5, and (c) 3.0. The films were deposited at 300 °C with a total gas pressure of 20 mTorr.

ited by low pressure chemical vapor deposition (LPCVD) method using the SiH₄ reduction of WF₆. The properties of CVD-WSi_x layers including crystalline phase, deposition rate, electrical resistivity, residual stress, surface roughness, and step coverage were investigated. The thermal stability of CVD-WSi_x layers was also investigated using various techniques [scanning electron microscopy (SEM), x-ray diffraction (XRD) analyses, Rutherford backscattering spectroscopy (RBS), and sheet resistance measurements]. The results of this study might be useful in multilevel metallization for ULSI circuits.

II. EXPERIMENT

The test samples were fabricated on *n* type, (100)-oriented, 4-in.-diam silicon wafers with 4–7 Ω cm nominal resistivity. After RCA standard cleaning, one group of wafers was thermally oxidized to grow a 500-nm-thick SiO₂ layer. Unpatterned samples of WSi_x/Si and WSi_x/SiO₂/Si structures were then prepared for material analysis. For step coverage study, patterned samples with trenches having aspect ratios ranging from 1 to 4 were also prepared.

The WSi_x layers were deposited by CVD method using SiH₄ reduction of WF₆. Prior to the WSi_x deposition, both the bare Si and SiO₂/Si wafers were dipped in dilute HF (50:1) for 30 s, followed by a rinse in DI water for 3 min and spin dry. The wafers were then loaded into a load-locked cold wall CVD system within 5 min and transferred by a robot arm to the deposition chamber without exposure to the atmosphere. The base pressure of the CVD chamber was 10⁻⁶ Torr. In this study, WSi_x films were chemically vapor deposited from SiH₄/WF₆ gas mixtures with the conditions illustrated as follows: substrate temperature 150–450 °C, total gas pressure 12–20 mTorr, WF₆ flow rate 2 sccm, and SiH₄ flow rate 4–100 sccm.

The properties of the CVD-WSi_x layers including crystalline phase, deposition rate, electrical resistivity, residual stress, surface roughness, and step coverage were investigated. The samples of the WSi_x/Si and WSi_x/SiO₂/Si structures were thermally annealed in N₂ flowing furnace for 30

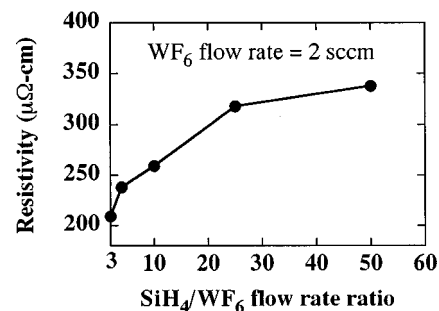


FIG. 2. Resistivity of WSi_x films vs SiH₄/WF₆ flow ratio. The WSi_x films were deposited at 250 °C with a total gas pressure of 12 mTorr and WF₆ flow rate of 2 sccm.

min at a temperature ranging from 400 to 800 °C. The variation of sheet resistance with respect to the annealing temperature was used to monitor the thermal stability. Atomic force microscopy (AFM) was employed to characterize the surface roughness. XRD analysis was used for phase identification. RBS was used to determine the Si/W atomic ratio of WSi_x films and to examine the interdiffusion between W and Si substrate at the WSi_x/Si interface. Moreover, SEM was employed to measure the film thickness and observe the surface morphology as well as the change of microstructure.

III. RESULTS AND DISCUSSION

A. Properties of CVD-WSi_x thin films

1. Effects of SiH₄/WF₆ flow rate

Three different types of film microstructure, α-W phase, β-W phase, and amorphous WSi_x phase, were obtained by the SiH₄ reduction of WF₆ with different SiH₄/WF₆ flow ratio, as revealed by XRD analysis (Fig. 1). At a substrate temperature of 300 °C and with a total gas pressure of 20 mTorr, α-W diffraction peaks were detected for films deposited with SiH₄/WF₆ flow ratio lower than 1.0 [Fig. 1(a)], while β-W peaks were detected for films deposited with SiH₄/WF₆ flow ratio ranging from 1.0 to 1.5 [Fig. 1(b)]. With the SiH₄/WF₆ flow ratio higher than 2, the structure of WSi_x films was eventually amorphous [Fig. 1(c)].

To investigate the effects of SiH₄/WF₆ flow ratio on the resistivity and Si/W atomic ratio of WSi_x films, the CVD

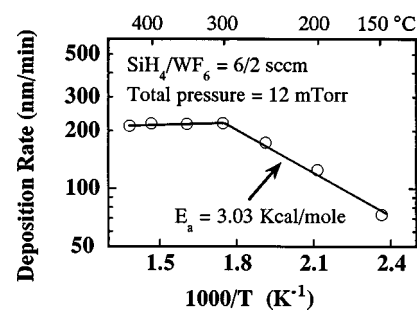


FIG. 3. Deposition rate of WSi_x films vs deposition temperature. The WSi_x films were deposited with a total gas pressure of 12 mTorr and SiH₄/WF₆ flow rates of 6/2 sccm.

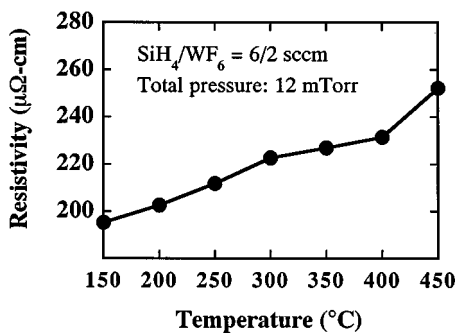


FIG. 4. Resistivity of WSi_x films vs deposition temperature. The WSi_x films were deposited at a total gas pressure of 12 mTorr and SiH_4/WF_6 flow rates of 6/2 sccm.

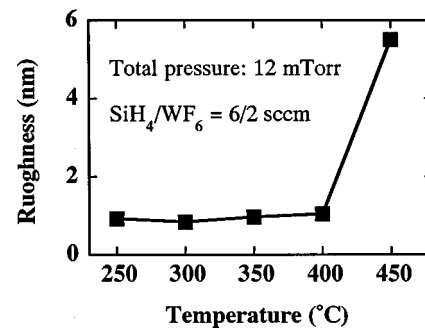


FIG. 6. Surface roughness of as-deposited CVD- WSi_x films vs deposition temperature. The WSi_x films were deposited at a total gas pressure of 12 mTorr and SiH_4/WF_6 flow rates of 6/2 sccm.

process was conducted at a substrate temperature of 250 °C and with a SiH_4 flow rate ranging from 4 to 100 sccm, while keeping the WF_6 flow rate at 2 sccm and the total gas pressure at 12 mTorr. Figure 2 shows the resistivity of CVD- WSi_x films versus SiH_4/WF_6 flow ratio. The resistivity of WSi_x layers increases with increasing flow ratio of SiH_4/WF_6 ; this increase in resistivity is presumably related to an increased amount of Si incorporated in the WSi_x layer. We found that the Si/W atomic ratio in the WSi_x layer increased from 1.0 to 1.3 as the SiH_4/WF_6 flow ratio was increased from 3 to 50, as determined by RBS measurements. Similar results were reported by Clark, although the SiH_4/WF_6 flow ratio ranged from 85 to 315, deposition temperature ranged from 330 to 360 °C and the resultant WSi_x layer was nonstoichiometric silicon-rich ($x > 2$) in his study.²²

2. Deposition temperature effect

The CVD of WSi_x films was conducted at temperatures ranging from 150 to 450 °C with a total gas pressure of 12 mTorr, WF_6 flow rate of 2 sccm, and SiH_4 flow rate of 6 sccm. Figures 3 and 4 show the deposition rate and resistivity of WSi_x films versus deposition temperature. Below 300 °C, the surface reaction might be the rate limiting process, and the activation energy of the CVD process was determined to be 3.0 kcal/mole. At temperatures above 300 °C, the deposition rate was independent of the substrate temperature; as a result, the process was possibly controlled by mass

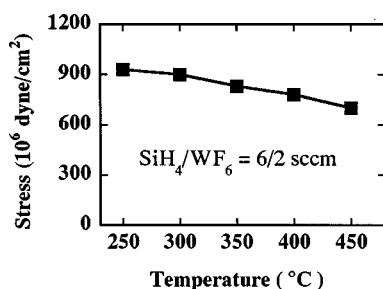


FIG. 5. Residual stress in as-deposited WSi_x films as a function of deposition temperature. The WSi_x films were deposited at a total gas pressure of 12 mTorr and SiH_4/WF_6 flow rates of 6/2 sccm.

transfer mechanism. Thermodynamically, silane is an unstable compound and will decompose into silicon and hydrogen. Since the decomposition of SiH_4 is a thermally activated process, the amount of Si incorporated into WSi_x films will increase with increasing deposition temperature. It was reported that the resistivity of chemically vapor deposited amorphous WSi_x films increased with increasing Si content in the as-deposited films.^{20,22} The reported observation is thus consistent with the results of this work that the increase in deposition temperature resulted in an increase in resistivity for the as-deposited WSi_x films.

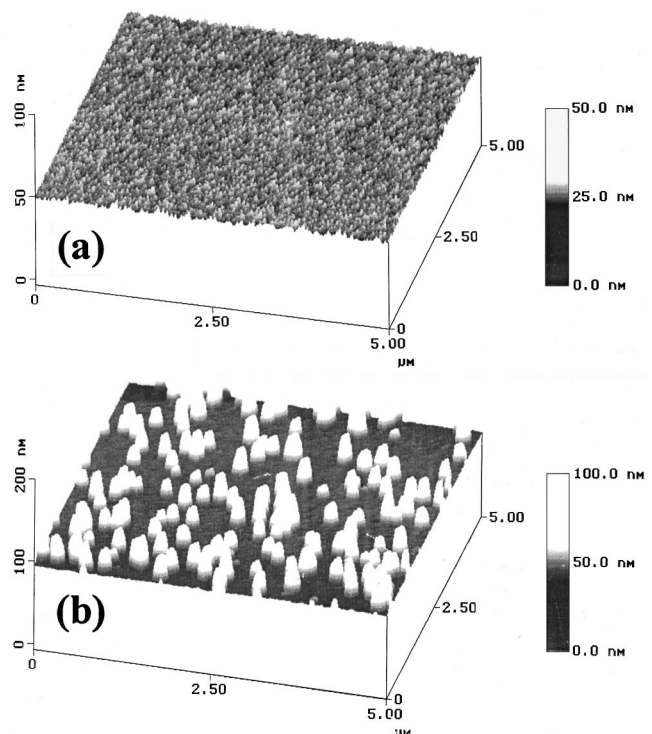


FIG. 7. AFM micrographs for WSi_x films deposited at substrate temperature of (a) 250 and (b) 450 °C.

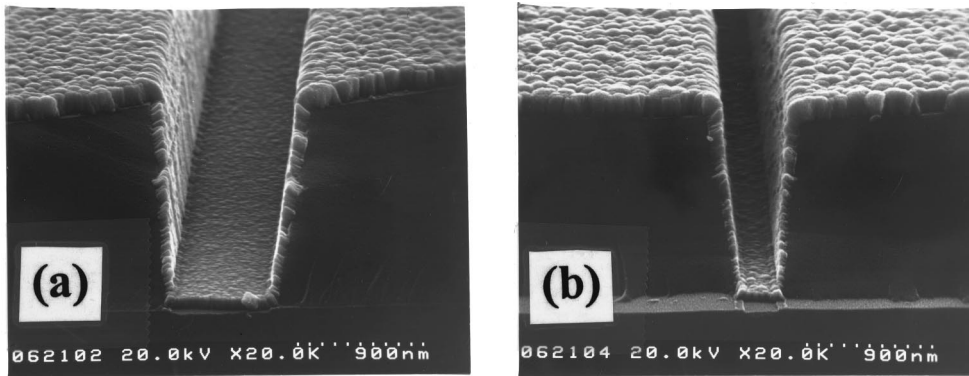


Fig. 8. Step coverage of WSi_x films deposited on submicron trenches with aspect ratio of (a) 2.0 and (b) 4.0.

3. Residual stress

The residual stress was measured using a Tencor's FLX-2320 system. The value of stress was determined according to Eq. (1),

$$\sigma = \frac{E}{6(1-\nu)} \frac{t^2}{d} \left[\frac{1}{R} - \frac{1}{R_0} \right], \quad (1)$$

where σ is the stress, E is the Young's modulus of Si substrate, ν is the Poisson ratio of Si substrate, t is the thickness of WSi_x film, d is the thickness of Si substrate, while R_0 and R are the radii of curvature of the substrate before and after the film deposition, respectively.

Figure 5 shows the residual stress in as-deposited WSi_x films versus deposition temperature. The stress decreases slightly with increasing deposition temperature. This is presumably due to larger amount of Si incorporated in the WSi_x layer at higher deposition temperatures. This result agrees with the reported work in literature that the stress of WSi_x is influenced by the Si/W atomic ratio in the WSi_x film.^{22,23}

It should be noted that a good adherence can be obtained for the CVD- WSi_x layer deposited on Si substrate at temperatures higher than 200 °C. Peeling of WSi_x layer on Si substrate was found for the WSi_x layer deposited at 150 °C to a thickness of 220 nm. Moreover, peeling of WSi_x layer on SiO_2 was found for the WSi_x layer deposited at 200 °C.

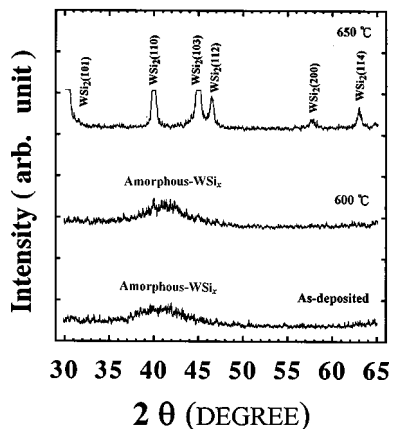


Fig. 9. XRD spectra for as-deposited and thermally annealed WSi_x (220 nm)/Si samples.

4. Surface roughness

The surface roughness of CVD- WSi_x films was measured using AFM on unpatterned WSi_x/Si samples. Figure 6 shows the surface roughness versus deposition temperature for as-deposited CVD- WSi_x layers. A fairly smooth surface was obtained for the WSi_x films deposited at temperatures between 250 and 400 °C, as analyzed using AFM [Fig. 7(a)]. However, the surface roughness increased drastically for the films deposited at temperatures above 450 °C [Fig. 7(b)]. Particles generated by gas phase nucleation might lead to the surface roughness. It has been reported that the gas phase nucleation occurred at temperatures above 400 °C and with SiH_4/WF_6 flow ratio higher than unity. Moreover, it was found that the particle generation rate increased with increasing deposition pressure.²⁴

5. Step coverage

A highly conformal deposition of CVD- WSi_x films was obtained. Figure 8 shows the WSi_x films deposited on submicron trenches with aspect ratios of 2 and 4 using the deposition condition illustrated as follows: substrate temperature 250 °C, total gas pressure 12 mTorr, WF_6 flow rate 2 sccm, and SiH_4 flow rate 6 sccm. We referred to this condition as "standard deposition condition" hereafter.

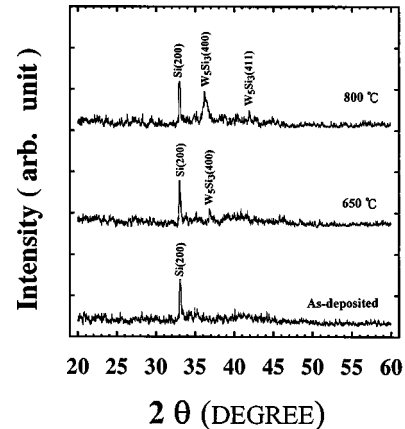


Fig. 10. XRD spectra for as-deposited and thermally annealed WSi_x (50 nm)/ SiO_2 /Si samples.

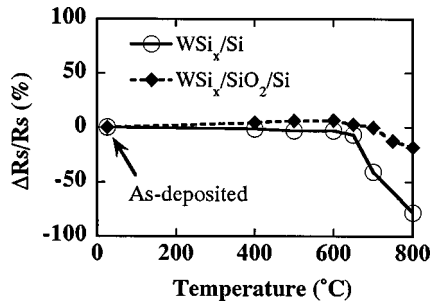


FIG. 11. Sheet resistance change vs annealing temperature for WSi_x/Si and WSi_x/SiO₂/Si samples.

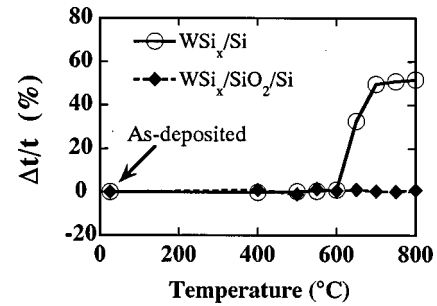


FIG. 12. Thickness change of WSi_x layer vs annealing temperature for WSi_x/Si and WSi_x/SiO₂/Si samples.

B. Thermal stability of CVD-WSi_x films

The thermal stability of the WSi_x layers, deposited using the standard deposition condition on bare Si and SiO₂/Si substrates to produce WSi_x(220 nm)/Si and WSi_x(50 nm)/SiO₂/Si structures, respectively, was investigated using the techniques of XRD, RBS, SEM, and the sheet resistance measurement.

1. XRD analyses

For WSi_x(220 nm)/Si samples, the as-deposited WSi_x films are amorphous, as indicated by XRD analysis shown in Fig. 9. A broad peak was present clearly at 2θ angle of 39° – 43° . Since at least six diffraction peaks available to various phases (110- α -W, 330-W₅Si₃, 202-W₅Si₃, 420-W₅Si₃, 411-W₅Si₃, and 110-WSi₂) are located within this 2θ range, it is not possible to draw any conclusion from the

position of this broad peak. After annealing at 600°C , the WSi_x layer retained its original amorphous phase. However, a number of diffraction peaks belonging to WSi₂ phase appeared after the sample was annealed at 650°C . The presence of WSi₂ phase indicates that reaction occurred at the WSi_x/Si interface.

XRD spectra for as-deposited and thermally annealed WSi_x(50 nm)/SiO₂/Si samples are illustrated in Fig. 10. After annealing at 650°C , a very weak peak of W₅Si₃ phase appeared at 2θ angle of about 37° , and the intensity of the W₅Si₃ peaks increased with increasing annealing temperature. However, no peak of WSi₂ phase was observed even after annealing at 800°C . This different behavior between the WSi_x/Si and WSi_x/SiO₂/Si structures is apparently related to the presence of SiO₂ layer in the latter structure. The SiO₂ layer prevented out diffusion of Si atoms from the sub-

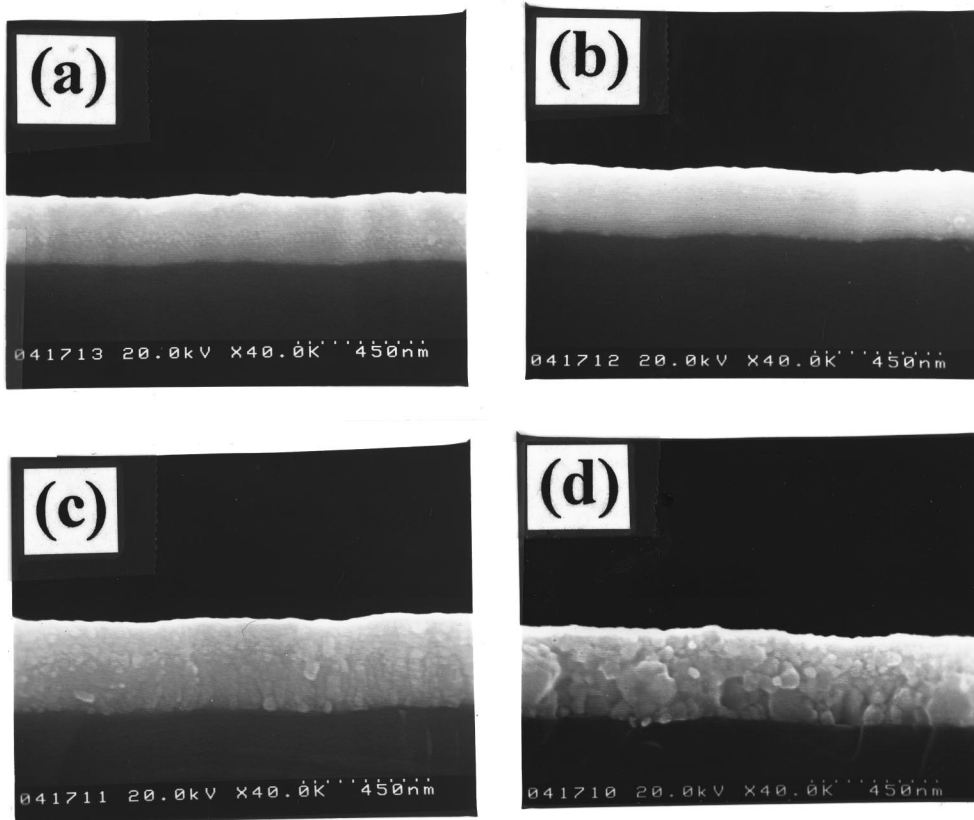


FIG. 13. Cross-sectional SEM micrographs for WSi_x/Si samples (a) as-deposited, and thermally annealed at (b) 600, (c) 650, and (d) 800 °C.

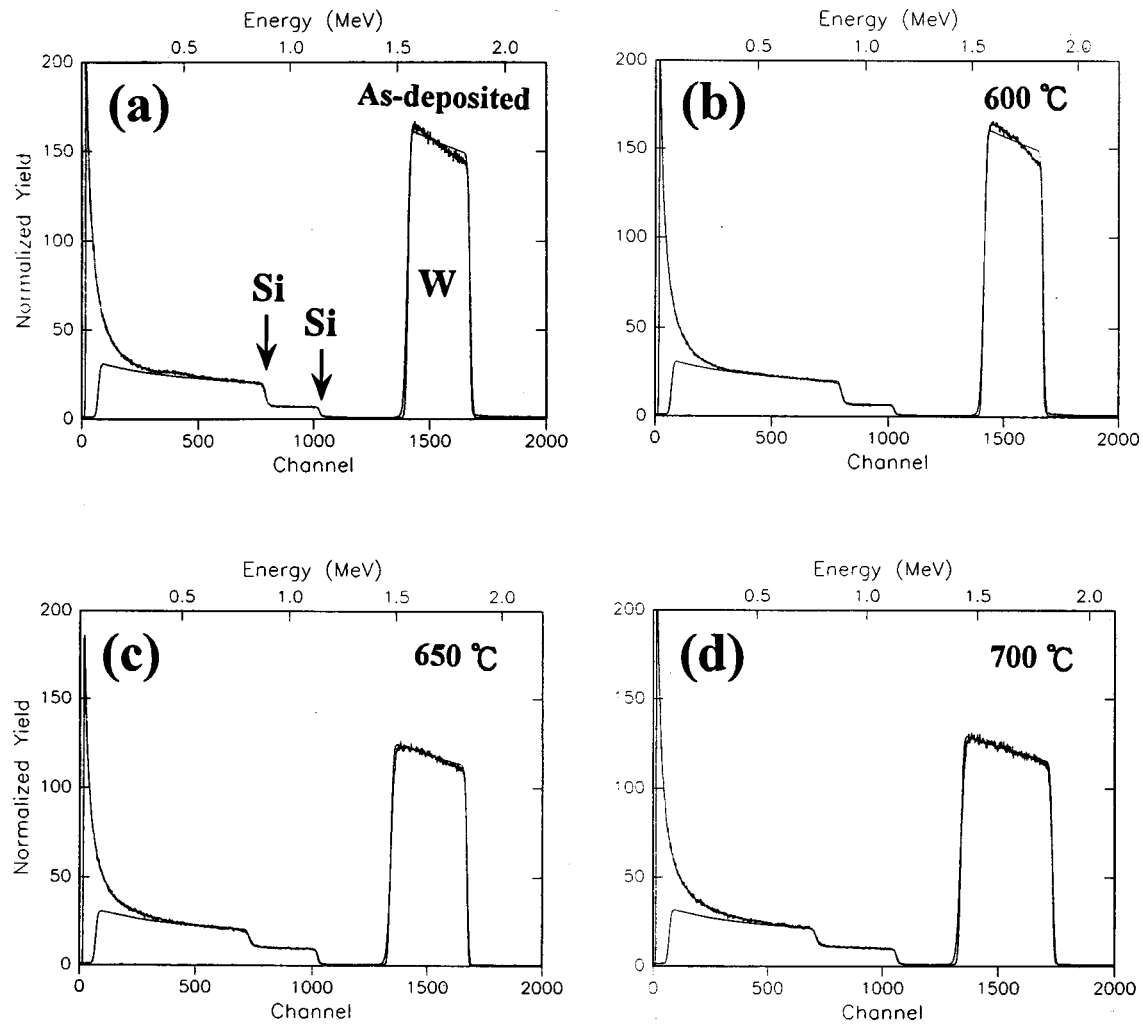


FIG. 14. Rutherford backscattering spectra for WSi_x/Si samples (a) as-deposited, and thermally annealed at (b) 600, (c) 650, and (d) 700 °C.

strate to the WSi_x layer; thus, the Si deficient WSi_x layer was not able to form stable WSi_2 phase during thermal annealing. Moreover, since no signal of WSi_2 phase was observed for the thermally annealed $\text{WSi}_x/\text{SiO}_2/\text{Si}$ sample, we excluded the possibility that the as-deposited WSi_x film contained amorphous WSi_2 . Therefore, we conclude that the as-deposited WSi_x is a mixture of amorphous phase of W and Si, together with possible existence of amorphous phase of W_5Si_3 .⁶

2. Sheet resistance measurements

The sheet resistance change of annealed samples, normalized to the as-deposited sheet resistance value, is denoted as $\Delta R_s/R_s$ (%) and defined as follows:

$$\frac{\Delta R_s}{R_s} (\%) = \left[\frac{R_{s \text{ after anneal}} - R_{s \text{ as-deposited}}}{R_{s \text{ as-deposited}}} \right] \times 100\%. \quad (2)$$

Figure 11 shows the sheet resistance change versus annealing temperature for the WSi_x/Si and $\text{WSi}_x/\text{SiO}_2/\text{Si}$ samples, in which the WSi_x layers were deposited using the standard deposition condition. The sheet resistance of WSi_x/Si remained constant up to 600 °C, implying that the

amorphous structure of WSi_x film remained unchanged, as confirmed by XRD patterns shown in Fig. 9. With the samples annealed at temperatures above 650 °C, the sheet resistance decreased rapidly with increasing annealing temperature. This is attributed to the formation of the low resistivity WSi_2 phase at temperatures above 650 °C (Fig. 9). For $\text{WSi}_x(50 \text{ nm})/\text{SiO}_2/\text{Si}$ samples, the sheet resistance also showed decreasing trend after annealing at temperatures above 650 °C; however, the extent of decrease is much smaller than the WSi_x/Si samples. The decrease in sheet resistance was presumably due to crystallization and grain growth of W_5Si_3 phase (Fig. 10).

3. Thickness change of WSi_x layers

The thermal annealing was found to result in the thickness change of WSi_x layers for WSi_x/Si samples. The thickness change normalized to the as-deposited thickness is denoted as $\Delta t/t$ (%) and defined as follows:

$$\frac{\Delta t}{t} (\%) = \left[\frac{t_{\text{after anneal}} - t_{\text{as-deposited}}}{t_{\text{as-deposited}}} \right] \times 100\%, \quad (3)$$

where t is the thickness of WSi_x layers.

Figure 12 shows the thickness change of WSi_x layers for the WSi_x/Si and $WSi_x/SiO_2/Si$ samples after annealing at various temperatures. The thickness of WSi_x layers for WSi_x/Si samples remained constant after annealing at temperatures up to 600 °C; however, the thickness made a significant increase at temperatures above 600 °C and the normalized increase finally reached a saturated value of about 50% when the sample was annealed at temperatures above 700 °C. This is consistent with the results of XRD analysis (Fig. 9) and sheet resistance measurements (Fig. 11) that WSi_2 phase was formed at temperatures above 600 °C. For $WSi_x/SiO_2/Si$ samples, the thickness of WSi_x layers showed no obvious change after thermal annealing at temperatures up to 800 °C. Figure 13 shows the cross sectional SEM micrographs for WSi_x/Si samples before and after thermal annealing. The increase in thickness of WSi_x layers was clearly observed for WSi_x/Si samples annealed at temperatures above 650 °C. Moreover, the amorphous phase of the as-deposited WSi_x layer became a grain-like structure, presumably related to the WSi_2 grains.

4. RBS analyses

The observed spectra from 2.0 MeV He^+ RBS measurements for the as-deposited and thermally annealed WSi_x/Si samples are illustrated in Fig. 14. The as-deposited sample exhibits one RBS peak of channeling energies relating to W in the WSi_x layer, and two edges which relate to, respectively, the Si in the WSi_x layer (at about 1.12 MeV) and the Si substrate (at about 0.88 MeV) [Fig. 14(a)]. After annealing at 600 °C, no obvious change in the RBS spectrum was observed [Fig. 14(b)]. The Si/W atomic ratio of as-deposited WSi_x layers was determined to be 1.0 and remained unchanged after annealing at 600 °C. This suggests that the WSi_x/Si structure remained stable up to at least 600 °C. After annealing at 650 °C, the width of the W peak increased, indicating an increase in thickness of the W containing layer [Fig. 14(c)]. Upon annealing at 700 °C, the width of the W peak increased to about 1.5 times the original width [Fig. 14(d)]. This is consistent with our previous results of the increase in the WSi_x thickness shown in Fig. 12. The Si/W atomic ratio was determined to be 66/34 and a small increase in Si peak intensity at backing energy of 1.12 MeV was also observed, indicating the increase of Si/W atomic ratio for the WSi_x layer. This clearly indicates the transformation of WSi_x into WSi_2 phase.

IV. SUMMARY

The properties and thermal stability of W-rich CVD- WSi_x thin films were investigated. We found that the WSi_x layers have a low stress, low electrical resistivity, and excellent step coverage. For WSi_x layers deposited on Si substrates, the stress varies from 7 to 9×10^8 dynes/cm² depending on the deposition temperature. The resistivity of the WSi_x films varies from 200 to 340 $\mu\Omega$ cm; higher deposition temperatures

and SiH_4/WF_6 flow ratios resulted in higher film resistivities. With SiH_4/WF_6 flow rates of 6/2 sccm and a total gas pressure of 12 mTorr, the activation energy of the CVD process was determined to be 3.0 kcal/mole, and the WSi_x film deposited at a temperature of 250 °C has a Si/W atomic ratio of unity. As for the thermal stability of CVD- WSi_x films, we found that the WSi_x/Si contact system is thermally stable up to at least 600 °C. However, WSi_x was transformed into WSi_2 phase when the WSi_x/Si structure was thermally annealed at temperatures above 650 °C.

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- ¹M. T. Wang, Y. C. Lin, J. Y. Lee, C. C. Wang, and M. C. Chen, J. Electrochem. Soc. (to be published).
- ²M. T. Wang, Y. C. Lin, J. Y. Lee, C. C. Wang, and M. C. Chen (unpublished).
- ³T. P. Chow and A. J. Steckl, IEEE Trans. Electron Devices **ED-30**, 1480 (1983).
- ⁴S. P. Murarka, J. Vac. Sci. Technol. **17**, 775 (1980).
- ⁵J. E. J. Schmitz, *Chemical Vapor Deposition of Tungsten and Tungsten Silicides for VLSI/ULSI Applications* (Noyes, Park Ridge, NJ, 1992), pp. 171–208.
- ⁶S. R. Wilson, C. J. Tracy, and J. L. Freeman, Jr., *Handbook of Multilevel Metallization for Integrated Circuits: Materials, Technology, and Applications* (Noyes, Park Ridge, NJ, 1993), pp. 53–55.
- ⁷D. L. Brors, J. A. Fair, K. A. Monnig, and K. C. Saraswat, Solid State Technol. **26**, 183 (1983).
- ⁸M. Suzuki, N. Kobayashi, and K. Mukai, *Tungsten and Other Advanced Metals for VLSI/ULSI Applications V*, edited by S. S. Wang and S. Furukawa (Materials Research Society, Pittsburgh, PA, 1990), pp. 259–265.
- ⁹D. L. Brors, J. A. Fair, and K. Monnig, Semiconductor International, May 1984 (unpublished), p. 82.
- ¹⁰S. Sachdev and R. Castellano, Semiconductor International, May 1985 (unpublished), p. 306.
- ¹¹R. Toge, J. Appl. Phys. **59**, 3582 (1986).
- ¹²M. Kottke, F. Pintchovski, T. R. White, and P. J. Tobin, J. Appl. Phys. **60**, 2835 (1986).
- ¹³Y. Shioya, T. Itoh, I. Kobayashi, and M. Maeda, J. Electrochem. Soc. **133**, 1475 (1986).
- ¹⁴Y. Shioya and M. Maeda, J. Appl. Phys. **60**, 327 (1986).
- ¹⁵C. Bernard, R. Madar, and Y. Pauleau, Semicond. Sci. Technol. **32**, 79 (1989).
- ¹⁶K. C. Saraswat, D. L. Brors, J. A. Fair, K. A. Monnig, and R. Beyers, IEEE Trans. Electron Devices **ED-30**, 1497 (1983).
- ¹⁷D. K. Sadana, A. E. Morgan, M. H. Norcott, and S. Naik, J. Appl. Phys. **62**, 2830 (1987).
- ¹⁸D. Dobkin, L. Bartholomew, G. McDaniel, and J. DeDontney, J. Electrochem. Soc. **137**, 1623 (1990).
- ¹⁹M. Suzuki, N. Kobayashi, K. Mukai, and S. Kondo, J. Electrochem. Soc. **137**, 3213 (1990).
- ²⁰J. H. Sone and H. J. Kim, in *Advanced Metallization and Processing for Semiconductor Devices and Circuits*, edited by A. Katz, S. P. Murarka, Y. I. Nissim, and James M. E. Harper (Materials Research Society, Pittsburgh, PA, 1990), Vol. 260, pp. 621–626.
- ²¹N. Thomas, A. M. Dutron, C. Vahlas, C. Bernard, and R. Madar, J. Electrochem. Soc. **142**, 1608 (1995).
- ²²T. E. Clark, J. Vac. Sci. Technol. B **6**, 1678 (1988).
- ²³Y. Shioya, T. Itoh, S. Inoue, and M. Maeda, J. Appl. Phys. **58**, 4194 (1985).
- ²⁴E. J. McInerney, T. W. Mountsier, B. L. Chin, and E. K. Broadbent, J. Vac. Sci. Technol. B **11**, 734 (1993).