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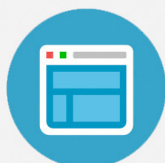
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Formation of silicided shallow p^+n junctions by BF_2^+ implantation into thin amorphous-Si or Ni/amorphous-Si films on Si substrates and subsequent Ni silicidation

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The process scheme that forms NiSi-silicided shallow p^+n junctions by BF_2^+ implantation into thin amorphous-Si (a-Si) or Ni/a-Si films on Si substrates and subsequent Ni silicidation has been studied. As for the scheme using a-Si as an implantation barrier, an NiSi-silicided junction with a leakage of about 0.7 nA/cm^2 at -5 V is obtained by the sample Ni silicided at 700 °C for 30 min. The implantation energy and the crystallinity of the deposited Si films after annealing would greatly affect the junctions formed at various temperatures, attributable to different implantation effects and boron depth profile. However, the junctions formed by rapid thermal processing or high implant energy are considerably degraded at 800 °C, attributable to anomalous Ni penetration into the Si substrate with the further silicidation of NiSi into $NiSi_2$. On the other hand, the specimens with Ni/a-Si as an implantation barrier sustain few defects, thus significantly suppressing the junction degradation at 800 °C. However, the formed junctions are worse than those by the former scheme, mainly due to lower dopant drive-in efficiency. © *1999 American Vacuum Society.*
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I. INTRODUCTION

With the progress of the ultralarge-scale-integration (ULSI) technology, the metal-oxide-semiconductor field-effect transistor (MOSFET) channel length has been scaled down to deep submicron dimensions. Hence, a concomitant reduction in source/drain junction depth is required to minimize short channel effects.[1] Moreover, metal silicides can be used to reduce the parasitic resistance in LSI circuits, thus enhancing the performance of deep submicron complementary metal-oxide-semiconductor (CMOS) devices. The self-aligned-silicide (salicide) technology has become an essential part of the fabrication process for recent ultrahigh-speed CMOS logic LSI circuits.[2] Titanium silicide ($TiSi_2$) is used exclusively as the material for this purpose.[3–6] However, the sheet resistance of $TiSi_2$ formed at annealing temperatures lower than 800 °C is relatively high because of the C49 structure.[7] In addition, the sheet resistance of a $TiSi_2$ line increases as it is made narrower.[8]

Shallow p^+n junctions were conventionally difficult to be realized in part ascribed to the rapid anomalous diffusion of boron in Si.[9] Several methods have been proposed to form shallow junctions, such as very-low-energy boron implantation, gas immersion laser doping, and so on.[10,11] However, a high-temperature $TiSi_2$ process would further deepen the junction. In addition, in terms of the salicide technology, when silicide is formed on source/drain regions, a portion of the heavily doped junction is consumed as the silicidation proceeds. As the junction depth is reduced, the variation in the amount of Si consumed by the silicide makes it increasingly difficult to achieve the proper junction depth.[12] Though the $CoSi_2$ process can achieve small sheet resistance at a low temperature as 700 °C, the consumed Si is significant. The Si consumption is about 1.04 Å for 1 Å $CoSi_2$ (3.6 Å Si for 1 Å Co) and is about 0.9 Å for 1 Å $TiSi_2$ (2.2 Å Si for 1 Å Ti).[13]

Therefore, new schemes should be employed to form silicided shallow junctions. Excellent silicided shallow junctions have been prepared by implanting dopant into thin metal or metal silicide layers and then driving the dopant into the Si substrate.[14–17] However, some inherent problems occur when these schemes are used, such as poor drive-in efficiency, difficult process control, and so on.[17–19] By implanting the dopant into thin polycrystalline-Si (poly-Si) films, good junctions can be formed without the above problems.[19–22] Devices made by this scheme have been described previously.[20] However, subsequent silicidation may affect the resultant junction characteristics, especially for p^+n junctions heavily doped by boron.[21] On the other hand, nickel–monosilicide (NiSi) has a resistivity of about 20 $\mu\Omega$ cm at annealing temperatures below 600 °C with a Si consumption of only about 0.82 Å for 1 Å NiSi (only 1.8 Å Si for 1 Å Ni).[13] In addition, the silicidation of Ni has good resistance to bridging between the gate and the source/drain.[23] Hence, NiSi silicides may be a proper material for low-temperature processing. Several articles have previously reported the applications of NiSi technology for deep submicron devices.[23–25]

In this study, the scheme that forms Ni-silicided shallow

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p^+n junctions by BF_2^+ implantation into thin amorphous-Si (a-Si) or Ni/a-Si films on Si substrates and subsequent Ni silicidation has been investigated. Various thermal cycles and process conditions have been examined to clarify their effects on the resultant silicided shallow junctions.

II. EXPERIMENT PROCEDURE

Phosphorus-doped n-type Si wafers, (100)-oriented, 0.55–1.1 Ω cm, were first chemically cleaned by using the standard RCA process. A 500-nm-thick thermally grown oxide was used for patterning the active regions of diodes as well as for an etch mask for selective etching. The size of the diodes was $1000\times 1000\ \mu m^2$. After the patterning, 150-nm-thick films of a-Si were deposited onto the wafers by using a low-pressure-chemical-vapor-deposition (LPCVD) system at 550 °C. Furthermore, an additional patterning was done to etch off the a-Si films on the field oxide for performing the salicide process.

Some of the postpatterned samples were then BF_2^+ implanted at 25 or 75 keV to a dose of $5\times 10^{15}\ cm^{-2}$, referred to as the implant through amorphous-silicon (ITA) samples. This reflects the usage of the thin a-Si films as an implantation barrier. After implantation, the specimens were covered with a Ni film of about 30 nm thickness using an electron-gun evaporation system with a base pressure better than 1.5×10^{-6} Torr. Immediately, an a-Si capping layer of 5 nm thickness was deposited to prevent Ni oxidation during annealing. A two-step annealing process, by rapid thermal annealing (RTA) for 30 s or conventional furnace annealing (CFA) for 30 min in an N_2 ambient, was used for the salicide technique and dopant drive-in. The first step annealing was at 400 °C, and then the unreacted Ni on the field oxide was chemically removed by an etchant which consists of a 1:1:6 volume mixture of HCl, H_2O_2, and H_2O, used at 55 °C. The second step annealing was performed at 500–800 °C for dopant drive-in and better silicide crystallinity. The reaction of thin Ni films with Si would form NiSi when the annealing temperature is higher than 350 °C. And, the NiSi would be further transformed into $NiSi_2$ when an annealing temperature above 750 °C is undertaken.[26] The reported sheet resistivity for NiSi was about 20–30 $\mu\Omega$ cm, but that for $NiSi_2$ was about 35–60 $\mu\Omega$ cm.[26] The Si consumption is about 1.02 Å for 1 Å $NiSi_2$ (3.7 Å Si for 1 Å Ni).[13]

Part of the former postpatterned samples were first covered by a thin Ni film with a capping layer, and then BF_2^+ implanted at 25 or 75 keV to a dose of $5\times 10^{15}\ cm^{-2}$, called the implant through metal/amorphous-silicon (ITMA) samples. This reflects the usage of the thin Ni films and the underlying a-Si films as an implantation barrier. Similarly, a two-step annealing process was done after the implantation. It is noted that the technology discussed here is not a fully salicide process, since an extra mask was required for pattern definition of the a-Si films. This scheme would become a substantial salicide process, when a selective Si technique growth is used.

The junction depth beneath the silicides was determined by conducting a spreading-resistance-probe (SRP) measurement. A JEOL-2000FX scanning transmission electron microscope (STEM) operating at 160 kV was used to examine the crystallinity of the silicide films. The electrical characteristics of the silicided junctions were achieved by utilizing an HP 4145B semiconductor parametric analyzer. At least ten diodes for each sample were taken to attain the average values. The average leakage current density of a junction is defined as the leakage at −5 V and at 25 °C.

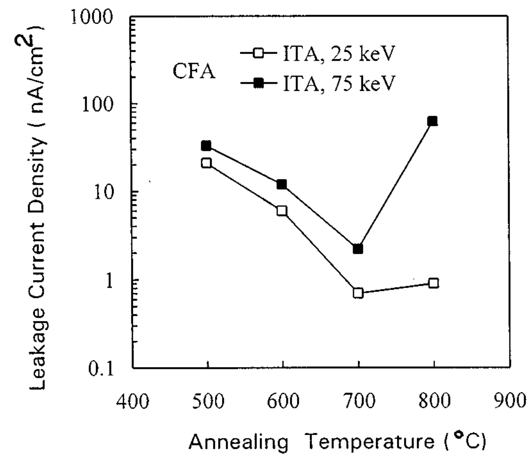

FIG. 1. Dependence of leakage current density on annealing temperature for the 25 and 75 keV implanted ITA samples Ni silicided by CFA processing.

III. RESULTS AND DISCUSSION

When the ITA scheme was used, the resultant silicided junctions exhibited good characteristics. Figure 1 shows the dependence of the leakage current density on the annealing temperature for the 25 and 75 keV implanted ITA samples Ni silicided by CFA processing. The forward ideality factor, n, corresponding to Fig. 1 is shown in Fig. 2. From the TRIM (transport of ion in matter) program simulation, the 25 keV implantation led to a distribution profile with most of the implanted dopant being confined in the thin a-Si films. The 75 keV implantation would result in considerable dopant penetration into the Si substrate. Figure 3 shows the TRIM

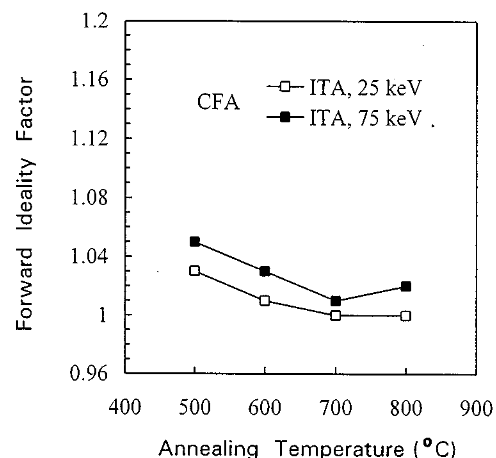

FIG. 2. Forward ideality factor corresponding to Fig. 1.

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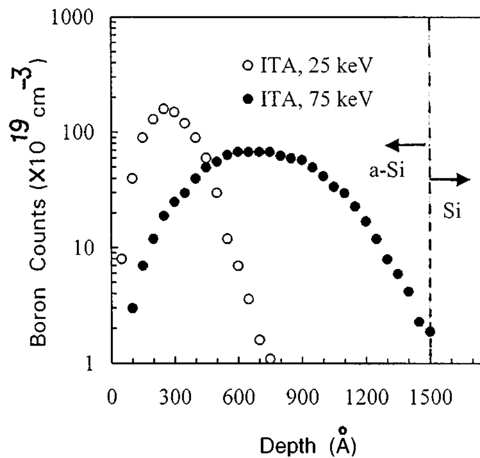

FIG. 3. TRIM simulation results for the BF_2^+ implantation into thin a-Si (150 nm) films on an Si substrate. The implantation is done at an energy of 25 or 75 keV to a dose of $5\times10^{15}\,cm^{-2}$.

simulation results for the ITA samples implanted at 25 and 75 keV to a dose of $5\times10^{15}\,cm^{-2}$, respectively. For the 25 keV implant sample, a silicided junction with a leakage of about $0.7\,nA/cm^2$ and an n value of about 1.00 was obtained by CFA at 700 °C, and a junction leakage of about 6 nA/cm^2 can be achieved even at 600 °C.

Moreover, better junctions were obtained with increasing CFA temperature until 700 °C, attributable to increased dopant activation, the dopant drive-in from the stacked silicide/poly-Si layer, the better defect recovery, and the better crystallinity of the deposited Si films after annealing. Figure 4 shows the boron concentration profile for the 25 and 75 keV implanted ITA samples annealed at 500 and 700 °C, respectively. In terms of the 500 °C annealing, the junctions formed by the 25 keV implanted samples were still within the a-Si films, and thus the junction leakage was considerable due to poor crystallinity of the implanted a-Si films. In addition, for the 75 keV implanted samples, the junctions were formed near the a-Si/Si(100) interface. The resultant junction leakage was even larger than that for the 25 keV implanted specimens due to the higher number of substrate defects and the worse crystallinity of the 75 keV implanted a-Si films. On the other hand, the a-Si film would be transformed into the poly-Si structure at temperatures higher than about 600 °C. Hence, the junctions formed at 600 °C were further improved due to increased dopant activation and better crystallinity of deposited Si films after annealing. A grain size of about 0.3 μm was observed. On the other hand, for the 700 °C annealing, the resultantly electrical junction depths for the 25 and 75 keV implanted samples were about 0.02 and 0.04 μm below the poly-Si/Si(100) interface. As a result, the junctions formed at 700 °C showed good characteristics. Moreover, the 25 keV implant samples resulted in a smaller junction leakage than the 75 keV implant ones due to lower implant-induced damage in the Si substrate. As a result, a lower implant energy is more helpful to low-temperature junction formation by this scheme.

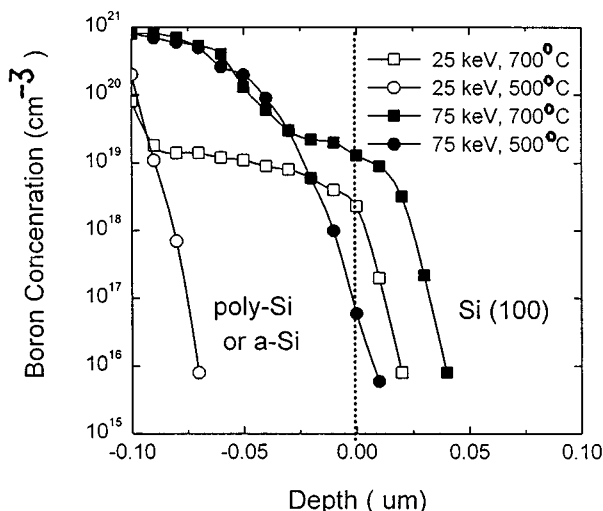

FIG. 4. Depth profiles of boron concentration for the 25 and 75 keV implanted samples annealed at 500 and 700 °C, respectively.

However, from Fig. 1, a significant increase of leakage from 2 to about $80\,nA/cm^2$ was found for the 75 keV implant samples, when the annealing temperature was raised from 700 to 800 °C. For a nonsilicided ITA sample, the dopant activation, the dopant drive-in, and the damage annihilation would be improved with increasing the annealing temperature. Accordingly, the junction deterioration for the 75 keV implant ITA samples Ni silicided at 800 °C was primarily ascribed to the further silicidation of NiSi into $NiSi_2$ at this temperature. Anomalous dopant diffusion in Si was reported to occur during annealing due to interstitial defects.[27] In addition, the residual poly-Si thickness after the $NiSi_2$ formation was reduced from about 100 to about 40 nm, and the grain size of the poly-Si was examined to be about 50 nm at 800 °C. Anomalous Ni diffusion through the poly-Si layer, directly via the grain boundaries, would thus probably occur during the silicidation of NiSi into $NiSi_2$. Accordingly, the Ni penetration into the Si substrate would be further caused due to the presence of implant-induced defects in the Si substrate. Since the silicide formed at temperatures below 700 °C was still kept to be the NiSi structure formed at 400 °C of the first step annealing, no further silicidation and thus no anomalous Ni penetration would be induced at temperatures below 700 °C. Owing to more defects in Si substrates, the 75 keV implant ITA samples Ni silicided at 800 °C would result in much more serious junction deterioration than the 25 keV implant ones, as indicated in Figs. 1 and 2.

Moreover, as the ITA samples were Ni silicided by RTA processing, the results were not so good as those by CFA. Figure 5 shows the dependence of leakage current density on the annealing temperature for the 25 and 75 keV implant ITA samples Ni silicided by RTA processing. The forward ideality factor, n, corresponding to Fig. 5 is shown in Fig. 6. Rapid thermal processing was reported to effectively reduce the dopant diffusion, activate the dopant, and annihilate the implantation defects.[28,29] However, by this ITA method, the dopant for forming junctions, which was schemed to out dif-

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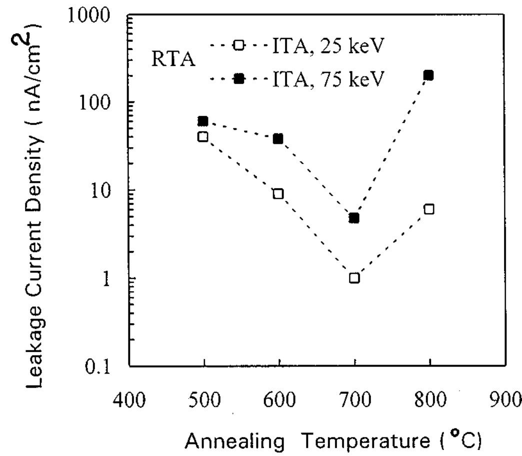

FIG. 5. Dependence of leakage current density on annealing temperature for the 25 and 75 keV implanted ITA samples Ni silicided by RTA processing.

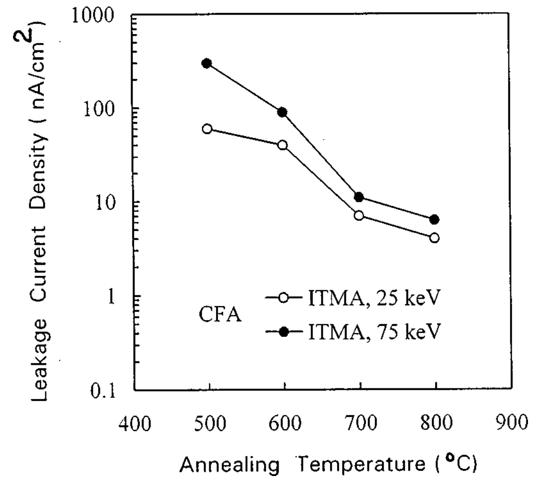

FIG. 7. Dependence of leakage current density on annealing temperature for the 25 and 75 keV implanted ITMA samples treated by CFA processing.

fuse from the stack NiSi/poly-Si layer, would be reduced due to the short annealing time. The dopants, boron, and arsenic, were reported to be forced out of the Ni silicides during silicidation, in contrast to the dopant absorption for the Ti silicidation.[22,23] As a result, the resultant junctions were still improved with increasing the RTA temperature until 700 °C, due to increased dopant activation and better crystallinity of the deposited Si films after annealing. For the 25 keV implant samples, a silicided junction with a leakage of about 1 nA/cm^2 and an n value of about 1.01 was obtained by RTA at 700 °C, and a junction leakage of about 9 nA/cm^2 can be achieved at 600 °C. On the other hand, the further silicidation of NiSi into $NiSi_2$ occurred when the annealing temperature was raised to 800 °C, which would confine more dopant within the $NiSi_2$ silicide. And, RTA could not provide sufficient time to efficiently drive the dopant out of the $NiSi_2$ silicides. A junction with smaller dopant concentration would lead to a larger depletion width at reverse bias. As a result, for a 800 °C anneal, RTA led to more serious junction degradation caused by anomalous Ni penetration than CFA, which can be inspected from Figs. 1 and 5.

On the other hand, the ITMA scheme was intended to develop an even lower-temperature process. By implanting the dopant into the stacked Ni/a-Si layer, little damage was caused in the Si substrate. Figure 7 shows the dependence of leakage current density on the annealing temperature for the 25 and 75 keV implant ITMA samples treated by CFA processing. The forward ideality factor, n, corresponding to Fig. 7 is shown in Fig. 8. From the TRIM program simulation, the 25 keV implantation led to a distribution profile with most of the implanted dopant being confined in the thin Ni films. The 75 keV implantation would result in considerable dopant penetration into the a-Si film, but the resulting dopant penetration into the Si substrate was small. For the 25 keV implanted ITMA sample, a junction with a leakage of about 7 nA/cm^2 and an n value of about 1.02 was formed by CFA at 700 °C. The dopant was mainly implanted into the thin Ni films of the stacked Ni/a-Si implantation barrier. Hence, as compared to the ITA scheme, the ITMA method produced a shallower boron implant profile and much better dopant confinement by the silicides. Accordingly, the ITMA scheme would lead to worse dopant drive-in efficiency than the ITA

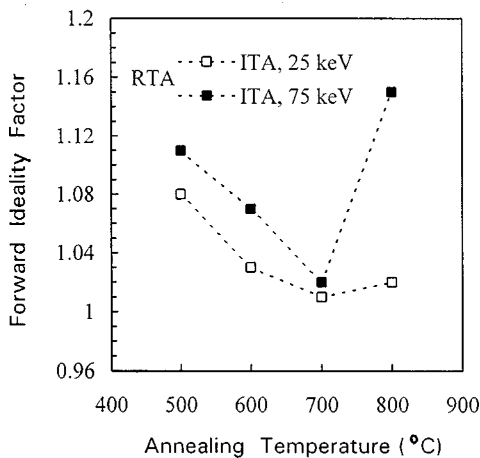

FIG. 6. Forward ideality factor corresponding to Fig. 5.

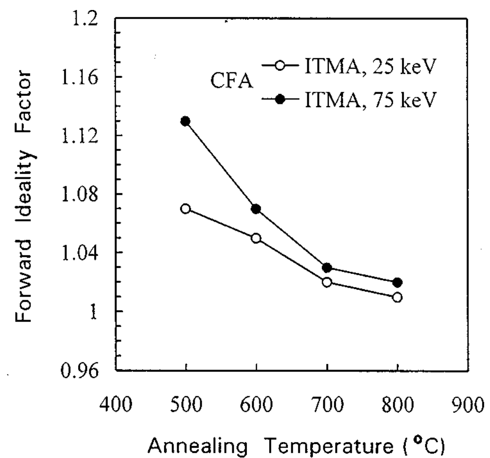

FIG. 8. Forward ideality factor corresponding to Fig. 7.

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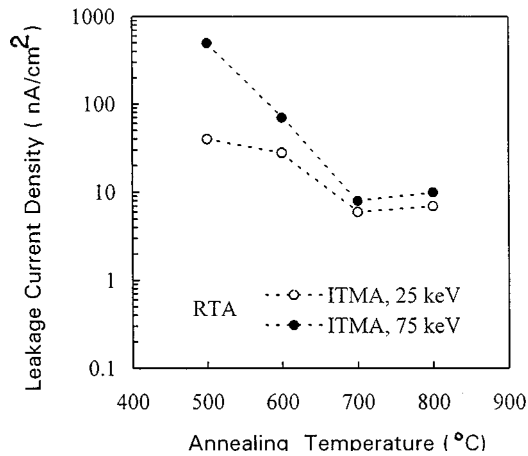

FIG. 9. Dependence of leakage current density on annealing temperature for the 25 and 75 keV implanted ITMA samples treated by RTA processing.

method. As a result, the ITMA samples showed worse junctions than the silicided ITA specimens, though sustaining lower implantation damage. However, unlike the silicided ITA samples, no significant junction degradation was observed at 800 °C for this scheme. As for the ITMA scheme, few defects were present in the Si substrate, thus largely suppressing the anomalous Ni penetration.

Moreover, by RTA processing, the resulting junctions of the ITMA samples were not as good as those of the silicided ITA samples. Figure 9 shows the dependence of leakage current density on the annealing temperature for the 25 and 75 keV implanted ITMA samples treated by RTA processing. A junction with a leakage of about 6 nA/cm^2 was obtained by the 25 keV implanted ITMA samples RTA treated at 700 °C. Though having shorter annealing/drive-in time, RTA can yield better dopant activation and defect recovery.[28,29] In addition, the dopant drive-in efficiency for the ITMA method was still low even by CFA. As a result, for the ITMA samples, RTA could still lead to junction characteristics comparable to those made by CFA. From Figs. 5 and 9 for RTA processing, it was also noted that relative to the silicided ITA samples, the ITMA samples showed less degraded junctions at 800 °C.

IV. CONCLUSIONS

As for the silicided ITA samples, excellent NiSi-silicided shallow p^+n junctions can be achieved. A junction with a leakage of about 0.7 nA/cm^2 and an ideality factor of about 1.00 is obtained by CFA at 700 °C. The implantation energy and the crystallinity of the deposited Si films after annealing would greatly affect the junctions formed at various temperatures, attributable to different implantation effects and boron depth profile. By this Ni-silicided ITA scheme, a lower implant energy is more helpful to low-temperature junction formation, due to fewer implant-induced defects. However, while the silicidation of NiSi into $NiSi_2$, anomalous Ni penetration into the Si substrate would be induced due to the implant-induced defects in the Si substrate. As a result, the junctions prepared by RTA treatment or higher implant energy are considerably deteriorated at 800 °C. On the other hand, the ITMA samples would sustain fewer defects, and thus the junction degradation at 800 °C is significantly suppressed. However, since the dopant is mainly implanted into the thin Ni films of the stacked Ni/a-Si layer, the junctions formed by this scheme are worse than those by the silicided ITA scheme, ascribed to lower dopant drive-in efficiency.

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