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Preparation and properties of tantalum pentoxide (Ta_2O_5) thin films for ultra large scale integrated circuits (ULSIs) application – A review

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Tantalum pentoxide (Ta_2O_5) thin films have rapidly evolved into an important field of research/development for both basic and applied science with the promise of creating a new generation of advanced micro devices for electronics applications. This paper provides a broad review of the current status and future trends of Ta_2O_5 thin films as a highly promising storage dielectric material for high-density dynamic random access memory applications. Various methods of thin film material processing are briefly reviewed. The physical, electrical and dielectric characteristics of Ta_2O_5 thin films with specific examples from recent literature and the associated conduction mechanisms are summarized and discussed. Some suggestions to improve the electrical properties of the films are finally included.

1. Introduction

The increase in the dynamic random access memory (DRAMs) density up to 1 Gbit creates a serious problem to ensure the required storage capacitance in trench three-dimensional (3-D) stacked-capacitor cell and technologies based on the $SiO_2/Si_3N_4/SiO_2$ (ONO) stacked capacitor. To satisfy DRAM requirements of 1-Gbit and beyond higher dielectric constant materials are necessary to keep the capacitor cells structures simple and manufacturable [1–3]. Among those new dielectrics, Ta_2O_5 has received considerable attention, because of its high dielectric constant (~ 35), high refractive index and chemical and thermal stability with the promise of compatibility with microelectronics processing.

Successful applications of any thin film material require the development of sophisticated synthesis and processing techniques, the understanding of structure-property relationships and the implementation of various novel devices. The purpose of this paper is therefore to present a brief overview of Ta_2O_5 thin films and their applicability to the processing of the next generation of ultra-large-scale integrated (ULSI) DRAMs.

In this review, we first describe the different methods of thin film material processing, since they are the ultimate factors determining the oxide properties. We then consider the main physical and electrical characteristics, highlighting some well established experimental results. Specific examples from the recent literature are reviewed to exemplify how the technique has been utilized to date in solid state technology. The general theories of electrical conduction mechanisms and the various methods of leakage current reduction are reviewed in order to check the limits of their applicability to ULSI. Background information is given on the materials chemistry and physics and over 150 references are cited. The paper will end with a critical review of summary and future trends.

2. Background

Until recently, the capacitor materials utilized in DRAMs are either a silicon dioxide or a silicon oxide/ nitride composite layer (ONO) with a relative dielectric constant of 6. As the number of memory cells increases to gigabytes, the available area for the capacitor decreases rapidly (approximately $0.4\,\mu m^2$ for a 256-Mbit device and $0.2\,\mu m^2$ for a 1-Gbit device) to maintain acceptable die sizes. Table I indicates that the capacitance per unit area should be increased to achieve higher DRAM densities [4, 5]. For maintaining sufficient storage capacitance of memory cell, manufactures have abandoned the idea of flat integrated circuits and three-dimensional cell structures were consequently incorporated by use of deep trenches and stacked layers to offer more surface area. So far, these structures combined with ONO storage dielectrics can meet the requirements of 256-Mbit DRAMs. The capacitor areas will be close to $0.2\,\mu m^2$ and $0.1\,\mu m^2$ for future 1-Gbit and 4-Gbit DRAMs, respectively (Table I). The ONO dielectrics will not be used in these products since the capacitor area cannot be maintained constant in a cell that is still manufacturable [6]. Consequently, a high dielectric constant (ε) material has been proposed for memory cells of DRAM.

Ta_2O_5 has been investigated as the most promising material for 256-Mbit and 1-Gbit DRAMs [7, 8]. The

TABLE I The road map of DRAM technology [5]

	Minimum feature size (μm)	C/area (fF/μm^{-2})	Capacitor area (μm^2)	Operating voltage (V)	Year* 1 million devices
16 Mbit	0.60	25	1.10	3.3	1992
64 Mbit	0.35	30	0.70	3.3	1995
256 Mbit	0.25	55	0.35	2.2	1998
1 Gbit	0.18	100	0.20	1.6	2001
4 Gbit	0.15	140	0.10	1.1	2004

*Year in which 1 million devices were/are projected to be produced.

DRAM cell technologies using this new materials, however, must overcome many obstacles before they will be suitable for mass production. For example, a technique for patterning of precious metal electrodes in sub-quarter-micrometer processes and a technique for very low temperature integration that does not degrade such high ε materials have to be developed. As a result, a great deal of work has been directed toward adapting Ta_2O_5 capacitor technology to 256-Mbit DRAMs, since Ta_2O_5 seems to be the most appropriate and compatible material for the conventional DRAM process [9]. In spite of these efforts, some problems remain to be solved before Ta_2O_5 can be applied to the mass-production of 256-Mbit DRAMs. For example, it is unknown how well Ta_2O_5 will stand up to the thermal treatment in the memory integration process and how thin we can make the Ta_2O_5 technology for 256-Mbit DRAMs. This will consequently lead the way to the mass production of 1-Gbit DRAMs.

At present, the trends and prospects in reducing memory cell area up to 4-Gbit [9] and the cell area has been reduced by about 36% every generation. The chip area has been increased by about 50%. The minimum feature size will be 0.2–0.25 μm in 256-Mbit DRAMs and less than 0.2 μm in 1-Gbit DRAMs, which will require the deep UV-lithography techniques. This means that the height of capacitors will be around 0.5 μm if the levelling techniques i.e. the recessed array technology [10] are used, will become a constraint.

3. Ta_2O_5 thin films and process integration

Tantalum oxide (Ta_2O_5) has useful optical and dielectric properties. It is a fairly stable oxide with an orthorhombic structure, a melting point of 1870 °C and a density of 8.27 g cm^{-3} [11]. It is moderately hard with a Vickers hardness of 1400 kg mm^{-2}. It has a refractive index of 2.1–2.2. It is an electrical insulator with a high dielectric constant (25–35). Ta_2O_5 can accommodate a wide variety of dopant ions through subtle variations of its crystal structure. Recently, it was reported that the dielectric constant of Ta_2O_5 can be increased drastically through an 8% substitution of TiO_2 [12].

Ta_2O_5 films find applications in various fields such as

(i) Dielectric for storage capacitors;
(ii) Gate insulators in metal-oxide-semiconductor (MOS) devices;
(iii) Optical coatings, anti-reflection coatings and coatings for hot mirrors.

Ta_2O_5 films are polycrystalline. Their properties depend heavily on stoichiometry, microstructure (grain size distribution), film thickness, characteristics of electrode and homogeneity of the film. The Ta_2O_5 film growth method significantly affects above parameters and consequently its dielectric properties. A variety of techniques such as anodization r.f. sputtering, reactive sputtering, thermal oxidation, chemical vapor deposition (CVD), low pressure chemical vapor deposition (LPCVD), photo-CVD, plasma CVD, metalorganic chemical vapor deposition (MOCVD) and ion assisted deposition have been used to deposit Ta_2O_5 films. The Ta_2O_5 film shows excellent electrical characteristics in an amorphous state. However, it is crystallized at temperatures higher than 700 °C, resulting in a drastic increase in the leakage current [13]. Various post-deposition annealing techniques have been proposed to reduce the leakage current in Ta_2O_5. The time dependent dielectric breakdown (TDDB) for crystalline Ta_2O_5 film annealed in N_2O was estimated to be better than the amorphous film with a reliability of around 10 years of lifetime [14].

As the DRAM generation moves to 256-Mbit and beyond, the DRAM fabrication process has become more complicated. This will cause the production cost of the high density DRAMs to become unacceptably high and will significantly degrade the device reliability. Thus, it is essential to develop a process technology that is simple and yet ensures high performance and high reliability. CVD Ta_2O_5 is a potential material for this purpose, because of its high dielectric constant and its excellent step coverage characteristics. Therefore, many investigators have studied the Ta_2O_5 CVD method and the capacitor process associated with it.

Three basic parameters for applying capacitor thin films on DRAMs are dielectric constant, leakage current density and reliability. The targets for ideal 256-Mbit and 1-Gbit DRAM dielectric include the following:

(1) SiO_2 equivalent thickness, < 0.5 nm for 256-Mbit, < 0.2 nm for 1-Gbit;
(2) leakage current density $< 1 \times 10^{-7}$ A cm^{-2} at IV;
(3) lifetime of 10 year at 85 °C and 1.6 V;
(4) stability 10^{15} cycles at > 100 MHz;
(5) general compatibility with semiconductor processing.

A new process technology for fabricating highly reliable 2.5 nm Ta_2O_5 films for stacked cylindrical polysilicon capacitors of 256-Mbit DRAM was devel-

oped by Kamiyama *et al.* [15]. The key points of this technology were rapid thermal nitride (RTN) treatment of the stacked polysilicon surface, rapid thermal annealing (RTA) treatment after Ta_2O_5 deposition and use of a TiN plate electrode on the Ta_2O_5. Kang *et al.* [16] developed a highly manufacturable process technology for 256-Mbit DRAMs and beyond. The process was simplified by employing a simple cell structure and metallizations with less complexity. The photolithography margin was significantly improved by a better level of planarization. The main features of this process were a CVD Ta_2O_5 dielectric film on poly-Si cylinder capacitors, chemical mechanical polishing (CMP) planarization, pure W bit-line and A1 reflow. This technology was reported to provide a larger process margin, higher reliability and better design flexibility, 256-Mbit DRAM cells using a 0.5 μm high crown capacitor with crystallized Ta_2O_5 dielectric film were fabricated by Ohjo *et al.* [9]. They confirmed that the crystallized Ta_2O_5 (3.3 nm of SiO_2—equivalent thickness) was very stable in the conventional metallization process and the key issues for manufacturing were to eliminate the hydrocarbon contaminants during high temperature O_2 annealing. Based on their preliminary investigation of Ta_2O_5 metal-insulator-metal (MIM) capacitors, they suggested that it was possible to fabricate 1-Gbit DRAM cells using the amorphous Ta_2O_5 MIM capacitor with a crown structure.

4. Materials processing

Deposition process are generally divided into two categories: physical vapor deposition (PVD) and chemical vapor deposition (CVD). CVD is of most interest since PVD processes, such as evaporation and sputtering, do not generally produce films of the same quality as CVD processes. The commonly used techniques for depositing dielectric thin films include low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD), sputtering, pulse laser ablation, anodization and sol-gel methods. Each technique has its merit and drawbacks. For example, MOCVD can be used for large scale production but an elevated growth temperature is required for cracking the metal-organic (MO) source. Pulse laser ablation is suitable for low temperature epitaxial growth but it can only process samples on a limited scale. Thin films are used in a host of different applications in ULSI fabrication and can be prepared by a variety of techniques. Regardless of the method by which they are formed, however, the process must be economical and the resultant films must exhibit the following characteristics: (a) good thickness uniformity, (b) high purity and density, (c) controlled composition stoichiometries, (d) high degree of structural perfection, (e) good electrical properties, (f) excellent adhesion and (g) good step converge. In the following, each deposition technique will be briefly introduced.

4.1. Chemical vapor deposition (CVD)

CVD is defined as the formation of a non-volatile solid film on a substrate by the reaction of vapor phase chemicals (reactants) that contain the required constituents. The reaction gases are introduced into a reaction chamber and are decomposed and reacted at a heated surface to form the film. A wide variety of thin films utilized a ULSI fabrication have been prepared by CVD [17, 18]. CVD processes are often selected over competing deposition techniques because they offer the following advantages; a) high purity deposits can be achieved, b) a great variety of chemical compositions can be deposited, c) some films cannot be deposited with adequate film properties by any other method and d) good economy and process control are possible for many films.

4.2. Atmospheric pressure CVD (APCVD) reactors

APCVD reactors were the first to be used by the microelectronics industry [19]. Operation at atmospheric pressures kept reactor design simple and allowed high film deposition rates. APCVD, however, was susceptible to gas phase reactions and the films typically exhibit poor step coverage [19]. Table II summarizes the characteristics and applications of the various CVD reactor designs.

4.3. Low pressure CVD (LPCVD)

The growth of thin films by LPCVD has become one of the most important methods of film formation in semiconductor fabrication. LPCVD in some cases is able to overcome the uniformity, step converge and particulate contamination limitations of early APCVD systems [20–26]. By operating at a medium vacuum (33–266 Pa) and higher temperatures (550–600 °C), LPCVD reactors typically deposit films in the reaction rate limited regime. Low pressure operation also decrease gas phase reactions, making LPCVD films less subject to particulate contamination. Two main disadvantages of LPCVD are the relatively low deposition rates and relatively high operating temperatures. Attempting to increase deposition rates by increasing the reactant partial pressures, tends to initiate gas phase reactions. LPCVD is used for depositing many types of films, including poly-Si, Si_3N_4, SiO_2, PSG, BPSG and W.

4.4. Rapid thermal low pressure metal-organic chemical vapor deposition (RT-LPMOCVD)

RT-LPMOCVD was explored as a means to carry out a number of critical steps in the processing of many electronic devices, under a vacuum environment [27]. With shorter time duration cycles for wafers, the reaction temperature is a key characteristic in RTP. Thus, the incorporation of impurities into wafers is minimized. In addition, the unique time-temperature schedule provided by the RTP cycle allows for more highly controlled processes than conventional furnace sintering.

The RTP-LPMOCVD technique appears to be very promising in the fabrication of thin high quality semiconductor, dielectric and metallic films with abrupt interfaces. The technique combines rapid thermal

TABLE II Characteristics and applications of CVD reactors [11, 17]

Process	Advantages	Disadvantages	Applications
Atmospheric pressure-CVD	Simple reactor, fast deposition, low temperature	Poor step coverage, particle contamination	Low temperature oxides, both doped and undoped
Low pressure CVD	Excellent purity and uniformity, conformal step converage, large wafer capacity	High temperature, low deposition rate	High temperature oxides, both doped and undoped, silicon nitride, poly-Si, W, WSi_2
Plasma enhanced CVD	Low temperature, fast deposition, good step coverage	Chemical (e.g. H_2) and particulate contamination	Low temperature insulators over metals, passivation (nitride)
Photon induced CVD	Low substrate temperature, good step coverage	Low density, molecular contamination	Low-temperature insulators over metals
Electron cyclotron Resonance plasma CVD	Low temperature, minimized substrate damage	Need low pressure 0.133–0.00133 Pa high intensity magnetic field	III-V and II-VI compounds

annealing and chemical deposition processes. The reactions are carried out by switching the radiant energy sources (halogen-tungsten lamps) on and off, to initiate and terminate reactions that occur in the presence of continuously flowing gases. Alternatively, the radiant sources can be left operating continuously, while switching the gas flow. In the later case, the RT-LPMOCVD reactor behaves as a standard LPMOCVD reactor.

4.5. Metal-organic chemical vapor deposition (MOCVD)

MOCVD is a specialized area of CVD which utilizes metal-organic compounds as precursors, usually in combination with hydrides or other reactants. The thermodynamic and other kinetic principles of CVD and its general chemistry also apply to MOCVD. The major issues of concern in the MOCVD technique are the choice of precursor sources and the substrate temperature required for cracking the precursors. For depositing dielectric thin films, the ideal precursor for MOCVD should possess the following requirements: (1) high vapor pressure and low vaporization temperature, (2) low cracking temperature, (3) large temperature difference between vaporization and cracking and (4) no contamination from the organic constituent.

A wide variety of materials can be deposited by MOCVD, either as single crystal, polycrystalline or amorphous films [11]. The most important application is for the deposition of the group III-V semiconductor compounds such as gallium arsenide (GaAs), indium arsenide (InAs), indium phosphide (InP) and gallium aluminum phosphide (GaAIP), particularly for epitaxial deposition. Most MOCVD reactions occur in the temperature range of 600–1000 °C and at pressures varying from 133 Pa to atmospheric. The equipment and chemicals used in MOCVD are expensive and the production cost is high. For this reason, MOCVD is considered most often where very high quality is required. It has recently been investigated for other applications in the area of very high temperature oxidation protection up to 2200 °C.

4.6. Liquid source CVD

Although each application has unique material requirements, in most cases the deposition process must have good conformability, composition control and throughput, while minimizing the thermal budget. The absence of volatile and in some cases stable precursors has driven the development of the ''liquid delivery technique'' in which reactant gas composition is set by volumetric metering of liquids followed by flash vaporization [29]. The liquid delivery technique relies on the flash vaporization of liquid solutions and overcomes the limitations of bubbling. Neat liquids as well as liquid solutions comprised of solids dissolved in organic or inorganic media can be used with this technique. The liquid source reagent solutions are maintained at room temperature and the composition of the inlet to the CVD chamber is controlled by one of several methods. In the preferred embodiment the reactant gas composition is controlled through real time volumetric mixing of the individual source reagent solutions. The liquid mixture is then flash vaporized to generate a homogeneous gas at the inlet to the CVD tool. This method ensures process reproducibility as variations in delivery rate give rise to variations in the overall deposition rate but do not affect film composition [29].

4.7. Sputtering

The sputtering system used for depositing oxides can be divided into r.f. magnetron sputtering and ion beam sputtering (IBD). The operating principles of r.f. sputtering and ion beam sputtering have been described in previous references [30]. In recent years, ion beam sputtering has gradually become a popular technique for the deposition of oxide thin films. In the ion beam sputtering system, one or several Kaufman type ion guns are used to generate a broad inert gas ion beam with the accelerating voltage between 100–1500 eV. As the ion beam impinges on the target surface, the oxide materials are sputtered to deposit on a heated substrate. It has been shown that IBD can be used for growing high quality oxide thin film like PLZT and $KNbO_3$ for optical applications [31, 32].

4.8. Pulse laser ablation

The fundamental principle of pulse laser ablation deposition involves the interaction between a laser beam and a solid surface which is divided into three steps: (1) absorption of photon energy by the target and heat conduction, (2) surface melting of oxide target and (3) evaporation and ionization of the oxide target. It has been demonstrated that ferroelectric or oxide conductors like PZT [33], $SrBaTiO_3$ [34], $SrRuO_3$ [33] and ITO [35], can be deposited or epitaxially grown by pulse laser deposition.

4.9. Anodization

Anodic oxide films of Ta_2O_5 have received much attention in the last decades due to their good insulating properties. The anodic Ta_2O_5 oxide shows very peculiar characteristics. It is grown electrolytically from the Ta metal at very high electric fields ($\sim 10^6\,V\,cm^{-1}$), so that the films are also able to withstand high fields under anodic polarization. Usually, they are obtained in galvanostatic conditions, i.e. by applying a constant current to the anodizing cell. In these circumstances, the charge passed makes the thickness of the film increase linearly with time. In the same way, the applied voltage also increases linearly, in order to keep the electric field constant during the process. Under these apparent steady-state conditions (i.e. with a constant field) the voltage finally reaches a value at which some light sparks start to appear. They are frequently accompanied by voltage and current pulses, as well as copious gas evolution and other phenomena. This is the so-called electrolytic breakdown on scintillation, which limits the oxide growth in a natural manner [36].

The incorporation of electrolyte species into the oxide plays an important role in determining many of the parameters of the oxidation process. The incorporation process was first investigated by Randall *et al*. [37]. The presence of electrolyte species incorporated into the oxides seriously affects the properties of the final oxide. It has been shown for Ta_2O_5 formed in phosphoric acid electrolytes, that a large decrease in the density occurs as the anodization is performed in electrolytes of increasing concentration. This produces a corresponding decrease of the relative permittivity and refractive index [38–42].

4.10. Sol-gel method

In the sol-gel process, the reaction involves the following steps: 1) Sol preparation: The process involves the dissolution of the required metal ions, either as alkoxides or other metallo-organic salts, in a suitable alcoholic solvent, or as inorganic salts in an aqueous solvent to form the ''sol''. 2) Gel formation: In which the fluid sol is transformed to a semi-rigid solid ''gel''. The process can proceed by a number of different routes, resulting in either polymetric or colloidal gels, depending upon the particular system. In the case of a colloidal system, gellation is controlled by electrostatic or steric interactions between the colloidal constitutents in the sol, whilst the formation of polymeric gel is determined by the reactive rates and extents of chemical reactions, including, hydrolysis, condensation and polymerization. 3) Gel to ceramic conversion: Heat treating the prepared gel has the effect of drying and pyrolysis of the gel structure rearrangement and densification occurs simultaneously, then crystallization occurs. Owing to the intimacy of mixing of the constituents and to the extreme reactivity of the dried gel, the crystallization stage may occur at temperatures several hundreds of degrees below those required for traditional mixed-oxide processing. These reduced temperatures could enable the direct integration of ceramic components with semiconductor devices and other substrate materials as well as the fabrication of unique material combinations with unusual phase assemblies and novel properties [43].

Among the various techniques described above, the most common techniques that have been frequently utilized to deposit Ta_2O_5 thin films are anodization [44, 45], thermal oxidation [46, 47], reactive sputtering [48, 49], LPCVD [50, 51] and PECVD [52–54]. For application to storage capacitors, the dielectric films must have a very small leakage current to maintain the favourable retention characteristics and, in the case of topography for three-dimensional memory cells, have the ability for excellent step coverage. Anodic oxidation which has been used to deposit Ta_2O_5 for a long time produces dielectric films which allow ionic flow readily during the deposition process and hence suffer from a high temperature oxygen ion drift effect under bias. This will result in a large hysteresis phenomena observed in their capacitance-voltage (C–V) characteristics [44, 45]. A large C–V clockwise hysteresis phenomena in Ta_2O_5 film formed by thermal oxidation has been also observed by Hwu and co-workers [47, 55]. D.C. magnetron reactive sputtering [56] deposition has the advantage of depositing Ta_2O_5 films at low temperatures, which is very desirable for applications where the processing temperature or thermal budget is a major concern. A major difficulty in the reactive sputtering deposition technique is choosing the process conditions to obtain stoichiometric Ta_2O_5 films at the highest deposition rate. Several researchers have investigated the reactive sputtering deposition process and have proposed different criteria of the deposition condition for preparing stoichiometric Ta_2O_5 films [57, 58].

Although as-deposited sputtered films have low leakage currents in the amorphous phase, the high temperature treatments, which are necessary for standard DRAM processes, will lead to the crystallization of these films and hence a drastic increase in the leakage current [59]. This, obviously, limited their application on DRAMs in terms of the cells. The as-deposited CVD Ta_2O_5 films have rather leaky current characteristics due to oxygen deficiency and impurity contamination existing in films, this can be significantly reduced to acceptable levels for applications by annealing techniques. The amorphous Ta_2O_5 MIM capacitors deposited by PECVD also exhibit good electrical and dielectric properties [60]. The ability of step coverage is very important for application to three-dimensional memory cells. Anodic oxidation, thermal oxidation and sputter techniques have been found to be insufficient for the ability of step coverage in complicated cell structures. CVD Ta_2O_5 films can provide better step coverage ability and good thickness uniformity across the wafer

[50, 61]. Thus, based on the consideration of the electrical characteristics and step coverage, CVD Ta_2O_5 is more suitable for application to mass production. Recently, dual spectral sources assisted metal-organic chemical vapor deposition (MOCVD) was reported to be an ideal technique for the deposition of Ta_2O_5 films. The leakage current densities of 10.6 nm thick films were as low as 10^{-10} A cm^{-2} for gate voltages under 4 V [62].

5. Rapid thermal annealing

Recently, rapid thermal annealing (RTA) has become more important in the application on ULSI technologies, such as thin dielectric deposition, polysilicon growth, shallow junction formation, silicidation and annealing [63]. The great advantages of the technique are a rather short processing time and its relative process simplicity as compared with the conventional furnace apparatus. A short processing time will be beneficial to reduce the time-temperature product such that the physical or chemical processes are completed while unwanted processes such as dopant diffusion penetration, interface reactions, decomposition are effectively controlled. Kamiyama *et al*. [64] reported that RTA in O_2 after Ta_2O_5 deposition will densify the CVD Ta_2O_5 films. It is also reported that a nitridation on the surface of polysilicon bottom electrode utilizing RTA before Ta_2O_5 deposition can minimize the interface oxidation between Ta_2O_5 and bottom polysilicon deposition and post-deposition annealing treatments [65–67]. Rapid thermal N_2O annealing (RTN_2O) has been applied to reduce the leakage current in the Ta_2O_5 films prepared by LPCVD [68–71]. It was reported that the effective dielectric constant decreases with increasing RTN_2O temperature.

6. Conducting oxides

With the growth of density and complexity of integrated circuits, a flexibility in available metallization options is very desirable. Metallization used for interconnects, contact diffusion barriers and gate electrodes require low resistivity and high thermal stability of the conducting material. It would be preferable for the processing simplicity to have one metal applicable to all these functions. However, because of more specific requirements such as low contact resistance in contact applications [72] and a proper work function in gate metallization [73], the present metallization schemes cannot satisfy all the above mention functions. The choices are further reduced by the required compatibility with present fabrication techniques. Therefore, there is a need for novel materials that can fulfil one or more of the metallization requirements in current and future microelectronic devices.

The metallic oxides of transition metals may present a very attractive metallization option in a variety of very large scale integrated (VLSI) applications [74]. Dioxides of Ru, Ir, Os, Rh, V, Cr, Re and Nb, have bulk metallic resistivities ranging from 30 to 100 μΩ cm, with IrO_2 being the best conductor in this group. There exist other transition metal oxides that merit attention, such as ReO_3 with a resistivity of 10 μΩ cm, which is lower than that of the widely used $TiSi_2$. The heats of formation of transition metal oxides are comparable to that of transition metal nitrides [75] which emphasizes their normal stability. Ruthenium dioxide was reported to have low contact resistance on Ti metal [76], comparable to pure ruthenium and gold. Chromium oxide, although fairly resistive has been used successfully as a diffusion barrier in the late seventies [77] and recently, films of RuO_2 prepared by CVD were also reported to exhibit good diffusion barrier properties [78].

It was reported that the electrical characteristics of Ta_2O_5 films strongly depend on the top electrode material [15, 50] e.g. Al, Au, W and TiN. Matsuhashi and Nishikawa [79] showed that the work function of the top electrode material and the stability of the top electrode/Ta_2O_5 interface determine the electrical characteristics of the Ta_2O_5 film. They investigated the effects of electrode materials, metal (W, Mo, Ti, and Ta) and their nitrides (WN, MoN, TiN and TaN), on the leakage current in Ta_2O_5 films before after annealing and proposed that TiN is the optimum electrode for low temperature process (about 400 °C) while Mo or MoN is the optimum electrode for high temperature processes (about 800 °C). Table III shows that work function (ϕ_m) of electrode materials before and after annealing [79]. The effects of interfacial oxide layers formed on the various bottom electrodes (Si, Pt, TiN and W) on the dielectric properties of Ta_2O_5 thin films were reported by Kim *et al*. [80]. The incubation period of the Ta_2O_5 film deposition was related to the oxidation of the electrodes.

7. Physical properties

7.1. X-ray diffraction (XRD) and microstructure

The electrical properties of Ta_2O_5 films were strongly dependent on fabrication methods and were expected to be related to the composition, chemical characteristics and microstructure of thin films. In this section, the effect of physical and chemical characteristics on the electrical properties of Ta_2O_5 thin films studied by various workers are briefly reviewed. Kimura *et al*. [48] showed the variation of intensity of two peaks from (0 0 1) and (2 0 1) of crystallized Ta_2O_5 films as a function of annealing temperature. They also confirmed that the Ta_2O_5 films annealed below 600 °C do not show any notable crystallization and the crystallization temperature of

TABLE III Work function (ϕ_m) of electrode materials before and after annealing [79]

Electrode materials	Work function ϕ_m (V)		
	Before annealing	400 °C annealing	800 °C annealing
Mo	4.64	4.78	4.94
W	4.75	4.74	4.77
Ti	4.17	3.91	—
Ta	4.25	4.33	4.72
MoN	5.33	4.89	4.70
WN	5.00	4.76	4.83
TiN	4.95	4.80	4.81
TaN	5.41	4.55	—

Ta_2O_5 film grown by reactive sputtering lies between 650 °C and 700 °C. The results obtained by Kimura *et al.* [48] were consistent with the other reports [81, 82] for anodically or thermally grown Ta_2O_5 film. More recently, Aoyama *et al.* [83] and Chiu *et al.* [84] reported similar crystallization behaviour of Ta_2O_5 films deposited by LPCVD process. It is, therefore, clear that the crystallization temperature of Ta_2O_5 film does not depend on the method by which the film is grown.

The investigation of Ta_2O_5 thickness dependence on crystallization by Nishioka *et al.* [85] showed that the film does not crystallize in the lower thickness region after dry O_2 annealing at temperatures higher than 800 °C. Using electron diffraction studies they demonstrated that the amorphous state in a 20 nm thick Ta_2O_5 film was maintained even after high temperature annealing. These electron diffraction results seem to be contradictory to the published results by Roberts *et al.* [86] which show that Ta_2O_5 film with a thickness of less than 20 nm crystallizes in 1000 °C N_2 ambient. However, Nishioka *et al.*, [85] confirmed that in Ta_2O_5 film less than 20 nm thick, no change from an amorphous-type diffraction and no change of surface morphology were observed after dry O_2 annealing for 30 min at temperatures up to 1000 °C. From the transmission electron microscopy (TEM) studies, they further clarified that the surfaces of the Ta_2O_5 films were very smooth, no surface was created after the O_2 annealing and no grain boundary which is the characteristic of a polycrystalline film, were observed. Hence, they claim that the crystallization conditions of the very thin Ta_2O_5 film would depend on annealing gases, impurities in the Ta_2O_5 films, stress in the films, surface conditions of Si substrates, etc. Revesz and Kirkkendall [87] reported that an O_2 anneal of Ta_2O_5 films on Si enhances the diffusion of Si into the Ta_2O_5 film.

Recent investigation on the short duration RTA processing of Ta_2O_5 films by Ezhilvalavan and Tseng [88] demonstrated that XRD of Ta_2O_5 films subjected to 30 s O_2 RTA at 800 °C correspond either to β-Ta_2O_5 (orthorhombic crystal structure) (Fig. 1) or α-Ta_2O_5, which is a high temperature from of Ta_2O_5 [89]. This is because the spectra of the two phases are too similar to allow distinction between them on the basis of XRD

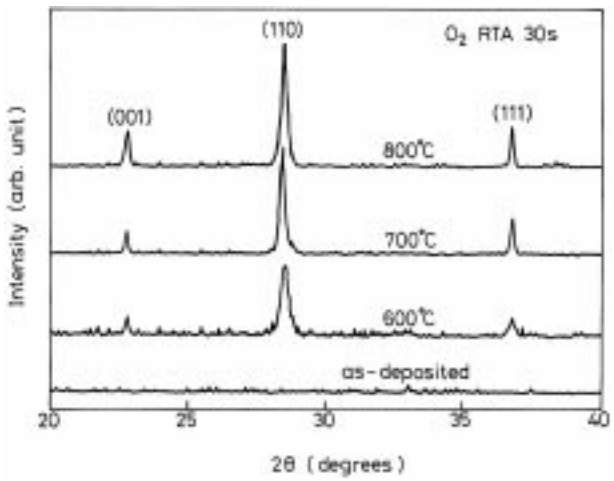

Figure 1 X-ray diffraction spectra of Ta_2O_5 films as-deposited and O_2 RTA processed at different temperatures for 30 s [88].

alone [89, 90]. In RTA processing of amorphous films, during crystallization, the excess free energy of the amorphous state relative to the crystalline phase is released instantaneously resulting in explosive crystallization. Such a process often renders much higher temperature than the set values instantaneously in localized areas and provides a probable opportunity to lead the Ta_2O_5 into the α-phase [63, 91, 92]. Since RTA processing time is very short, and also the cooling and heating rates are very high ($100\,°C\,s^{-1}$) almost equivalent to normal quenching methods, there is a possibility of α-phase which can appear as a minor phase and may be distributed in the grain boundaries. Such two-phase structures have been mentioned in RTA Ta_2O_5 films by Pignolet *et al.* [92]. Further, from scanning electron microscopy (SEM) observations, Ezhilvalavan and Tseng [88] showed that RTA carried out for longer duration leads to sufficient grain growth. In contrast, there was restricted grain growth and grain boundary formation for RTA treated for 30 s. This is obvious because the RTA processing time of 30 s is very short for a possible large nucleation and growth kinetics. Through energy dispersive X-ray analysis (EDX) of RTA processed Ta_2O_5 films, they also observed that Si was detected both in the grain boundary and grain interior, the distribution of Si at the grain boundary was larger than that within the grain. Also, it is to be noticed from their EDX distribution profile that the concentration of Si in the RTA processed Ta_2O_5 films for 30 s is very low in comparison to that of films RTA treated for 30 min [88].

From the cross-sectional TEM study on annealed Ta_2O_5. Shen *et al.* [93] suggested that the leakage current was related to the grain boundary grooving due to the crystallization and void formation possibly due to excess argon and oxygen. The recrystallization was observed to have occurred even for a thickness as low as 16 nm, contrary to the report, by Nishioka *et al.* [85] that thin Ta_2O_5 film remained amorphous even after high temperature treatment, XRD results of Roberts *et al.* and Zaima *et al.* [51, 86] showed that the annealed films were crystallized into β-Ta_2O_5. The Ta_2O_5 films were examined with XRD methods for evidence of crystallinity [94]. The absence of diffraction peaks in the pattern obtained from films oxidized at < 550 °C indicated that these films were predominantly amorphous [94]. The films heated to 900 °C for times as short as 5 min, were observed to have sharp diffraction lines in the XRD spectra.

Examination of Ta_2O_5 surfaces by Nomarski phase contrast microscopy Oehrlein *et al.* [94] found that after annealing of Ta_2O_5 films at 650 °C in Ar for 14 h, the entire surface of the film appears grainy and they ascertained that the appearance of structure in the Nomarski micrographs corresponds to crystallization of Ta_2O_5 into the low temperature β-Ta_2O_5 modification. However, this was verified by XRD studies by many authors. Oehrlein *et al.* [94] examined the Ta_2O_5 film on Si by Rutherford backscattering and demonstrated that within the experimental error limits both the amorphous and polycrystalline Ta_2O_5 films were stoichiometric.

TEM studies with films of 5–40 nm were carried out by Roberts *et al.* [86]. Very little difference in microstructure was observed for the films greater than

20 nm. The overall features for the r.f.-sputtered films were similar to those for the equivalent thickness of the extensive and random distribution of submicrometer pores which were believed to be precipitated argon (as determined from energy dispersive X-ray analysis). The microstructure of the d.c. films varies considerable within the range of 5–20 nm with filaments terminating randomly, but not at grain boundaries, which was related to the submicrometer microcracks which arose from differential thermal contraction during cooling from the high temperature anneal. The structural change of the Ta_2O_5/Si interface after O_3 annealing was examined by Isobe and Saitoh [95] from the cross-sectional transmission electron micrograph images. The increase of the interfacial SiO_2 layer at the interface caused by O_3 annealing was observed from TEM analysis. The cross-sectional TEM analysis reported by Shen *et al.* [93] also confirmed the SiO_2 growth under the Ta_2O_5.

A cross-sectional scanning electron micrograph of excellent step coverage by CVD tantalum oxide was demonstrated by Shinrik and Nakata [96]. A uniform coverage of approximately 0.1 μm of tantalum oxide was deposited. This result was related to the film formation due to the surface reaction being limited. In contrast, a sputter-deposited Ta_2O_5 film has poor step coverage. The Ta_2O_5 film was extremely thin at the side wall of a similarly shaped trench and the film was not formed at the corner of the bottom of the trench. Therefore, it is clear that the CVD-Ta_2O_5 film is superior to sputtered Ta_2O_5 films for application in advanced three-dimensional memory cells.

7.2. X-ray photoelectron spectroscopy (XPS)

XPS analysis was used by Byeon and Tzeng [97] to study the physical properties of the three types of oxides. Accordingly, the Ta 4f spectra for the sputtered and anodized oxides showed binding energy peaks at 26.5 and 26.8 eV, respectively, indicating weakly bound oxide states. The Ta 4f spectrum for the sputtered/anodized oxide showed a peak at 28.6 eV. The shift toward a higher binding energy in the sputtered anodized oxide was interpreted as a chemical shift of core electrons in the oxide due to the two-step oxidation, which causes strong binding between metal and oxygen atoms. This indicates the more complete oxidation of the sputtered/anodized oxide film which leads to its superior dielectric properties.

The chemical states of elementary atoms at the surface of tantalum oxide films thermally grown on silicon, have been reported [98]. It appears that the XPS peaks of these specimens do not change with oxidation temperature. The binding energies of Ta $4d_{3/2}$ and Ta $4d_{5/2}$ were in agreement with the values reported [99]. Hence, they concluded that the chemical composition of thermally oxidized tantalum films was Ta_2O_5 regardless of oxidation temperature and oxide thickness. A weak Si 2p peak detected from the surface of the films with a binding energy of $\sim$ 103 eV was interpreted as being due to the presence of silicon at the surface of tantalum oxide in the form of SiO_2. Sun and Chen [100] reported the XPS analysis at the surface of as-deposited LPCVD-Ta_2O_5 film. Their result indicates that the film consists of Ta, O and C at the surface of Ta_2O_5. The existence of carbon impurities was attributed to the introduction into the Ta_2O_5 film through thermal decomposition of the $Ta(OC_2H_5)_5$ source during film deposition [101, 102].

7.3. Auger electron spectroscopy (AES)

AES profiling study was performed by Oehrlein *et al.* [94] for 66 nm Ta_2O_5 on Si where Ta_2O_5 had been formed by oxidation of deposited Ta at 550 °C for 1 h in Ar/O_2. They reported that the Ta and O Auger intensities throughout the bulk of the Ta_2O_5 film were nearly constant and decreased rapidly at the Ta_2O_5/Si interface. They observed a peak from the oxide signal at the Ta_2O_5/Si interface as well as a shoulder in the oxygen distribution at the same location. This was suggestive of an interfacial SiO_2 layer. The oxide signal was substantially higher in the specimens which had been heat-treated in O_2 at higher temperatures than that in the as-formed sample.

A weak Auger peak of Si (78 eV) [103] which was observed at the interface of Ta_2O_5/Si annealed in O_2 or N_2 has also manifested the existence of the SiO_2 layer at the interface. The SiO_2 formation was attributed to the interfacial oxidation of Si substrate with oxygen atoms supplied from outside through the Ta_2O_5 films or the reaction of Ta_2O_5 and Si at the interface. One, therefore, should conclude that during a high temperature heat treatment oxygen diffuses through the Ta_2O_5 film to the Ta_2O_5/Si interface and oxidizes the Si substrate to form a thin SiO_2 layer.

7.4. Secondary ion mass spectrometry (SIMS)

Fig. 2 shows the SIMS depth profile of the Ta_2O_5 on Si reported by the Park and co-workers [13, 98]. The solid line in the figure is for the sample with a thickness of 19 nm prepared by oxidizing the sputter-deposited Ta at 500 °C for 1 h in dry O_2. The dotted curve is for the sample that was subsequently annealed at 950 °C for 20 min in dry O_2. It can be seen that the annealed sample showed a higher concentration of Si in the Ta_2O_5 films than in the oxidized one. They attributed this phenomenon to Si atoms diffused from the Si substrate into the overlying Ta_2O_5 film during the high temperature annealing. Matsui *et al.* [107] and Tanimoto *et al.* [108] also observed similar results for the Ta_2O_5 films formed by UV photo-CVD using ozone and $TaCl_5$ [107, 108]. Recently, Ezhilvalavan and Tseng [88] reported SIMS analysis of sputtered Ta_2O_5 films and confirmed the presence of Si contamination in the RTA processed Ta_2O_5 film at high temperatures. RTA processed film showed a higher concentration of Si and lower concentration of oxygen. It is also to be noticed from their results that the Si concentration at the interface was increased after annealing and it further extends into the Ta_2O_5 film, whereas the 30 s RTA processed film showed a lower concentration of Si at the interface and in the film, in comparison to the 30 min RTA processed Ta_2O_5 film. They envisaged that the origin was the underlying SiO_2/n-Si substrate, from which Si probably

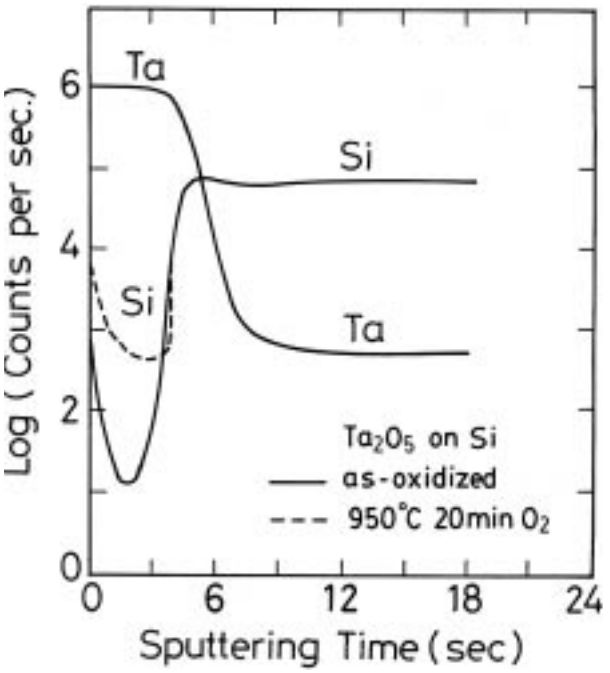

Figure 2 SIMS depth profiles of Ta_2O_5 as-oxidized and annealed at 950 °C for 20 min [13]: —, as-oxidized: —, 950 °C 20 min O_2.

diffused into the Ta_2O_5 film through the very thin Pt layer (150 nm) during the high temperature annealing. They suggested that Ta_2O_5 crystallizes rapidly and Si diffuses along the grain boundary and further penetrates into the grain and the diffusion process of Si depends on the temperature as well as the time of RTA processing.

7.5. Fourier transform infrared (FTIR) absorbance

The change in FTIR absorbance of the Ta_2O_5 as a function of annealing temperature is shown in Fig. 3 [13]. An as-oxidized sample, with the amorphous structure, showed a prominent peak at 635 cm^{-1}. In contrast, a peak at 520 cm^{-1} is prominent for the sample annealed at 950 °C. With the increase in annealing temperature, the magnitude of the absorbance at 635 cm^{-1} and 520 cm^{-1} was increased, which was related to the increase in the number of Ta—O bonds. The peak at 1070 cm^{-1} which was due to the stretching motion of the Si—O bond in the SiO_2 was also observed from the Ta_2O_5 films annealed at above 750 °C and the magnitude of the absorbance also increased with increased annealing temperature [104]. Park *et al.* [13] reported that the SiO_2 layer at the interface increased with increase of annealing temperature and the sample annealed in N_2 ambient also showed the same result, except that the absorbance at 1070 cm^{-1} of these films was lower than that of films annealed in O_2.

8. Electrical properties

Ta_2O_5 films have excellent electrical and dielectric properties. In this section, the several studies that were reported on the electrical and dielectric characteristics of Ta_2O_5 films are reviewed. Table IV lists the best properties of Ta_2O_5 films processed by various methods.

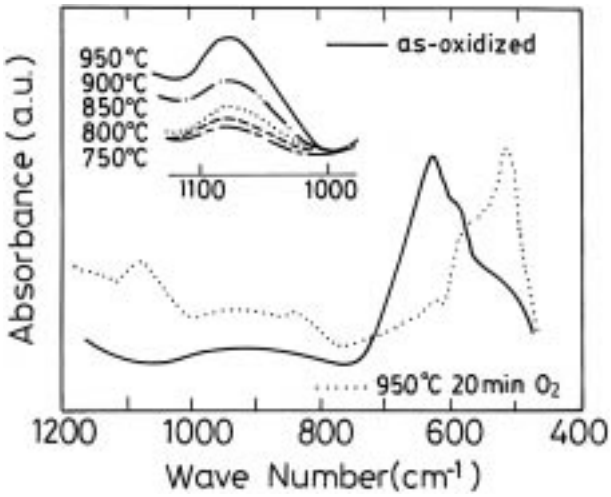

Figure 3 FTIR spectra of 19 nm thick Ta_2O_5 as-oxidized and annealed at various temperatures in O_2 ambient for 20 min [13]: —, as-oxidized: ....., 950 °C 20 min O_2.

8.1. Dielectric constant

The crystallographic orientation dependence of Si substrates on the dielectric constant of Ta_2O_5 was reported by Seki *et al.* [105]. They compared the dielectric constant to the thickness variations of Ta_2O_5 film deposited on Si having different crystallographic orientations. It can be noticed that for each substrate, the dielectric constant of deposited Ta_2O_5 increases monotonically with its thickness and there was a dependence of the dielectric constant on the substrate orientation, i.e. at every thickness the dielectric constant followed the sequence $\varepsilon(110) > \varepsilon(111) > \varepsilon(100)$. From the dielectric constant profile studies, they pointed out that the crystallographic orientation has no influence on the homogeneous layer formation and it mainly has an effect on the transition layer formation. The above authors also reported [106] the variations in the dielectric constant of the deposited Ta_2O_5 with the total thickness of the film using the dielectric constant profile. From these results, they concluded that a 5.8 nm thick transition region with a gradual variation of the composition exists at the interface. They also studied the relationship between the dielectric constant of the Ta_2O_5 film and the initial oxygen partial pressure during the first minute of deposition and found an increase in dielectric constant as the initial oxygen partial pressure decreases.

The thickness dependence of the dielectric constant of a photo-CVD Ta_2O_5 film with and without p-O_2 annealing reported by Matsui *et al.* [107] is shown in Fig. 4. The dielectric constant decreased with decreasing Ta_2O_5 thickness, but it did not decrease significantly with p-O_2 annealing. From the above figure it was claimed that the dielectric constants of photo-CVD Ta_2O_5 films were larger than those previously reported for Ta_2O_5 films sputtered on single crystalline silicon [49, 105] throughout the whole thickness region. Tanimoto *et al.* [108] determined that the dielectric constant of Ta_2O_5 film deposited by photo-CVD saturated at the deposition temperatures over 300 °C which they interpreted as due to the increase in film density. Table V summarizes the properties of Ta_2O_5 film at various annealing conditions. The effective dielectric constant of Ta_2O_5 film deposited on Si decreases with the

TABLE IV Best properties of Ta_2O_5 films processed by various methods

Processing methods	Film thickness (mm)	Leakage current density ($A\,cm^{-2}$)	Dielectric constant	Dielectric breakdown strength ($MV\,cm^{-1}$)	Capacitor structure	Ref.
RF-sputtering	56–60	10^{-9} at 1 MV cm^{-1}	18–20	6	Al/Ta_2O_5/p-Si	[106]
Reactive sputtering	100	10^{-6} at 1 MV cm^{-1}		4.5	W/Ta_2O_5/n-Si	[85]
	100	10^{-10} at 100 kV cm^{-1}	52	2–3	Pt/Ta_2O_5/Pt/SiO_2/n-Si	[88]
Reoxidation	120		22–22.5	6.2–6.6	Al/Ta_2O_5/Al	[97]
Electron beam	20	3×10^{-6} at 1 MV cm^{-1}	22–30	3–4	Al/Ta_2O_5/p-Si	[46]
deposition/thermal oxidation	60–180	1×10^{-7} at 1 MV cm^{-1}		2–4.5	Al/Ta_2O_5/p-Si	[115]
Anodization	120	10^{-7} at 1 MV cm^{-1}		1–1.5	Al/Ta_2O_5/Ta	[116]
LPCVD (oxygen annealing)	30	10^{-11} at 1 MV cm^{-1}	18–19	2–3	Al/Ta_2O_5/p-Si	[51]
LPCVD (ozone annealing)	10–20	10^{-9} at 1 MV cm^{-1}	15–20		Al/Ta_2O_5/n-Si	[95]
Photo-CVD	100	10^{-8} at 1 MV cm^{-1}	20–25		Al/Ta_2O_5/n-Si	[107]

TABLE V Properties of Ta_2O_5 films under various annealing conditions

Processing methods	Annealing conditions	Temperature (C)	Leakage current density ($A\,cm^{-2}$)	Dielectric constant	Ref.
Thermal oxidation	As-deposited		$> 10^{-6}$	22	[13]
	O_2 annealing	800	$< 10^{-8}$	25–30	[98]
RF-magnetron sputtering	O_2 annealing		$< 10^{-9}$	15–20	[106]
Reactive sputtering	As-deposited		10^{-6}	15–22	[85]
	O_2 annealing	1000	$< 10^{-9}$		[93]
	O_2 RTA	800	10^{-10}	52	[88]
LPCVD	As-deposited		$> 10^{-3}$	21	[51]
	O_2 annealing	700	10^{-4}–10^{-6}	25	
		800	10^{-11}	18–20	
LPCVD	RTO	800	10^{-8}	20–30	[123]
	FO	800	10^{-8}–10^{-9}	15–20	
	RTN_2O	800	10^{-9}–10^{-10}	10–20	
Photo-CVD	As-deposited		$> 10^{-4}$	24	[107]
	O_2 annealing	400	10^{-8}	25–30	

decrement of film thickness. This is due to the thin (1.5–3 nm) SiO_2 layer formed at the interface between the Si and Ta_2O_5. Hashimoto *et al*. [109] suggested that a suitable electrode material is necessary to prevent this dielectric constant degradation. They found that the metal-oxide-metal structure fabricated with Ta_2O_5 sandwiched between Mo electrodes did not show the dielectric constant degradation.

The effect of O_3 (ozone) annealing on the dielectric constant of Ta_2O_5 was studied by Isobe and Saitoh [95]. Accordingly, the effective dielectric constant of the O_3 annealed Ta_2O_5/Si was slightly smaller than that of the as-deposited film especially when the Ta_2O_5 film was thin. This decrease of the effective dielectric constant was reported to be essentially consistent with the increase of SiO_2 layer at the interface caused by O_3 annealing, as observed by TEM analysis.

The growth and electrical characteristics of Ta_2O_5 films by cold wall-type LPCVD and post annealing in O_2 at temperatures ranging from 600–900 °C were studied by Zaima *et al*. [51]. It was reported that for the films grown by the above method, a high-temperature anneal was found to be exceedingly effective for an increase in dielectric constant and a decrease in leakage current flowing through the film. Fig. 4 shows the dependence of relative dielectric constant (ε_r) on the film thickness for Ta_2O_5 films deposited at 340–400 °C. It should be noted that ε_r of the film depends preferentially on the film thickness, in spite of the wide variety of deposition conditions. The ε_r for the as-deposited film was larger than those reported by reactive sputtering [49, 105] and was as large as those reported by a cold wall-type LPCVD [50] and photo-CVD [13]. The dielectric constant of the films was increased by annealing at 600 °C, ε_r values of 25–35 could be obtained by

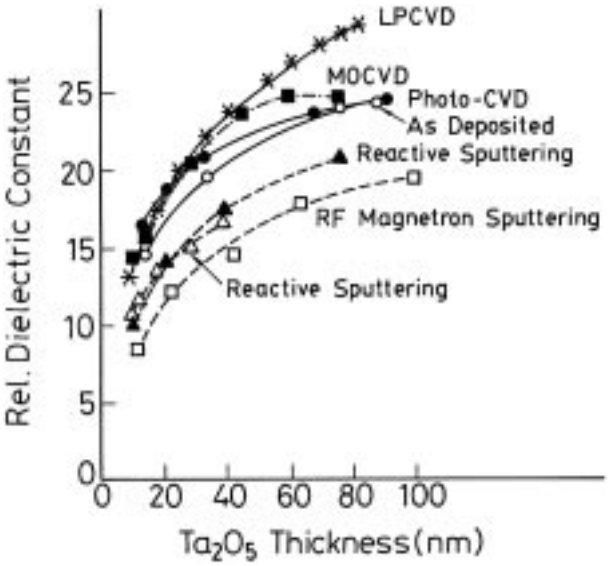

Figure 4 Dependence of relative dielectric constant (ε_r) on the thickness of Ta_2O_5 films deposited by various methods [107].

annealing at 700 °C for a thickness of more than 40 nm. A marked decrease in ε_r with decreasing film thickness was observed also in the annealed films. Similar results were reported for reactively sputtered films [13, 50, 110] and were attributed to the existence of a transition layer between the Ta_2O_5 film and the Si substrates. The transition layer was considered to be a compound consisting of Ta, Si and O atoms.

Park *et al.* [13] observed that the dielectric constant versus annealing temperature curve showed a maximum peak at 750–800 °C resulting from the crystallization. This phenomenon was more pronounced for thicker Ta_2O_5 films. However, the dielectric constant decreased with increased annealing temperature above 800 °C. They explained this phenomenon in terms of the growth of SiO_2 layer at Ta_2O_5/Si interface which was observed by their FTIR and SIMS analyses. The effect of oxidation on the dielectric constant of the Ta_2O_5 films was reported by Park and Im [98]. They showed that the dielectric constant obtained from an $Al/Ta_2O_5/Si$ capacitor depends on the thickness of the oxide and increases with increasing oxidation temperature. This variation was explained in terms of the non-crystalline state which was supported by their FTIR analysis. Further, they claimed that the effect of silicon was dominant for thin Ta_2O_5 (65 nm) and the effect of short-range order was dominant for thick Ta_2O_5 (160 nm). Rapid thermal N_2O annealing (RTN_2O) has been applied to reduce the leakage current in the Ta_2O_5 films prepared by LPCVD [111]. It was reported that the effective dielectric constant decreases with increasing RTN_2O temperature.

Fig. 5 shows the dielectric constants and dielectric loss of Ta_2O_5 films as a function of RTA temperature for 30 s in O_2 ambient reported by Ezhilvalavan and Tseng [88]. The effective dielectric constant of Ta_2O_5 film annealed at 800 °C was larger than the 600 °C or 700 °C annealed film. Similarly, the loss factor showed an increase from 0.01 to 0.017. This suggests that the fully crystalline film has a larger dielectric constant than the partially crystallized film. Furthermore, increasing the RTA processing time for a given RTA temperature resulted in an increase of the dielectric constant as well as the dielectric loss factor from 0.012 to 0.035, as shown in Fig. 6. However, increasing the RTA processing time above 30 s increased the leakage current density. Hence, they reported that the best RTA processing time of about 30 s was found to be optimum for MIM Ta_2O_5 capacitor films in obtaining higher dielectric constant (52), yet preserving relatively low leakage current density of 10^{-10} A cm^{-2} at 100 kV cm^{-1}.

Quite frequently, the dielectric constant reported for Ta_2O_5 film is about 25–35. However, dielectric constants above 35 have also been reported in the literature [112, 113]. For example, Wu *et al.* [112] reported that their Ta_2O_5 films had a dielectric constant ranging from 20 to 45. Pignolet *et al.* [92] reported an O_2RTA processed sample showed a dielectric constant of 45 and Lau *et al.* [70] observed that the O_2 RTA films showed a dielectric constant of 40. Triechel *et al.* [113] reported that the dielectric constant is a function of film thickness and the annealing parameters and for relatively thick Ta_2O_5 films (> 60 nm), a dielectric constant as high as 40 was possible. It is to be noted that Ezhilvalavan and Tseng [88] have used Ta_2O_5 films for their study having a thickness around 100 nm. It may be therefore realized that the dielectric constant of 52 obtained for their Ta_2O_5 films are higher than observed conventionally.

8.2. Dielectric strength

Dielectric breakdown in materials is an important parameter in expressing capacitor performance. Electrical breakdowns are characterized statistically by applying a ramped voltage to the capacitors at a ramp rate of 0.5–1.0 V s^{-1} and observing the leakage current through the oxide. As the electric field increases, the leakage current increases sharply, at a critical electric field by showing a deviation from the normal exponential-like increase of the leakage current prior to the occurrence of destructive breakdown. This critical electric field is defined as the breakdown field of the Ta_2O_5 capacitor. The breakdown field for the Ta_2O_5 is dependent on the oxide thickness [114]. The dielectric strength is defined as the average electric field through a film at a leakage current of 1×10^7 A cm^{-2}.

The dielectric breakdown field distribution of

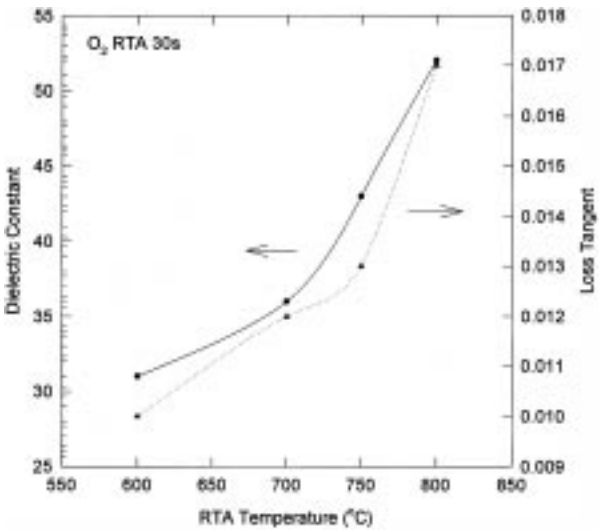

Figure 5 Effective dielectric constant of Ta_2O_5 film versus RTA temperature [88].

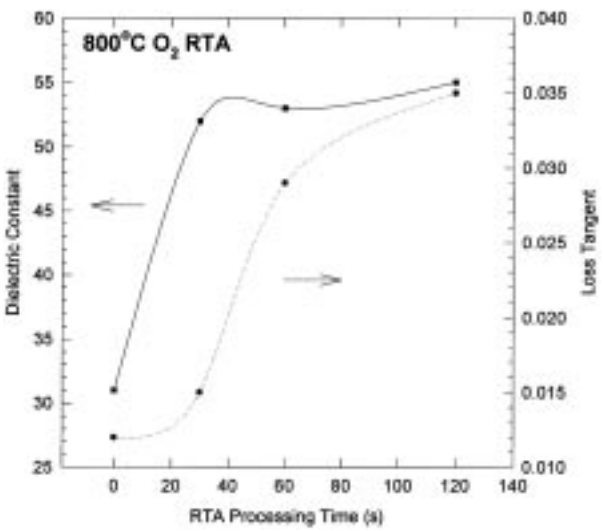

Figure 6 Effective dielectric constant of Ta_2O_5 film versus RTA processing time [88].

anodized, sputtered and sputtered/anodized Ta_2O_5 films were presented by Byeon and Tzeng [97]. The breakdown field for the sputtered oxide under positive voltage on the Ta electrode was about 2.5 MV cm^{-1} or below, which was relatively independent of the oxide thickness. The breakdown field for the anodized oxide on the Ta electrode was about 3.6 MV cm^{-1} in oxide thickness above 120 nm and it was found to decrease when the oxide thickness was decreased, whereas the sputtered/anodized oxide showed much higher breakdown fields between 6.2 and 6.5 MV cm^{-1} and showed little thickness dependence. The higher breakdown strength and narrow breakdown distribution in the sputtered/anodized oxide was explained as a result of the weak spots existing in the initial sputtered oxide being sealed as well as more complete oxidation of weakly oxidized spots after anodic reoxidation.

The dielectric strength of the Ta_2O_5 films was found to depend on the Ta_2O_5 formation temperature [115]. For Ta_2O_5 films oxidized at 490 °C for 1 h in dry O_2, dielectric strengths of 2 MV cm^{-1} up to 4.5 MV cm^{-1} were observed. The greatest number of capacitors had a breakdown strength of 3.0–3.5 MV cm^{-1} in this case. It appears from their breakdown data that the dielectric strength of the Ta_2O_5 films depend in an inverse way on the leakage current which was observed for the same film, i.e. for Ta_2O_5 films with lower leakage, a greater dielectric strength was reported.

A decrease of dielectric breakdown strength of Ta_2O_5 film after high temperature heat treatment has been a serious problem when attempts were made to introduce the film in ULSI fabrication process. Table VI shows the comparison of the properties between amorphous and crystalline Ta_2O_5 films. Nishioka *et al.* [85] compared the dielectric breakdown strength dependence of dry oxygen heat treatment temperature at different Ta_2O_5 thicknesses. Their results showed that the Ta_2O_5 film with a thickness of 100 nm crystallizes at temperatures higher than 600 °C resulting in the reduction of breakdown strength. On the other hand, the 20 nm thick film maintains a high breakdown strength and amorphous state even after heat treatments up to 1000 °C.

The breakdown fields of capacitors fabricated by different techniques were compared by Mohammed and Morgan [116]. The breakdown fields of anodic Ta_2O_5 films and an unimplanted sample were 1.07–1.5 MV cm^{-1} and 0.6–0.96 MV cm^{-1} respectively. This is much lower than for the ion implanted samples (the breakdown field was 3.2–4.4 MV cm^{-1}). The breakdown in anodic and unimplanted films was explained as a result of (i) the technique used for fabrication of Ta_2O_5 films and (ii) the defects (pin-holes) and other impurities in which aluminum and tantalum were likely to enter the microfissures and pores in the oxide films resulting in capacitors with lower breakdown fields.

TABLE VI Comparison of the properties between amorphous and crystalline Ta_2O_5 films

Properties	Amorphous	Crystalline
Leakage current density	10^{-5}–10^{-8} A cm^{-2}	10^{-10} A cm^{-2}
Dielectric constant	20–35	25–52
Dielectric strength	3–5.4 MV cm	2–3 MV cm^{-1}
Capacitance per unit area	4–6 fF μm^{-2}	5.5–6 fF μm^{-2}
TDDB lifetime	$\gg$ 10 years	$\geq$ 10 years

The correlation between dielectric strength and ε_r in Ta_2O_5 films annealed at 850 °C was reported by Zaima *et al.* [51]. The phenomenon that a larger dielectric strength corresponds to a smaller dielectric constant was found to be closely related to the thickness of the interface transition layer which consists of Ta, Si and O atoms. It was stated that the increase in transition layer thickness leads to a decrease in the dielectric constant for a whole film and to an increase in the effective dielectric strength, because the voltage applied to the pure Ta_2O_5 film region decreases. They proposed that the most appropriate film should have an ε_r of 16–20 and a dielectric strength of 2–3 MV cm^{-1}.

8.3. Time dependent dielectric breakdown (TDDB)

Lifetime extrapolation using constant voltage stress time dependent dielectric breakdown studies predicts the 10 years lifetime at 1 V operating voltage. TDDB is also referred to as resistance degradation of dielectrics which shows a slow increase of leakage current under a d.c. field stress. TDDB is characteristic of the intrinsic materials, the procedure and quality of the process and electrode materials [117, 118]. The reliability of Ta_2O_5 films is evaluated by comparing the TDDB characteristics with those of SiO_2 films. Fig. 7 shows the effective electric-field dependence of the time to 50% failures for Ta_2O_5 capacitors compared with SiO_2 capacitors as reported by Nishioka *et al.* [85]. The Ta_2O_5 films were annealed in dry O_2 at 800 °C for 30 min and its thickness was $\sim$ 5.3–20 nm. The effective electric field in Fig. 7 is defined as

$$E_s = CV/\varepsilon_o\varepsilon_s S \quad (1)$$

where C and V are the capacitance and the applied voltage, respectively, ε_v and ε_s are the permittivity in vacuum and the dielectric constant of SiO_2 (3.8), respectively, and S is the area of the capacitor. From

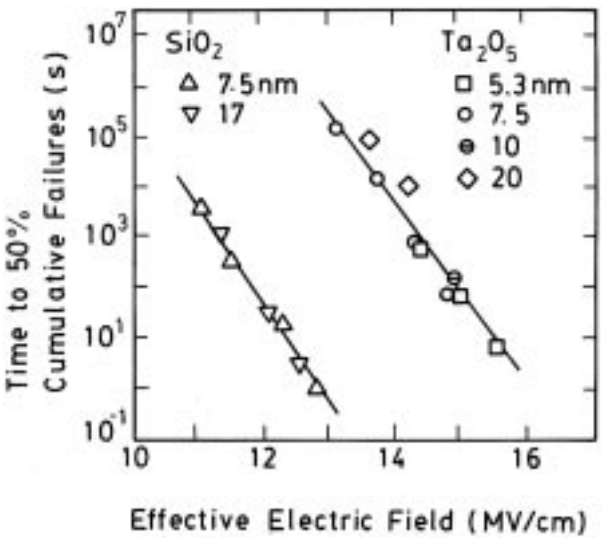

Figure 7 High reliability of weak spot oxidized (800 °C, 30 min) Ta_2O_5 capacitor analysed by the TDDB method [85]: △, 7.5 nm; △, 17; □, 5.3 nm; ○, 7.5; ⊖, 10; ◇, 20.

the above figure Nishioka and co-workers [49, 85] pointed out that the time to 50% cumulative failure for the Ta_2O_5 capacitor was about five orders of magnitude larger than that for SiO_2 capacitors compared under the same effective conditions.

The TDDB for Ta_2O_5 has been measured by Byeon and Tzeng [97] by applying either constant current or positive voltage to the Ta electrodes. As the Ta_2O_5 was stressed by either current or voltage, a rapid decrease of voltage or a sharp current spike prior to destructive breakdown was observed from instabilities in the *V–t* or *I–t* curve during the time-domain measurements. The time showing unstable voltage or current was defined as the time to breakdown. Byeon and Tzeng [97] compared the TDDB properties of anodized, sputtered and sputtered/anodized Ta_2O_5 films (80 nm) and they showed that the sputtered/anodized oxide performed better TDDB properties in both current and voltage stress conditions and it was a most promising oxide in terms of long-term reliability. Kamiyama *et al*. [15] reported a highly reliable 2.5 nm Ta_2O_5 films for stacked cylindrical polysilicon capacitors of 256 Mbit DRAM. Their TDDB tests showed that the capacitors have a reliability as high as 10 years and more for 1/2 $V_{CC} = 1.0$ V/100 °C operating conditions. TDDP lifetime characteristics for the short time of 30 s to 120 s O_2RTA processed Ta_2O_5 film have been reported [88]. The Ta_2O_5 film capacitor with 30 s O_2RTA processed film showed a longer lifetime than long annealed films.

8.4. Capacitance

As the dimension of DRAM is scaled down, the storage capacitor area is inevitably reduced. A large enough charge should be maintained in order to prevent soft errors for DRAM operation. Capacitor dielectrics like Ta_2O_5 having a high dielectric constant will eliminate this problem and enable a further shrinkage of capacitor area. Maximum charge storage capacity per unit area, i.e. $Q = CV_{BD}$, is calculated by multiplying the capacitance C by the statistically measured average breakdown voltage V_{BD} of Ta_2O_5 capacitors. The thickness dependence of the maximum charge storage capacity of Ta_2O_5 capacitors were analysed by Byeon and Tzeng [85]. It was reported that the anodized oxide with an oxide thickness above 80 nm exhibits higher storage capacity than the sputtered oxide. However, the storage capacity for the anodized oxide decreased dramatically with decreasing oxide thickness because of a decrease in breakdown field and the sputtered anodized oxide showed much higher storage capacity than other oxide capacitors.

Nishioka *et al*. [51] presented the relationship between film thickness and capacitance for the Ta_2O_5 film after weak spot oxidation (800 °C, 30 min) compared to that for the SiO_2 film and found that the capacitance of the Ta_2O_5 remains high. Fig. 8 shows the change of capacitance per unit area with the annealing temperature for a film thickness of 26–48 nm reported by Zaima *et al*. [98]. The capacitance of the films annealed at 600–800 °C was larger than that of the as-deposited films. At temperatures above 800 °C, however, the capacitance decreases rapidly with increasing annealing temperature.

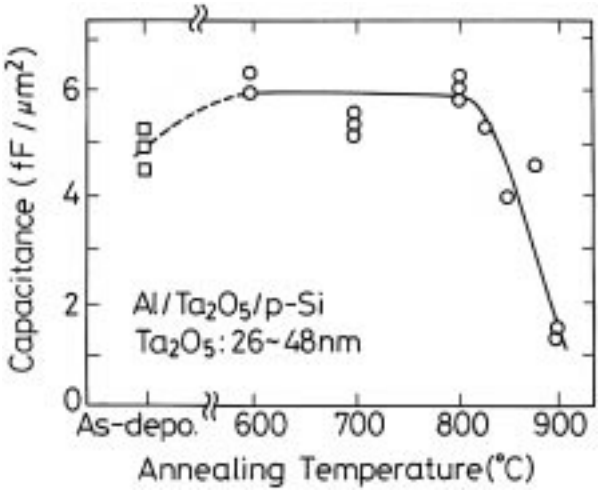

Figure 8 Change of capacitance per unit area with annealing temperature. The Ta_2O_5 thickness are 26–48 nm [51].

This was related to the growth of an SiO_2 layer at the Ta_2O_5-Si interface. This was supported by their Auger electron spectroscopy results showing the pile-up of Si atoms at the interface for the samples annealed above 900 °C. They have obtained the same result by annealing in an N_2 ambient. It was proposed that the SiO_2 formation was due to the oxidation of Si by Ta_2O_5 at the interface because of a difference in the heat of formation between Ta_2O_5 (-100 kcal mol^{-1}) and SiO_2 (-103 kcal mol^{-1}) which was unavoidable at high temperatures. In spite of a decrease in dielectric constant for the thinner range, as seen in Fig. 4, their results showed that the capacitance increases monotonously with decreasing film thickness. For a thickness of 20 nm, the capacitance of Ta_2O_5 films was four times larger than that of SiO_2 films, which indicates the potential application to ULSI.

8.5. *C–V* characteristics (flat band voltage)

The net charge residing in the Ta_2O_5 bulk and/or Ta_2O_5/Si interface region could be changed by the application of a bias vltage to an MIS capacitor during the *C–V* measurement. Park and Im [98] showed that the stretch-out of the *C–V* curve was more significant for Ta_2O_5 oxidized at low temperature and for the Ta_2O_5 with large thickness. They suggested that more donor-type interface states, which are neutral when filled with electrons and positively charged when empty, were present at the Ta_2O_5-Si interface for thicker Ta_2O_5 and the Ta_2O_5 that was oxidized at low temperature and that the interface states decrease with increase in oxidation temperature. It is known that the flat band voltage, V_{fb}, depends on the interface state as well as the bulk trap charge. In order to eliminate the effect of the interface state, they repeated the *C–V* measurements for Al/Ta_2O_5/SiO_2/p-Si capacitors and they observed that all *C–V* curves were shifted towards more negative gate voltage without any distortion in depletion and accumulation regions as the oxidation temperature was increased. This implied that the Si-SiO_2 interface state was not affected by thermal oxidation of tantalum, while the charge state in Ta_2O_5 was affected. The V_{fb} values obtained from the *C–V* curves by Peak and Im

[46, 115, 119] showed that the absolute value of V_{fb} increased as the oxidation temperature was increased.

Oehrlein and co-workers [13, 98] observed that V_{fb} was positive for a specimen oxidized at 430 °C and that it becomes negative when the oxidation temperature exceeds 550 °C. These results were explained in terms of the reduction in oxygen deficiency of Ta_2O_5 films, with Rutherford backscattering measurements revealing a greater oxygen-to-tantalum ratio for Ta_2O_5 films formed at higher oxidation temperature. If the above suggestion was correct, V_{fb} must be linearly related to the Ta : O ratio, According to Oehrlein's results, the Ta : O ratio becomes less for higher annealing temperatures in O_2, while this was negligible for N_2. However, Park and co-workers [98] observed that V_{fb} decreases linearly in negative voltage with increase in annealing temperature regardless of the ambient. Hence, they concluded that the decrease in net charge residing in Ta_2O_5 is not only caused by the reduction in oxygen deficiency in Ta_2O_5 but also caused by a decrease in defects, such as broken bonds or non-bridging oxygen, as a result of improvement in the short-range order of the non-crystalline structure.

The effect of constant gate voltage stress on the flat band voltage of a metal insulator semiconductor (MIS) capacitor with Ta_2O_5 of 19 mm thick as a function of annealing temperature was reported by Park and Im [51]. It can be seen that as the annealing temperature exceeds 750 °C, ΔV_{fb} showed a sharp increase, which was related to the negative charges trapped in Ta_2O_5 bulk, Ta_2O_5/Si and Ta_2O_5/SiO_2 interfaces. Further, they suggested that the increase in ΔV_{fb} of samples annealed above 750 °C could be caused by an increase in trapping charges with the annealing temperature up to 850 °C and then increased with further increase in annealing temperature. This phenomenon was explained in terms of the growth of an SiO_2 layer at Ta_2O_5/Si interface and variation in the defect density during annealing.

The interface density of the film annealed at 850 °C was of the order of $10^{12}\,cm^{-2}eV^{-1}$ at mid-gap and it was reported that a higher temperature of annealing is essential for the reduction of interface density [120]. This was consistent with their results with the formation of the transition layer at 850 °C. It was then considered that the Si-O bonds were formed at the interface between the Ta_2O_5 layer and the Si substrate which resulted in the formation of a very high-quality interface. They also found that the interface density of the film was less than $1 \times 10^{11}\,cm^{-2}eV^{-1}$ which cannot be deduced by Terman's method and these results were related to the formation of SiO_2 at 900 °C.

The $Si\text{-}Ta_2O_5$ interface contains a transition region, both in terms of atom position and stoichiometry. Various charges and traps are associated with the thermally oxidized Ta, some of which are related to the transition region. A charge at the interface can induce a charge of opposite polarity in the underlying silicon, thereby affecting the ideal characteristics of the MOS (metal-oxide-semiconductor) device. This results in both yield and reliability problems. The fixed oxide charge Q_f is located in the oxide within approximately 3 nm of the $Si\text{-}Ta_2O_5$ interface. Q_f cannot be charged or discharged. Its density ranges from $10^{10}\,cm^{-2}$ to $10^{12}\,cm^{-2}$, depending on oxidation and annealing conditions. The value of this charge can be determined using the *C–V* analysis. The fixed oxide charge density of thermally grown tantalum oxide on silicon was found to be higher than on the $Si\text{-}SiO_2$ interface [85]. However, the properties of the $Si\text{-}Ta_2O_5$ interface were comparable with those obtained by conventional oxidation of silicon.

8.6. Leakage current

Leakage current in Ta_2O_5 films limit applications to ULSIs in terms of storage characteristics. Several studies have been reported on the electrical properties of Ta_2O_5 films. Although as-deposited sputtered Ta_2O_5 films have low leakage current in the amorphous state, the leakage current is drastically increased by high temperature annealing. Various postdeposition annealing techniques, such as furnace O_2 [121], plasma O_2 [122], UV-O_3 [15], rapid thermal oxidation (RTO) [111] and RTN_2O [106] annealing have been proposed to reduce the leakage current and improve the quality of Ta_2O_5. During the thermal treatment in an oxygen containing ambient, oxygen diffuses into the Ta_2O_5 films, leading to repair of oxygen vacancies, elimination of organic inclusions and reduction of weak spots in the Ta_2O_5 films.

The oxidation of the Si substrate during the initial stage of deposition plays one of the major roles in the transition region formation. Fig. 9 indicates the variations in leakage current with the initial oxygen partial pressure [107]. A remarkable increase of the leakage current was observed with the decrease of initial oxygen partial pressure. The observed changes in the leakage current were related to the variation in the thickness and the composition of the transition region at the interface. This indicates that the reaction between oxygen in the sputtering gas and the Si substrate is one of the main mechanisms in transition region formation and that this transition region plays a dominant role in determining the

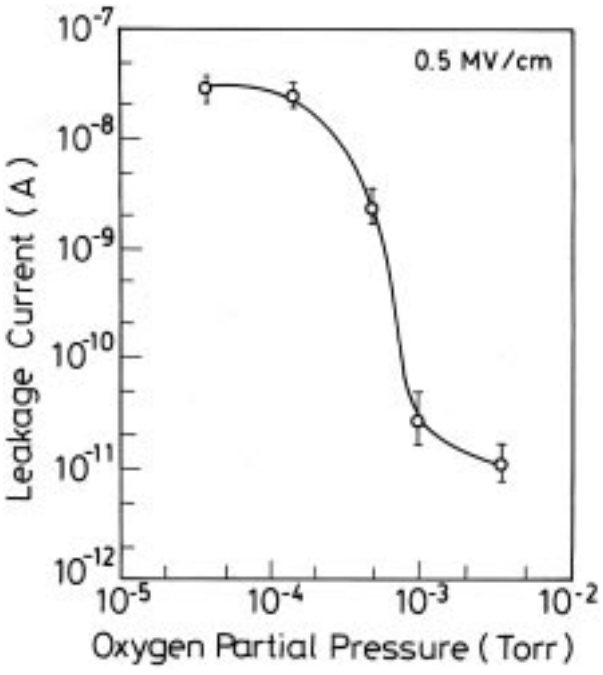

Figure 9 Variations in leakage current with oxygen partial pressure during the first minute of deposition. The applied voltage is 0.5 MV cm^{-1} [106].

leakage current characteristics. The leakage current of the formed Ta_2O_5 film decreased drastically with annealing in the presence of both UV-irradiation and an oxygen ambient after deposition (p-O_2 annealing), when the underlying layer contains Si [107]. The leakage current density was 10^{-8} Acm^{-2} at an electric field of 4 MV cm^{-1}.

p-O_2 annealing is a promising method for the fabrication of Ta_2O_5 films with a low leakage current and a high dielectric constant because it is not accompanied by a significant decrease in the dielectric constant. The leakage current density of various dielectric films as a function of the effective electric field is shown in Fig. 10. It was shown that the photoprocessed Ta_2O_5 film has the lowest leakage current among dielectric films [107]. It was reported that the leakage current of Ta_2O_5 films was decreased by increasing the annealing time, substrate temperature and oxygen pressure in the chamber. An interesting observation is that the p-O_2 annealing was effective for MIM structure capacitors when the underlying layer of Ta_2O_5 film was a material containing Si, such as WSi. However, the effect was small when the underlying layer did not contain Si, such as TiW [107].

The leakage current in Ta_2O_5 film that was deposited by a clear sputtering system [109], which installs a high purity target was far lower than that of film deposited with a conventional target and the leakage current increase caused by using a metal as a bottom electrode can be suppressed by reducing the electrode asperity. Using 2 nm Mo as the bottom electrode, Hashimoto *et al*. [109] claimed that the leakage current was reduced drastically. Isobe and Saitoh [95] found that the leakage current of Ta_2O_5 drastically decreased with O_3 annealing, while little reduction was observed with O_2 annealing. The leakage current reduction was larger at 400 °C than that of 300 °C, probably because of oxygen diffusing into the film. The leakage current density of this extermely thin film was found to be reduced from more than 10^{-3} to 10^{-9} A cm^{-2} at 3 MV cm^{-1}. The species responsible for the reduction of leakage current in O_3 annealing was active oxygen atom radicals created by a thermal dissociation of ozone. A probable mechanism for the O_3 annealing effect was attributed to the reduction of oxygen vacancies in the Ta_2O_5 film by reactive oxygen atom radicals.

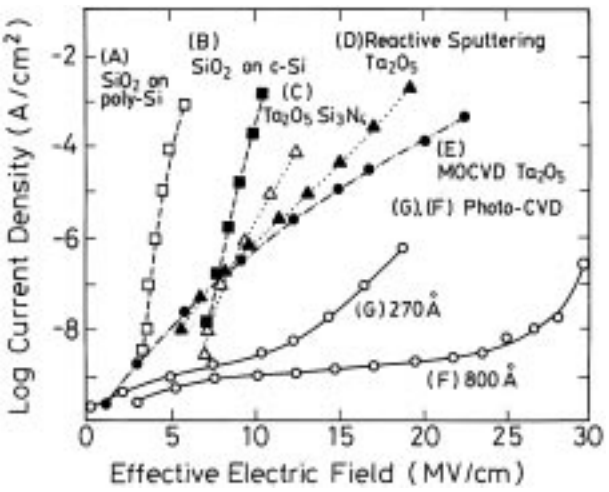

Figure 10 Leakage current density of various dielectric films as a function of the effective electric field [107].

Their previous work revealed that a low concentration of TiO_2 doping into the film could also reduce the leakage current [50]. In that case, it seems that oxygen vacancies were compensated by Ti^{4+} ions which were substitutionally incorporated into Ta^{5+} sites In the film. This suggests that the concentration of oxygen variances strongly affects the leakage characteristics of the CVD Ta_2O_5 film. To explain the relation of the leakage and the trap density more clearly, it will be necessary to measure the trap density in Ta_2O_5 before and after annealing by methods such as photoenhanced electron injection, deep level transient spectroscopy (DLTS), etc. In conclusion, the leakage current which has been considered as a serious problem of LPCVD-grown Ta_2O_5 film can be reduced remarkably with O_2 or O_3 annealing.

The post deposition annealing was very effective for a reduction of leakage current, as reported by Zaima *et al*. [51]. This was related to the crystallization of the annealed films. The decrease in leakage current in the crystallized film was opposite to the cases of reported reactive-sputtered films and oxidized Ta films [48]. The annealing at 900 °C leads to low leakage current $< 1 \times 10^{-11}$ A cm^{-2}, which they claim resulted from the formation of SiO_2 at the interface. Byeon and Tzeng [97] compared the leakage currents of the anodized, sputtered and sputtered/anodized Ta_2O_5 films. For the anodized and the sputtered oxides, the measured leakage currents rise very rapidly at low applied voltage in contrast, the onset of leakage currents for the sputtered/anodized oxide occurs at much higher electric field.

A two-step annealing technique for leakage current reduction in CVD-Ta_2O_5 film was demonstrated by Shinriki and Nakata [96]. The first annealing (UV-O_3) of the two-step annealing process improves the as-deposited Ta_2O_5 film, resulting in the reduction of leakage current. The UV-O_3 annealing treatment was claimed as the most effective method for reducing the leakage current compared to UV-O_2 and O_3 annealing treatments. This reduction was proposed to be due to the reduction between the oxygen vacancies and the oxygen atoms excited by the mercury lamp, the second annealing (dry-O_2 annealing) reduced the defect density of UV-O_3 annealed Ta_2O_5 film to less than 0.04 cm^{-2}.

The leakage current of thermally oxidized Ta_2O_5 prepared by LPCVD decreases with increasing annealing temperatures in dry O_2 or N_2 [13]. The reduction of leakage current for samples annealed in dry O_2 was larger than that for samples annealed in N_2. The decrease in leakage current of the crystallized films is contrary to the phenomenon reported by other investigators [48, 85, 94]. The reduction of leakage current after the annealing process was related to the formation of an SiO_2 layer at the Ta_2O_5/Si-interface and the decrease in defects, such as broken bonds and oxygen vacancies, as a result of an improvement in microstructure.

Recently Sun and Chen [111, 123] reported that rapid thermal N_2O annealing (RTN_2O) was the most effective method in suppressing the leakage current of LPCVD grown Ta_2O_5 films, compared to RTO and furnace O_2 annealing treatments. A high RTN_2O temperature will

deteriorate both the low field leakage current and the effective dielectric constant. As a result, it is critical to use optimal RTN_2O conditions such as 800 °C for 60 s to achieve Ta_2O_5 capacitors with low leakage, high capacitance and superior reliability. They also presented a plausible mechanism for the leakage current reduction by RTN_2O annealing, reactive atomic oxygen species (O^+) are generated by the dissociation of N_2O gas at elevated temperature ($N_2O \rightarrow N_2 + O^+$) during the rapid thermal process cycle [124]. These reactive oxygen species diffuse into Ta_2O_5 films and repair oxygen vacancies, thereby leading to a lower leakage current [96]. RTN_2O annealing is a single step process capable of simultaneously providing the excited atomic oxygen species and high temperature annealing. The excited oxygen atoms reduced the degree of imperfections caused by the deficiency of oxygen atoms adjacent to the tantalum atoms [125].

The remaining atomic oxygen recombines into molecular oxygen (O_2). High temperature (800 °C) O_2 annealing reduced the defect density due to weak spots and carbon contamination [96]. On the other hand, they pointed out that furnace O_2 annealing and RTO rely on the diffusion of molecular oxygen (which is less reactive than the atomic oxygen) in repairing the oxygen vacancies of Ta_2O_5 films. They also observed that a furnace O_2 annealing time of 30 min was not as good as annealing for 60 s of RTN_2O in reducing the leakage current. Furthermore, RTO annealing was even less effective than furnace O_2 annealing owing to the insufficient time to allow oxygen molecules to reduce defects.

The effect of RTA processing time duration, i.e. holding time of the films at higher temperature of annealing on the leakage current property of Ta_2O_5 films were studied by Ezhilvalavan and Tseng [88]. Fig. 11 shows the leakage current density as a function of RTA processing time of Ta_2O_5 films processed at 800 °C in O_2 ambient for 30 s to 120 s. It was reported that a shorter processing time $\sim$ 30 s leads to better electrical characteristics by way of lowering the leakage current density

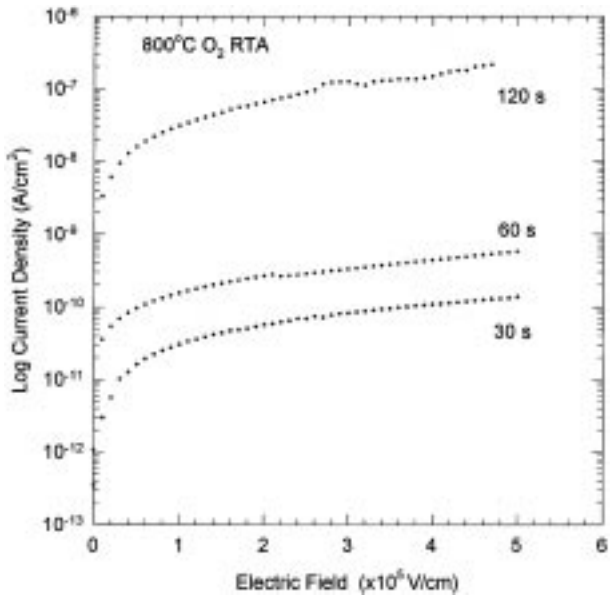

Figure 11 Leakage current density versus applied electric field for Ta_2O_5 film after 800 °C O_2 RTA process at different time duration [88].

from 10^{-7} to 10^{-10} A cm^{-2} at 100 kV m^{-1}. Their results demonstrated that a very short duration of RTA processing around 30 s is sufficient for the complete crystallization of the films and also for reducing the oxygen vacancies, yet minimizing the interface reactions through the grain boundaries.

9. Conduction mechanisms

In the last 25 years, many experiments have been performed to determine the mode of d.c. conduction in Ta_2O_5 films. Experimental results and their interpretation appeared to vary among different investigators. Electronic conduction in thin Ta_2O_5 film has been interpreted in terms of electronic conduction theories. A perennial problem is the question of whether d.c. conduction in controlled by a Schottky emission (SE, electrode-limited or by a Poole-Frenkel (PF, bulk limited) mechanism [126].

One of the main problems that plagued some of the early experimental work is that the Ta_2O_5 films used may exhibit flaw conduction rather than any mechanisms that are operative intrinsically in the oxide [127–129]. In fact, by a very careful preparation technique, Pulfrey *et al.* [44] have shown that the currents measured in their samples were several orders of magnitude smaller than those measured by other workers. Therefore, it is imperative in the discussion of the conduction mechanism in Ta_2O_5 films to ensure that the films under examination are essentially flaw free.

Furthermore, in the interpretation of the experimental data heavy reliance has been placed on the measured slope of the $\log(I) - E^{1/2}$ plot, $d\log(I)/dE^{1/2}$. If the measured value of $d\log(I)/dE^{1/2}$ is close to the Schottky value, the conduction mechanism is considered to be electrode limited (SE process). On the other hand, if the measured value is twice as large as the calculated Schottky value, the conduction mechanism is considered to be bulk limited (PF process). However, Simmons [130] has pointed out that the slope factor alone may be inadequate in determining the mode of conduction and he proposed a model for the bulk conduction where β (the slope) was identical for both of these processes. On the other hand, Mark and Hartman [131] pointed out that in real insulators, it was more probable that a difference in the slope factor β exists for these two different mechanisms and hence PF and SE processes should be distinguishable on the basis of *I–V* measurements.

As Pulfrey *et al.* [132] have recognized, even though the SE and the PF processes were the two most frequently quoted mechanisms for explaining the conduction processes in Ta_2O_5, they were not necessarily the only two operative mechanisms. One must examine the experimental conditions carefully to ensure that one mechanism is truly dominant over the rest. This is extremely difficult without some knowledge of the nature of the metal-Ta_2O_5 interface as well as the energy diagram of Ta_2O_5 that is relevant to the conduction process.

In particular, we have to answer the following questions:

(i) What is the value of the slope factor in flaw-free Ta_2O_5 films? Whereas measurements by Pulfrey *et al.*

[44] and Mead [133] appeared to be in agreement with the calculated Schottky slope. Work by O'Clock [134] appeared to be in disagreement with either the SE or the PF values.

(ii) Is there a substantial decrease in the slope factor as the film thickness decreases? O'Clock [134] suggested that his results showed a gradual transition from bulk-limited condition to electrode-limited conduction, as the film thickness decrease from 80 to 90 nm.

(iii) Is the slope factor sufficient to determine the mode of the conduction process? In particular, can other independent tests be conducted to verify the conclusion?

(iv) If bulk conduction is dominant, can the defect structures which control the conduction process be identified?

Anodic oxidation which has been historically used to grow Ta_2O_5, yields dielectric films which allow ionic flow readily during the growth processes and hence suffer from a high temperature oxygen ion drift phenomena under bias, which results in a large hysteresis in their *I–V* characteristics [45, 133, 145]. Mead [133] published the results of d.c. conduction measurements made on $Ta/Ta_2O_5/Au$ devices where the Ta was metallurgical grade Ta sheet. Very little data was given on the experimental procedure, in particular, the anodization procedure and type of electrolyte were not mentioned. Mead found that, for a given applied field, the current was constant and independent of oxide thickness at both 300 K and 77 K. The logarithm of the current followed a $V^{1/2}$ law over several decreases of current and the slope was claimed to fit the theoretical slope for the PF process. At 77 K, the currents could be explained by a tunnel mechanism and were also reversible (i.e. non-polar). The activation energy in the Ohmic conduction region was ~ 0.07 eV and in the PF region was ~ 0.6 eV. The mechanisms proposed by Mead were electron hopping between localized states at low voltages and high temperatures, the PF effect at high fields and high temperatures and the tunneling of trapped electrons at high fields and low temperatures [133].

A cathodic *J–V* curve for a 10 nm thich anodic oxide on an electron beam evaporated Ta film was shown by Hickmott [135]. The counter electrode was Au with an area of $\sim 10^{-2}$ cm^2. Although this was 10 times that of a comparable sample prepared by Mead, the current density was some 5 orders of magnitude lower at low voltages and about 10% of Mead's value at high voltages. Although the samples exhibit a wide range in leakage current levels, probably due in some part to different electrode materials and area, the general shapes of the *I–V* curves were similar. Standley and Maissel [136] presented some d.c. conduction measurements made, using Au electrodes, on oxides grown on sputtered Ta on glass substrates. They reported that the choice of anodizing electrolyte had no effect on the results but that a brief polarity reversal produced during anodization were improved uniformly across the substrate. Their devices exhibit rather peculiar temperature effects. At room temperature, the anodic currents were very low in comparison with the cathodic currents. As the temperature decreased, the anodic currents increased and the cathodic current decreased until, at 77 K, the devices were symmetric. This is comparable to the devices prepared by Mead.

D.C. conduction results for 190 nm and 320 nm thick anodic oxides, on sputtered β-Ta were reported by Walker [137]. He used contacts of nichrome/copper/palladium and generally used only anodic voltages. When plotted on a log *I*–log *V* plot the characteristics exhibited linear relations, with slopes between 3.7 and 7.5 at higher voltages. Walker interpreted this results in terms of space charge limited (SCL) currents. Although only three oxide thickness were used, the thickness dependence on the currents was consistent with the mechanism. At very high voltages a ''trap filled limit'' characteristic was apparent from which he calculated a trap density of $\sim 10^{18}$ cm^{-3}. However, there is a basic inconsistency in Walker's analysis as the conduction mechanism was interpreted in terms of traps distributed exponentially in energy throughout the band gap and the trap density was calculated assuming either a single trapping level or at least an upper limit on the energy levels of traps. Korinek [138] used the activation energy of d.c. conduction in Ta_2O_5 as a measure of oxide quality. He tested various groups of solid electrolytic capacitors and found that an increasing activation energy was associated with more stable leakage currents and also with better uniformity between samples within a group. It might be pointed out that the activation energies quoted by Korinek did not appear to be corrected for efforts due to field lowering of potential barriers.

Klein and Jaeger [139] carried out some interesting experiments on anodized bulk Ta with semiconducting oxide/electrolyte contacts, i.e. an electrolyte was used to make contact to the semiconducting oxide (Fe_2O_3 or MnO_2) on the Ta_2O_5. The advantage gained by using these oxide/electrolyte contacts was the elimination of the low field breakdown which were usually associated with metal contact while at the same time, the ionic processes, which occur at high fields when using an electrolyte contact were limited. They were thus able to observe electronic conduction at voltages approaching the formation voltage of the oxide. At voltages near the original formation voltage, they observed a uniform electrical conduction which increased roughly experimentally with time. They referred to this as an activation and found that the rate of activation increased rapidly with applied field and was independent of oxide thickness. Klein and Jaeger explained this result by proposing that, during the activation, ion migration was occurring in the oxide. This was visualized in terms of an oxygen deficiency being created near the interface because the electrode limited the availability of oxygen ions. The positive charge of the oxygen vacancies lawers the potential barrier to electron injection at the interface and thus larger electronic currents flow. Although this should lead to Schottky law currents, the results were attributed to the PF effect. O'Clock [134] suggested that his results showed a gradual transition from bulk-limited conduction to electrode-limited conduction as the film thickness decreased from 80 to 9 nm. Nakamura *et al.* [137] presented d.c. conduction results for capacitors formed from β-Ta on a glazed ceramic with a Ta_2O_5 etch stop layer. Their devices were non-polar and at low

voltages displayed an ohmic region. The logarithm of the high voltage currents was proportional to $V^{1/2}$ which was interpreted as being due to a PF effect. Their model involved a donor level at ~ 1.1 eV and a trap level at 0.5 eV. Young [140–142] presented experimental results on the conduction characteristics of thin Ta_2O_5 films formed by r.f. sputtering. His experimental results showed that for a Ta_2O_5 film, the measured slope agrees with the calculated Schottky value, especially for thin films. In contrast, the work of O'Clock [134] shows the slope factor decreases with increasing film thickness. Two independent tests were presented, which showed quite conclusively that the conduction mechanism in Ta_2O_5 films cannot be electrode limited.

The results also showed the abrupt change in slope factor from a modified PF (MPF) related value at low field to a normal PF related value at high field for a Ta_2O_5 film heated in air [143]. Both structural changes and oxygen deficiency were ruled out as causes of this effect and he proposed a small amount of water in the film was needed for the conduction process to be MPF-like and proposed that water was acting as a neutral trap in Ta_2O_5 films. Kaplan *et al*. [144] reported the d.c. conduction mechanism for Ta_2O_5 films deposited by oxygen-assisted pyrolysis. From the low activation energy and the value of the dielectric constant evaluated for the Ta_2O_5 films, they suggested that the conduction was bulk limited with a PF mechanism at low current densities and a transition towards a space charge-limited current at high current densities.

The conduction mechanism for thermally oxidized Ta films deposited by vacuum evaporation have been reported [115, 119]. With regard to detailed current transport models for Ta_2O_5, they pointed out that the overall ln J versus T behaviour of Ta_2O_5 on Si films appear to be similar to the behaviour of Si_3N_4 films on Si [115, 119]. whereas for Si_3N_4 at high temperatures and high fields, current conduction according to the PF effect, seems to dominate [119, 145], as the ln J versus E data for Ta_2O_5 appear more difficult to interpret. They claimed that by plotting typical I–V data as $\ln(J/E)$ versus $E^{1/2}$ gives curves which exhibit several straight line segments of various slopes and a linear behaviour of $\ln(J/E)$ versus $E^{1/2}$ imply PF behaviour. The location and the slope of the straight line portions for a particular Ta_2O_5 specimen were found to depend on the oxidation conditions used during formation of the specimen, e.g. oxidation temperature. The value of the relative permittivity evaluated from the slope of the linear portion of $\ln(J/E)$ versus $E^{1/2}$ at high fields could indicate a PF effect, whereas for lower fields, the value was not consistent. Also, they have mentioned that for a much greater range of electric field values than for which PF behaviour appears to be observed J correlates very well to $E^{6.4}$. This was related to the space charge limited conduction mechanism. They refrain from a more thorough discussion of conduction mechanism because of their limited data.

The electrical characteristics of the Ta_2O_5 films formed by three different techniques: thermal, anodic and O^+-implantation-enhanced thermal oxidation were compared by Mohammed and Morgan [116]. The d.c. conduction mechanism in all the films was claimed to be consistent with the bulk-limited (PF) effect. The dependence of the $\log(J/E)$ on $E^{1/2}$ was found to be linear over 5 decades of current. This linear dependence was a characteristic for a lowering of the coulombic potential barrier in the bulk of the material (thermal excitation of electrons from traps into the conduction band of the insulator) and therefore they claimed that the oxide films exhibited PF conduction mechanism. It was also reported that the values of the field lowering coefficient, α, for both anodic oxide films and implanted tantalum obtained from the slope $[d\log(J/E)]/dE^{1/2}$ of $\log(J/E) - E^{1/2}$ plots were in agreement with the theoretical value of α. This agreement was less satisfactory in the case of unimplanted tantalum.

In contrast, for unimplanted tantalum, if a blocking contact exists at the Al-Ta_2O_5 interface, the bulk-limited current was large. This gives rise to the formation of a depletion region near the interface. In the Schottky effect the rectification is very high; that is the asymmetry should cause a large variation in I–V characteristics as in a metal-semiconductor Schottky barrier [118] and metal-niobium structures [117]. The Ta_2O_5 films formed by the ion implantation technique did not give rise to the formation of a depletion region at the Al-Ta_2O_5 interface. This was in contrast to those formed by thermal oxidation. Further, they argued that the high leakage current density in anodic films was consistent with the existence of a sub-oxide of tantalum and other impurities [44, 134, 141, 146]. This appears to provide a higher conductivity compared with the Ta_2O_5 films. If, in a sample, there are many of these impurities, the leakage current density would increase more rapidly. This was in contrast with the implanted tantalum in which the leakage current density was much lower than that of an anoidic oxide and unimplanted tantalum. Therefore, it was concluded that the results described for ion-implanted tantalum were consistent with a mechanism in which only electrons enter the Ta_2O_5 films.

The temperature dependence of leakage in sputtered Ta_2O_5 films (10–30 nm) on Si substrates with an interfacial SiO_2 layer has been studied by Banerjee *et al*. [147], for temperatures between -50 and $+100\,^{\circ}$C and for electric fields between 0 and 2 MV cm^{-1}. The activation energy of leakage current versus voltage relationships have been used to identify various high field conduction mechanisms. They showed that there were two distinct activation energies (and therefore two different dominant conduction mechanisms) for the low temperature (-50–$25\,^{\circ}$C) regime and high temperature 50–$100\,^{\circ}$C) regime. Also, the characteristics were fairly independent of film thickness indicating that the structure and electrical properties were independent of film thickness.

They observed that the conduction mechanism was relatively independent of temperature at low temperatures while there was a strong dependence in the temperature range 50–$100\,^{\circ}$C (Fig. 12). One possibility was that at high fields, a field emission mechanism was operative at low temperatures while a PF effect was dominant at high temperatures [133]. A linear relation showed by plotting $\log(I/V^2)$ versus (I/V) and the activation energy in the low temperature region was small, from which they strongly suggested that the

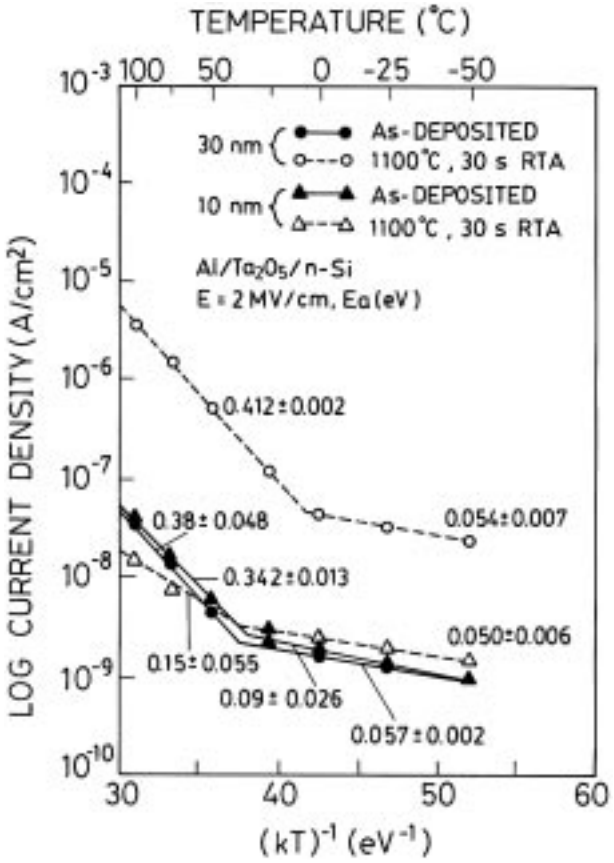

Figure 12 Arrhenius plots of leakage current for 10 and 30 nm Ta_2O_5 films before and after 30 s RTA at 1100 °C in an Ar ambient [147].

leakage was due to a tunneling process such as field emission of trapped electrons into the conduction band of Ta_2O_5. In the high temperature range, since the activation energy was high, the dominant mechanism at high temperature and high fields was claimed to be a PF bulk-limited mechanism [148].

From the capacitance and dissipation factor measurements, the 20 nm Ta_2O_5 film was estimated to have a relative dielectric constant of $\varepsilon_r = 13.1$. This value of $\varepsilon_i (= \varepsilon_r \varepsilon_o)$ substituted in the plot of $\log(I/V)$ versus $V^{0.5}$ yields $n = 1.1$, which they claim point to SE rather than PF transport. However, they obtain a slightly better fit of the plot $\log(I/V)$ versus $V^{1/2}$ instead of $\log I$ versus $V^{1/2}$. Also, the observed dependence of current upon temperature was not as steep as predicted by the SE process; it agrees better with the PF form. Further, they proposed that a close examination of the PF transport indicates that, while the slope was indeed twice that for SE for heavily compensated material, with a donor and acceptor trap concentration greater than the conduction electron, $n = 1$ for an insulator with few compensating traps. In practice n lies between 1 and 2 depending on the degree of compensation present [149]. Although in Ta_2O_5 grown by anodic oxidation $n = 2$ because of the large density of distributed traps, it was possible that there are relatively few traps in as-deposited sputtered Ta_2O_5, leading to $n = 1$.

Another method to distinguish between PF and SE mechanisms is to examine if the current is electrode limited or bulk limited. A true bulk-limited mechnism should be independent of the polarity of the voltage, while a SE mechanism would be sensitive to the bandedge discontinuity between the electrode and the insulator and should show a polarity dependence if the two electrodes on the two sides have different work functions. The current-voltage relationship for Al-Ta_2O_5-n^+-Si was observed to be independent of the polarity of the applied voltage. However, since the work function of Al was close to that of n^+-Si, a SE mechanism would also be independent of polarity for this structure. For Al-Ta_2O_5-p^+-Si, where there was a 1.1 eV work function difference between Al and p^+-Si, the leakage current was observed to be independent of the polarity of the applied voltage. Based on this, Banerjee *et al.* [147] strongly suggested that the current was indeed bulk limited, and therefore was due to PF mechanism.

Further, they observed that the current densities were much higher for the Al-Ta_2O_5-Ta (MIM) capacitor than for the Al-Ta_2O_5-n^+-Si (MIS) capacitors. One possibility was there may be a native interfacial SiO_2 layer for the MIS capacitors. This native SiO_2 layer may be responsible for lowering the electric fields in Ta_2O_5, and therefore lowering the leakage currents. An interfacial SiO_2 layer grown by oxidizing the Ta_2O_5 film in the Al-Ta_2O_5-n^+-Si (MIS) capacitors at 900 °C for 30 min in a dry O_2-ambient was reported by Banerjee *et al.* [147]. Hence, they concluded that the oxidation process indeed reduced the activation energy (0.136 eV), indicating one dominant conduction mechanism over the entire temperature range. The SiO_2 layer dominates the conduction process and changes the high temperature PF mechanism in the Ta_2O_5 to a Fowler-Nordheim (FN) tunneling mechanism throughout the entire temperature range.

The electrical properties and the conduction mechanism of Ta_2O_5 films deposited by LPCVD and then annealed at temperatures ranging from 600–900 °C in O_2 were reported by Zaima *et al.* [150]. They explained the *I–V* characteristics in Fig. 13 by dividing the curve into three regions. Region A, showed the ohmic behaviour. This behaviour was related to the hopping conduction mechanism in a low electric field, because the as-deposited film was thought to have so many defects that a thermal excitation of trapped electrons

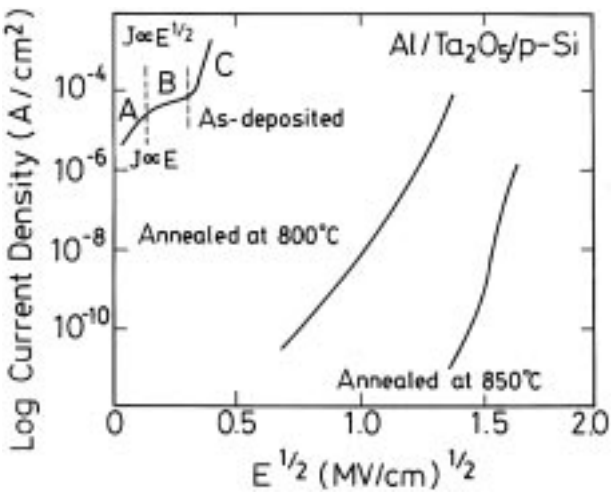

Figure 13 Leakage current density for Ta_2O_5 film as-deposited and annealed at 800 °C as a function of the square root of applied electric field at room temperature [150].

from one trap site to another dominates transport in the films. In region B, the current was proportional to the square root of the applied electric field and the current in region C would be dominated by electron avalanche, because the current increased markedly with a small increase in the applied electric field.

As seen in Fig. 13, a large reduction of leakage current can be observed after high-temperature annealing. The current flowing in the films annealed at 600–800 °C was related to a bulk-limited current at room temperature. Since the main features of the *I–V* characteristics did not depend on the polarity of the applied voltage. Fig. 14 shows Arrhenius plots of leakage current density for the films annealed at 700 °C and 800 °C at an applied electric field of 0.9 MV/cm. For the film annealed at 700 °C, a linear relationship between log J and $1/T$ can be observed and there exist two regions in the films annealed at 800 °C. They claimed that the leakage current obeyed the Arrhenius law at the high temperature range above 130 K and was independent of the measurement temperature at the low temperature range, below 130 K.

The bulk-limited conduction with an activation energy was considered to be either PF type or hopping type. The estimated dielectric constant was two orders of magnitude smaller than the static value obtained from *C–V* characteristics. This means that the conduction with an activation energy as seen in Fig. 14 cannot be explained by the PF conduction. Further, they observed that the level of hopping current was very dependent on the annealing temperature. The current density in the film annealed at 800 °C was smaller by a factor of 10^{-4} than that at 700 °C. Because the activation energies of hopping conduction in these films were observed to be equal, within the experimental error, and the mean hopping distance was little dependent on the annealing temperature, the ratio of current density in these films indicates the ratio of carrier density, n. Using this fact, they suggested that the density of defects with a shallow energy level was reduced by the high temperature annealing. The reduction of hopping current results in the appearance of the region where the current was independent of measurement temperature. It was suggested that the conduction mechanism in this region might be due to tunneling.

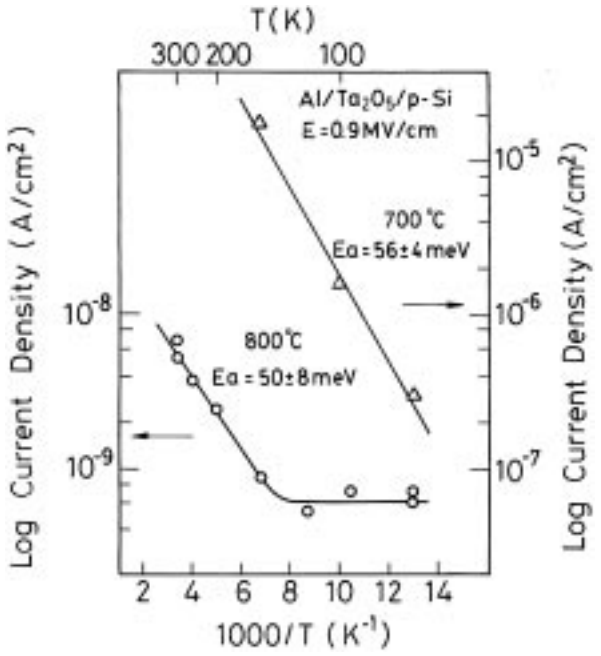

Figure 14 Temperature dependence of leakage current density for Ta_2O_5 films annealed at 700 °C (32 nm) and 800 °C (26 nm). The applied electric field is 0.9 MV cm^{-1} [150].

Further, they proposed that the conduction mechanism in the films annealed above 850 °C cannot be explained by the PF and the hopping conduction mechanism, since ε_r and hopping distance (a) have unacceptable values. The *I–V* characteristics in the FN plot $\log(J/E^2)$ versus $1/E$ for films annealed at 850 °C and 900 °C exhibited a linear relationship which indicated that the current was dominated by FN tunneling conduction. The results of Zaima *et al*. [150] have shown that the dominant conduction mechanism at room temperature was hopping conduction. Annealing at temperatures above 800 °C leads to a decrease of leakage current and the conduction mechanism changed to FN tunneling. More recently, Ezhilvalavan and Tsang [151] investigated the leakage current mechanisms of amorphous and polycrystalline Ta_2O_5 films. They unambiguously differentiated experimentally the ES and PF mechanism responsible for electrical transport at different electric field regimes in Ta_2O_5 films. Their *I–V* measurements displayed ohmic behaviour at low electric fields (100 KV cm^{-1}). On the other hand the Schottky mechanism dominated at the intermediate fields (100–350 kV cm^{-1}) and Poole-Frenkel becomes predominant at high fields (> 350 kV cm^{-1}).

10. Summary and future trends

We have briefly presented the current development of Ta_2O_5 thin films, including the device applications and synthesis-processing methods. Most of the studies accomplished so far have their focus on the understanding of film processing conditions in relation to structure-property characteristics. The above investigations suggest that satisfactory results can be obtained for Ta_2O_5 films deposited by reactive sputtering, photo-CVD and LPCVD. However, LPCVD is expected to be more appropriate for future high density device applications owing to its good step coverage. The maximum dielectric constant and low leakage current density obtainable with LPCVD-Ta_2O_5 films are better than those of other processing methods. Additional investigations are required to optimize processing parameters so that highly oriented Ta_2O_5 films can be obtained at lower deposition temperatures and their properties can be improved.

This review demonstrates that Ta_2O_5 films are appropriate for advanced DRAM applications. A more thorough understanding of the processing methods, electrical characteristics, interface properties, formation and reduction of oxygen vacancies, nature, type and densities of interface states in relation to the reliability of Ta_2O_5 film capacitors and development in process integration is necessary for high density DRAM applications. On the other hand, improving material properties and enhancing densities, manufacturability and reliability are prerequisites for DRAMs to make a major market impact.

The development of a new post-deposition annealing technique that employs O_2 or N_2O RTA to reduce the leakage current of CVD Ta_2O_5 thin films and to obtain the most reliable time-dependent dielectric breakdown, development of highly manufacturable process technology for reliable 256 and 1-Gbit DRAMs using Ta_2O_5 dielectric on poly-Si cylinder and fabrication of 0.5 μm high crown capacitor with crystallized Ta_2O_5 dielectric film are some of the major areas for the future generation of DRAMs for ULSI applications. Attributed to the advancement of thin film synthesis technology and the principles of miniaturation/integration, Ta_2O_5 thin films will remain as a fertile field of research and development, full of application potential and rich in science.

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References

1. M. KOYANAGI, H. SUNAMI, N. HASHIMOTO and M. ASHIKAWA, *IEDM Tech. Dig.* **348** (1978).
2. H. SUNAMI, T. KURE, N. HASHIMOTO, K. ITOH, T. TOYABE and S. ASAI, *IEEE Trans. Electron Devices* **31** (1984) 746.
3. K. MINEGISHI, S. NAKAJIMA, K. MIURA, K. HARADA and T. SHIBATA, *IEDM Tech. Dig.* **319** (1983).
4. T. Y. TSENG, *IEDMS* **89** (1996).
5. B. GNADE, ''Science and Technology of Electroceramic Thin Films: NATO ASI Series'', Vol. 284, edited by O. Auciello and R. Waser (Kluwer Academic Publishers, London, 1995) p. 373.
6. P. C. FAZAN, *Integr. Ferroelectr.* **247** (1994).
7. H. SHINRIKI, T. KISU, S. I. KIMURA, Y. NISHIOKA, Y. KAWAMOTO and K. MUKAI, *IEEE Trans. Electron Devices* **37** (1990) 1939.
8. P. Y. LESAICHERRE, S. YAMAMICHI, H. YAMAGUCHI, K. TAKEMURA, H. WATANABE, K. TOKASHIKI, K. SATOH, T. SAKURA, M. YOSHIDA, S. OHNISHI, K. NAKIJIMA, K. SHIBAHARA, Y. MIYASAKA and H. ONO, *IEDM Tech. Dig.* **831** (1994).
9. Y. OHJI, Y. MATSUI, T. ITOGA, M. HIRAYAMA, Y. SUGAWARA, K. TORII, H. MIKI, M. NAKATA, I. ASANO, S. IIJIMA and Y. KAWAMOTO, *ibid.* **111** (1995).
10. T. KAGA, Y. SUDOH, H. GOTO, K. SHOJI, T. KISU, H. YAMASHITA, R. NAGAI, S. IIJIMA, M. OHKURA, F. MURAI, T. TANAKA, Y. GOTO, N. YOKOYAMA, M. HORIGUCHI, M. ISODA, T. NISHIDA and E. TAKEDA, *ibid.* **927** (1994).
11. H. O. PIERSON, ''Handbook of Chemical Vapor Deposition: Principles, Technology and Applications'' (Noyes Publications, Park Ridge, New Jersy, USA, 1992).
12. R. J. CAVA, W. F. PECK Jr. and J. J. KRAJEWSKI, *Nature* **377** (1995) 215.
13. S. W. PARK, Y. K. BAEK, I. Y. LEE, C. O. PARK and H. B. IM, *J. Electron. Mater.* **21** (1992) 635.
14. T. F. CHEN, PhD Thesis, National Chiao Tung University, Hsinchu, Taiwan, (1997).
15. S. KAMIYAMA, T. SAEKI, H. MORI and Y. NUMASAWA, *IEDM Tech. Dig.* **827** (1991).
16. H. K. KANG, K. H. KIM, Y. G. SHIN, I. S. PARK, K. M. KO, C. G. KIM, K. Y. OH, S. E. KIM, C. G. HONG, K. W. KWON, J. Y. YOO, Y. G. KIM, C. G. LEE, W. S. PAICK, D. I. SUH, C. J. PARK, S. I. LEE, S. T. AHN, C. G. HWANG and M. Y. LEE, *Ibid.* (1994) 635.
17. A. C. ADAMS, ''Dielectric and Polysilicon Film Deposition'', in VLSI Technology edited by S. M. Sze, Ch. 3, McGraw-Hill, New York, 1993 p. 93.
18. W. KERN, 1985 *Semicond. Int.* **8** (1985) 122.
19. S. WOLF and R. N. TAUBER, ''Silicon Processing for the VLSI Era'', Vol. 1, (Lattice Pres, CA, USA 1986).
20. W. KERN and G. L. SCHNABLE, *IEEE Trans. Electron Devices* **26** (1979) 647.
21. P. SINGER, *Semicond. Int.* **5** (1984) 72.
22. R. S. ROSLER, *Solid State Technol.* **20** (1977) 63.
23. A. C. ADAMS, *ibid.* **4** (1983) 135.
24. B. GOROWITZ, T. B. GORCZYCA and R. J. SAIA, *ibid.* **4** (1985) 197.
25. J. Y. CHEN and R. HENDERSON, *J. Electrochem. Soc.* **131** (1984) 2147.
26. R. SOLANKI, C. MOORE and G. COLLINS, *Solid State Technol.* **6** (1985) 220.
27. A. FEINGOLD and A. KATZ, *Mater. Sci. Eng.* **R 13** (1994) 56.
28. W. KERN and V. S. BAN, ''Thin Film Processes'', edited by J. L. Vossen and W. Kern, (Academic Press, New York, 1978).
29. P. C. VAN BUSKIRK, S. M. BILODEAU, J. F. ROEDER and P. S. KIRLIN, *Jpn. J. Appl. Phys.* **35** (1996) 2520.
30. J. B. WACHTMAN and R. A. HABER, ''Ceramic Thin Films and Coatings'' (Noyes Publications, New Jersey, USA, 1993) p. 208.
31. T. M. GRAETTINGER, S. H. ROU, M. S. AMEEN, O. AUCIELLO and A. I. KINGON, *Appl. Phys. Lett.* **58** (1991) 1964.
32. A. I. KINGON, O. AUCIELLO, M. S. AMEEN, S. H. ROU and A. R. KRAUSS, *Ibid.* **55** (1989) 301.
33. R. RAMESH, H. GILCHRIST, T. STANDS, V. G. KERAMIDAS, R. HAAKENAASEN and D. K. FORK, *Ibid.* **63** (1993) 3592.
34. R. DAT, J. K. LEE, O. AUCIELLO and A. I. KINGON, *Ibid.* **67** (1995) 572.
35. N. TAGA, H. ODAKA, Y. SHIGESATO, I. YASUI and T. E. HAYNES, *J. Appl. Phys.* **80** (1996) 978.
36. J. M. ALBELLA, I. MONTERO, J. M. MARTINEZDUART and V. PARKHUTIK, *J. Mater. Sci.* **26** (1991) 3422.
37. J. J. RANDALL, W. J. BERNARD and R. R. WILKINSON, *Electrochim. Acta* **10** (1965) 183.
38. I. MONTERO, J. M. ALBELLA, J. M. MARTINEZDUART and L. SORIANO, *J. Mater. Sci.* **22** (1987) 1785.
39. J. J. RANDALL, *Electrochim. Acta.* **20** (1975) 663.
40. C. J. DELL'OCA and L. YOUNG, *J. Electrochem. Soc.* **117** (1970) 1545.
41. A. J. SCHRIJNER and A. MIDDLEHOEK, *Ibid.* **111** (1964) 1167.
42. D. J. SMITH and L. YOUNG, *Thin Solid Films* **101** (1983) 11.
43. C. D. LAKEMAN and D. A. PAYNE, *Mater. Chem. Phys.* **38** (1994) 305.
44. D. L. PULFREY, P. S. WILCOX and L. YOUNG, *J. Appl. Phys.* **40** (1969) 3891.
45. R. L. ANGLE and H. E. TALLEY, *IEEE Trans. Electron Devices* **25** (1978) 1277.
46. G. S. OEHRLEIN and A. REISMAN, *J. Appl. Phys.* **54** (1983) 6502.
47. J. G. HWU and S. T. LIN, *IEEE Proc.* **137** (1990) 390.
48. S. I. KIMURA, Y. NISHIOKA, A. SHINTANI and K. MUKAI, *J. Electrochem. Soc.* **130** (1983) 2414.
49. Y. NISHIOKA, S. I. KIMURA, H. SHINRIKI and K. MUKAI, *Ibid.* **134** (1987) 410.
50. M. SAITOH, T. MORI and T. TAMURA, *IEDM Tech. Dig.* **680** (1986).
51. S. ZAIMA, T. FURUTA and Y. YASUDA, *J. Electrochem. Soc.* **137** (1990) 1297.
52. P. A. MURAWALA, M. SAWAI, T. TATSUTA, O. TSUII, S. FUJITA and S. FUJITA, *Jpn. J. Appl. Phys.* **32** (1993) 368.
53. H. S. MOON, J. S. LEE, S. W. KAN, J. W. PARK, J. H. LEE, S. K. YANG and H. H. PARK, *J. Mater. Sci.* **29** (1994) 1545.
54. S. O. KIM, J. S. BYUN and H. J. KIM, *Thin Solid Films* **206** (1991) 102.
55. J. G. HWU and M. J. JENG, *J. Electrochem. Soc.* **135** (1988) 2808.
56. K. CHEN, M. NIELSEN, G. R. YANG, E. J. RYMASZEWSKI and T. M. LU, *J. Electron. Mater.* **26** (1997) 397.

57. S. SCHILLER, U. HEISIG, K. STEINEFELDER and J. STRUMPFEL, *Thin Solid Films* **63** (1979) 369.
58. T. M. REITH and P. J. FICALORA, *J. Vac. Sci. Technol. A* **1** (1983) 1362.
59. G. V. SAMSONOV, Ed., ''The Oxide Hand Book'' (IFI/Plenum, New York, 1973) p. 316.
60. F. C. CHIU, J. J. WANG, J. Y. LEE and S. C. WU, *J. Appl. Phys.* **81** (1997) 6911.
61. R. A. B. DEVINE, *Appl. Phys. Leti.* **68** (1996) 1924.
62. Y. CHEN, R. SINGH and J. NARAYAN, *J. Electron. Mater.* **26** (1997) 350.
63. R. SINGH, *J. Appl. Phys.* **63** (1988) R59.
64. S. KAMIYAMA, T. SAEKI, H. MORI and Y. NUMASAWA, *IEDM Tech. Dig.* (1991) 827.
65. S. KAMIYAMA, P. Y. LESAICHERRE, A. ISHITANI, A. SAKAI, A. TANIKAWA and I. NISHIYAMA, *Ext. Abst. Int. Solid State Devices and Materials* (1992) 521.
66. P. C. FAZAN, V. K. MATHEWS, R. L. MADDOX, A. DITALI, N. SANDLER and K. L. KWONG, *ibid.* (1992) 697.
67. S. KAMIYAMA, P. Y. LESAICHERRE, H. SUZUKI, A. SAKAI, I. NISHIYAMA and A. ISHITANI, *J. Electrochem. Soc.* **140** (1997) 1617.
68. S. C. SUN and T. F. CHEN, *IEEE Electron Device Lett.* **17** (1996) 355.
69. *Idem.*, *IEDM Tech. Dig.* (1996) 687.
70. W. S. LAU, P. W. QIAN, N. P. SANDLER, K. A. MCKINLEY and P. K. CHU, *Jpn. J. Appl. Phys.* **36** (1997) 661.
71. W. S. LAU, K. K. KHAW, P. W. QIAN, N. P. SANDLER and P. K. CHU, *ibid.* **35** (1996) 2599.
72. C. Y. TING and M. WITTMER, *J. Appl. Phys.* **54** (1983) 937.
73. L. KRUSIN-ELBAUM, M. WITTMER and D. S. YEE, *Appl. Phys. Lett.* **50** (1987) 1879.
74. M. WITTMER, *J. Vac. Sci. Technol. A* **2** (1984) 273.
75. L. KRUSIN-ELBAUM, M. WITTMER, C. Y. TING and I. J. CUOMO, *Thin Solid Films* **104** (1983) 81.
76. R. G. VADIMSKY, R. P. FRANKENTHAL and D. E. THOMPSON, *J. Electrochem. Soc.* **126** (1979) 2017.
77. P. H. HOLLOWAY and C. C. NELSON, *Thin Solid Films* **35** (1976) L13.
78. M. L. GREEN, M. E. GROSS, L. E. PAPA, K. J. SCHNOES and D. BRASEN, *J. Electrochem. Soc.* **132** (1985) 2677.
79. H. MATSUHASHI and S. NISHIKAWA, *Jpn. J. Appl. Phys.* **33** (1994) 1293.
80. I. KIM, J. S. CHUN and W. J. LEE, *Mater. Chem. Phys.* **44** (1996) 288.
81. J. HARVEY and H. WILMAN, *Acta. Crystallogr.* **14** (1961) 1278.
82. D. M. SMYTH, G. A. SHIRN and T. B. TRIPP, *J. Electrochem. Soc.* **130** (1983) 2414.
83. T. AOYAMA, S. SAIDU, Y. OKAYAMA, M. FUJISAKI, K. IMAI and T. ARIKADO, *ibid.* **143** (1996) 977.
84. F. C. CHIU, J. J. WANG, J. Y. LEE and S. C. WU, *J. Appl. Phys.* **81** (1997) 6911.
85. Y. NISHIOKA, N. HOMMA, H. SHINRIKI, K. MUKAI, K. YAMAGUCHI, A. UCHIDA, K. HIGETA and K. OGIUE, *IEEE Trans. Electron Divices* **34** (1987) 1957.
86. S. ROBERTS, J. RYAN and L. NESHIT, *J. Electrochem. Soc.* **133** (1986) 1405.
87. A. G. REVESZ and T. D. KIRKENDALL, *ibid.* **123** (1976) 1514.
88. S. EZHILVALAVAN and T. Y. TSENG, *J. Am. Ceram. Soc.* (1998) (in print).
89. A. S. PAVLOVIC, *J. Chem. Phys.* **40** (1964) 951.
90. A. REISMAN, F. HOLTZBURG, M. BERKENBLIT and M. BERRY, *J. Am. Chem. Soc.* **78** (1956) 4514.
91. H. HU, C. J. PENG and S. B. KRUPANIDHI, *Thin Solid Films* **223** (1993) 327.
92. A. PIGNOLET, G. MOHAN RAO and KRUPANIDHI, *ibid.* **258** (1995) 230.
93. B. W. SHEN, I. C. SHEN, S. BANERJEE, R. A. BROWN, J. BOHLMAN, P. H. CHANG and R. R. DOERING, *IEDM Tech. Dig.* **582** (1987).
94. G. S. OEHRLEIN, F. M. D'HEURLE and A. REISMAN, *J. Appl. Phys.* **55** (1984) 3715.
95. C. ISOBE and M. SAITOH, *Appl. Phys. Lett.* **56** (1990) 907.
96. H. SHINRIKI and M. NAKATA, *IEEE Trans. Electron Divices* **38** (1991) 455.
97. S. G. BYEON and Y. TZENG, *ibid.* **37** (1990) 972.
98. S. W. PARK and H. B. IM, *Thin Solid Films* **207** (1992) 258.
99. H. DEMIRYONT, J. R. SITES and K. GEIB, *Appl. Opt.* **24** (1985) 490.
100. S. C. SUN and T. F. CHEN, *Ext. Abst. Electrochem. Soc., Fall Meeting* (1995) pp. 870.
101. S. KAMIYAMA, H. SUZUKI and H. WATANABE, *J. Electrochem. Soc.* **141** (1994) 1246.
102. Y. MATSUI, K. TORII, M. HIRAYAMA, Y. FUJISAKI, S. IIJIMA and Y. OHJI, *IEEE Electron Device Lett.* **17** (1996) 431.
103. C. M. OSBURN and D. W. ORMOND, *J. Electrochem. Soc.* **109** (1972) 591.
104. K. SAYYAH, ''The Physics and Chemistry of SiO_2 and Si-SiO_2 Interface'' (Plenum Press, New York, 1988) p. 129.
105. S. SEKI, T. UNAGAMI and O. KOGURE, *J. Electrochem. Soc.* **131** (1984) 2457.
106. S. SEKI, T. UNAGAMI, O. KOGURE and B. TSUJIYAMA, *J. Vac. Sci. Technol.* **A5** (1987) 1771.
107. M. MATSUI, S. OKA, K. YAMAGISHI, K. KUROIWA and Y. TARUI, *Jpn. J. Appl. Phys.* **27** (1988) 506.
108. S. TANIMOTO, M. MATSUI, K. KAMISAKO, K. KUROIWA and Y. TARUI, *J. Electrochem. Soc.* **139** (1992) 320.
109. C. HASHIMOTO, H. OIKAWA and N. HONMA, *IEEE Trans. Electron Devices* **36** (1989) 14.
110. S. TANIMOTO, Y. SHICHI, K. KUROIWA and Y. TARUI, *Extended Abstracts of 19th Conference on Solid State Devices and Materials*, (1993) p. 859.
111. S. C. SUN and T. F. CHEN, *IEDM Tech. Dig.* **333** (1994).
112. X. M. WU, S. R. SOSS, E. J. RYMASZEWSKI and T. M. LU, *Mater. Chem. Phys.* **38** (1994) 297.
113. H. TREICHEL, A. MITWALSKY, N. P. SANDLER, D. TRIBULA, W. KERN and A. P. LANE, *Adv. Mater. Opt. Electron* **1** (1992) 299.
114. S. G. BYEON and Y. TZENG, *J. Electrochem. Soc.* **135** (1988) 2452.
115. G. S. OEHRLEIN, *J. Appl. Phys.* **59** (1986) 1587.
116. M. A. MOHAMMED and D. MORGAN, *Thin Solid Films* **176** (1989) 45.
117. J. J. LEE, C. L. THIO and S. B. DESU, *J. Appl. Phys.* **78** (1995) 5073.
118. S. M. SZE, ''Physics of Semiconductor Devices'' (John Wiley & Sons, New York, 2nd Edn 1981) p. 251.
119. G. S. OEHRLEIN, *Thin Solid Films* **156** (1988) 207.
120. A. G. REVESZ and J. F. ALLISON, *IEEE Trans. Electron. Devices* **23** (1976) 527.
121. S. KAMIYAMA, H. SUZUKI and H. WATANABE, A. SAKAI, M. OSHIDA, T. TATSUMI, T. TANIGAWA, N. KASAI and A. ISHITANI, *IEDM Tech. Dig.* **49** (1993).
122. H. SHINRIKI, M. NAKATA, Y. NISHIOKA and K. MUKAI, *IEEE Trans. Electron Device Lett.* **10** (1989) 514.
123. S. C. SUN and T. F. CHEN, *ibid.* **17** (1996) 355.
124. P. J. TOBIN, Y. OKADA, V. LAHKOTIA, S. A. AJURIA, W. A. FEIL and R. I. HEDGE, in *VLSI Tech. Symp.* (1993) p. 51.
125. H. KIMURA, J. MIZUKI, S. KAMIYAMA and H. SUZUKI, *Appl. Phys. Lett.* **66** (1995) 2209.
126. J. G. SIMMONS, *J. Phys. D. Appl. Phys.* **4** (1971) 613.
127. N. SCHWARTZ and M. GRESH, *J. Electrochem. Soc.* **112** (1965) 295.
128. D. A. VERMILYEA, *J. Appl. Phys.* **36** (1965) 3663.
129. N. N. AXELROD and N. SCHWARTZ, *J. Electrochem. Soc.* **116** (1969) 460.
130. J. G. SIMMONS, *Phys. Rev.* **155** (1967) 657.
131. P. MARK and T. E. HARTMAN, *J. Appl. Phys.* **39** (1968) 2163.
132. D. L. PULFREY, A. H. M. SHOUSHA and L. YOUNG, *J. Appl. Phys.* **41** (1970) 2838.
133. C. A. MEAD, *Phys. Rev.* **128** (1962) 2088.
134. G. D. O'CLOCK, Jr., *Appl. Phys. Lett.* **19** (1971) 403.
135. T. W. HICKMOTT, *J. Electrochem. Soc.* **113** (1966) 1223.
136. C. L. STANDLEY and L. I. MAISSEL, *J. Appl. Phys.* **35** (1964) 1530.
137. W. D. WESTWOOD, N. WATERHOUSE and P. S. WILCOX,

''Tantalum Thin Films'' (Academic Press, New York, 1975) p. 333.
138. G. KORINEC, *Electro. Technol* **6** (1968) 108.
139. G. P. KLEIN and N. I. JAEGER, *J. Electrochem. Soc.* **117** (1970) 1483.
140. P. L. YOUNG, *J. Appl. Phys.* **46** (1975) 2794.
141. *Idem.*, *ibid.* **47** (1976) 235.
142. *Idem.*, *ibid.* **47** (1976) 242.
143. J. L. HARTKE, *ibid.* **39** (1968) 4871.
144. E. KAPLAN, M. BALOG and D. FROHMAN-BENTCHKOWSKY, *J. Electrochem. Soc.* **123** (1976) 1570.
145. S. M. SZE, *J. Appl. Phys.* **38** (1967) 2951.
146. M. METIKOS-HUKOVIE and M. CHERAJ-CERIC, *Thin Solid Films* **145** (1986) 39.
147. S. BANERJEE, B. SHEN, I. CHEN, J. BOHLMAN, G. BROWN and R. DOERING, *J. Appl. Phys.* **65** (1989) 1140.
148. J. O'DWYER, ''Theory of Electrical Conduction and Breakdown in Slolid Dielectrics'' (Clarendon, Oxford, UK, 1973).
149. H. SEKI, *Phys. Rev. B* **2** (1970) 4877.
150. S. ZAIMA, T. FURUTA, Y. KOIDE and Y. YASUDA, *J. Electrochem. Soc.* **137** (1990) 2876.
151. S. EZHILVALAVAN and T. Y. TSENG, *J. Appl. Phys.* **83** (1989) 4797.

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