A 2-D Velocity- and Direction-Selective Sensor with BJT-Based Silicon Retina and Temporal Zero-Crossing Detector

Hsin-Chin Jiang and Chung-Yu Wu

***Abstract*—In this paper, a 2-D velocity- and direction-selective visual motion sensor with a bipolar junction transistor (BJT)-based silicon retina and temporal zero-crossing detector is proposed and implemented. In the proposed sensor, a token-based delay-and-correlate computational algorithm is adopted to detect the selected speed and direction of moving object images. Moreover, binary pulsed signals are used as correlative signals to increase the velocity and direction selectivities. Each basic detection cell in the sensor has a compact architecture, which consists of one BJT-based silicon retina cell, one current-input edge extractor, two delay paths, and four correlators. Using the proposed architecture, an experimental 32 $\times$ 32 visual motion sensor chip with a cell size of 100 $\times$ 100 μm^2 has been designed and fabricated by using 0.6-μm CMOS technology. The correct operations of the fabricated sensor chip have been verified through measurements. The measured ranges of selectively detected velocity and direction in the fabricated sensor chip are 56 mm/s–5 m/s and 0–360°, respectively. The complete sensor system consumes 20 mW at 5 V.**

***Index Terms*—Bipolar junction transistor (BJT)-based silicon retina, CMOS motion-selective sensor, current-input edge extractor, direction-selective sensing, temporal zero-crossings, velocity-selective sensing.**

I. Introduction

VELOCITY and direction are two important properties of motion. So far, many visual-motion sensors have been proposed [1]–[14] that incorporate photoreceptors and processing circuits on a single chip to estimate velocity and direction of motion. The adopted motion-sensing algorithms can be divided into two categories: intensity-based algorithms [1], [2] and token-based algorithms [3]–[14]. An intensity-based algorithm, which is based upon the mapping of mathematical techniques, usually requires high-precision temporal and spatial derivatives. Therefore, it is not suitable for an analog hardware implementation. In contrast, a token-based algorithm, which is inspired by biological models, has a higher numerical stability and is suitable for analog hardware implementations. Comprehensive comparisons of these two algorithms and their implementations can be found in [15]–[18].

In this paper, a bipolar junction transistor (BJT)-based silicon-retina sensory system for velocity- and direction-selective sensing is proposed. In this system, a token-based delay-and-correlate motion computation algorithm inspired by biological retinal processing is adopted, which uses edges as image tokens and correlates them with binary pulses. One of the two significant features of the proposed sensory system is that the circuitry of the current-input edge extractor is simple and robust, which makes very-large-scale integration (VLSI) implementation feasible. The other is that the binary pulse correlation [9]–[11] is used to increase the accuracy of velocity- and direction-selective sensing. Using the proposed architecture, an experimental 32 $\times$ 32 motion measurement chip has been fabricated by using a 0.6-μm CMOS technology. The operations are also verified through measurements.

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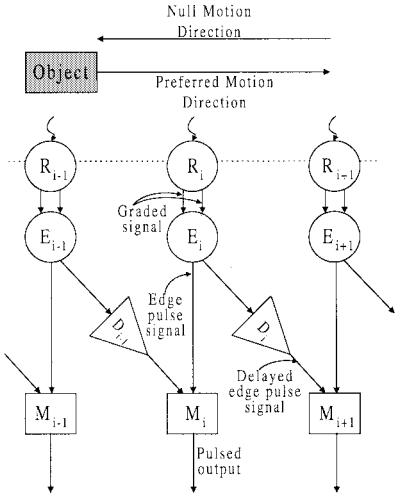
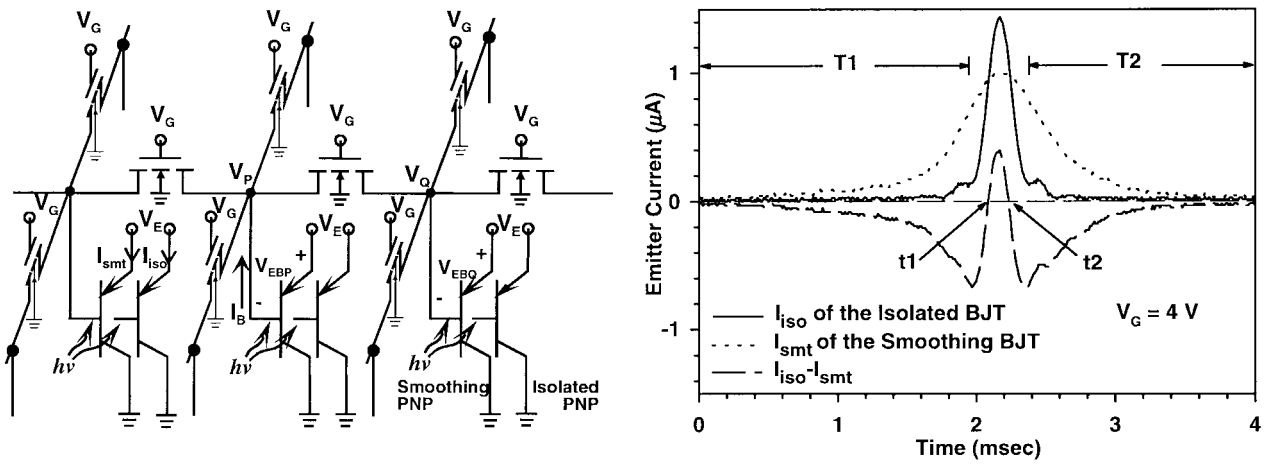


Fig. 1. The adopted token-based delay-and-correlate motion-computation algorithm.

II. Motion-Computation Algorithm

The token-based delay-and-correlate motion computation algorithm, which is similar to the Reichardt algorithm [19], is adopted in the sensor design. The conceptual structure of the algorithm is shown in Fig. 1. The elements R perform the functions of photoreceptors and horizontal cells in the retinas. The photoreceptors transduce light into electrical signals, whereas the horizontal cells perform the spatial smoothing on signals from photoreceptors. The edge extractors E perform the functions of the bipolar cells in the retinas, which process the signals from both the photoreceptor and horizontal cell to generate a signal that contains spatial edge information of the incident image. Meanwhile, the edge extractors E identify both turn-ON and turn-OFF edges of the moving image from the signals generated by bipolar cells. They generate edge pulses to perform a function similar to the action potential responses observed in transient amacrine cells of the retinas.



(a) (b)

Fig. 2. (a) The structure of a BJT-based silicon retina with tunable image-smoothing capability, which is proposed in [20] and [21]. (b) The measured responses of the emitter current difference of a single cell in the BJT-based silicon retina [21] with a moving light bar incident upon the chip.

The elements M are the correlators that correlate the edge pulse from E with the delayed edge pulse generated from the previous cell using the delay elements D. The correlator fires a pulse only when the object moves in the preferred direction and the difference between the traveling time of the object edge crossing the two cells and the selected delay time of the elements D is smaller than the width of the edge pulse. The combination of M and D is used to mimic the direction-sensitive responses of ganglion cells in the retinas.

III. Hardware Implementation

A. The BJT-Based Silicon Retina

Fig. 2(a) shows the structure of a BJT-based silicon retina [20], [21], which is used to realize the function of the elements R in Fig. 1. In this BJT-based silicon retina, each cell has two BJT's, called smoothing BJT and isolated BJT, which are implemented using the parasitic BJT structure in a standard CMOS process. The base region of one smoothing BJT is connected with the base regions of the smoothing BJT's in its four neighbor cells via nMOS field-effect transistors (nMOSFET's) to form a BJT smoothing network, which is used to implement the equivalent function of the horizontal cells in the retina. The isolated BJT is used to realize the photoreceptor in the retina. The outputs are the emitter currents of the BJT's.

The response of the bipolar cell in the retina is realized by subtracting the emitter current of the BJT in the smoothing network from that of the isolated BJT in the same cell. Fig. 2(b) shows the measured responses [21] of a single cell in the BJT-based silicon retina with a moving light bar projected upon it. When the turn-ON edge and the turn-OFF edge of the moving light bar pass over the readout cell at $t1$ and $t2$, respectively, the temporal averaging functions of the BJT smoothing network lead to the temporal zero-crossings in the emitter current difference of the phototransistors. The appearance of temporal zero-crossings can be used to identify whether an edge of a moving object passes over the readout cell.

B. The Edge Extractor

To simultaneously realize the response of the bipolar cell and detect the temporal zero-crossings of the response as the edges of the object image passing over the BJT-based silicon retina cell, an edge extractor is proposed, as shown in Fig. 3(a). In Fig. 3(a), the transistors $M_{\rm lpi}, M_{\rm ini}, M_{\rm ni}$, and $M_{\rm lps}, M_{\rm ins}, M_{\rm ns}$ are used to virtually bias the emitters of isolated BJT $Q_{\rm iso}$ and smoothing BJT $Q_{\rm smt}$ in the BJT-based silicon retina cell at the fixed voltage V_P and readout emitter currents $I_{\rm iso}$ and $I_{\rm smt}$, respectively. This readout scheme, which has a common part as shown on the left, is proposed in [22] as the readout circuit for the infrared detector.

To detect the zero-crossing point without ambiguity, even under noise and disturbance, a current-input Schmitt trigger [23] ($M_s, M_{sr}, M_{ir}, M_i, M_F$, and M_{F1}) is used. The input current $I_{\rm smt}$ is applied to the drain of the M_s, whereas the other input current $I_{\rm iso}$ is applied to the drain of M_i via a cascoded current mirror M_{p1}–M_{p4}. If the current through M_F and M_{F1} is ΔI, the edge signal at the output of the Schmitt trigger has a sudden change from VDD to GND when $I_{\rm iso}$ becomes greater than $\Delta I + I_{\rm smt}$. This corresponds to the temporal zero-crossing point of the turn-ON edge at $t1$ in Fig. 2(b). In this case, the GND level of the edge signal turns off the NMOS M_F, and ΔI is cut off from the drain of M_i. Only if $I_{\rm iso}$ is decreased to a value smaller than $I_{\rm smt}$ will the edge signal at the output of the edge extractor change from GND to VDD. This corresponds to the temporal zero-crossing point of the turn-OFF edge at $t2$.

A temporal transition at the *Edge-Signal* output is further converted into an edge pulse by using the pulse-conversion circuit, also shown in Fig. 3(a). It consists of two inverters used to shape the signal at the *Edge-Signal* node, a simple transient detection circuit used to perform the temporal differentiation, and an inverter used to produce a narrow pulse. The capacitor in the circuit is implemented using the PMOS transistor with its source and drain tied together as one plate and the gate as the other plate of the capacitor. The discharge in the circuit is implemented by an NMOS transistor with an adjustable bias voltage $V_{\rm pulse}$.

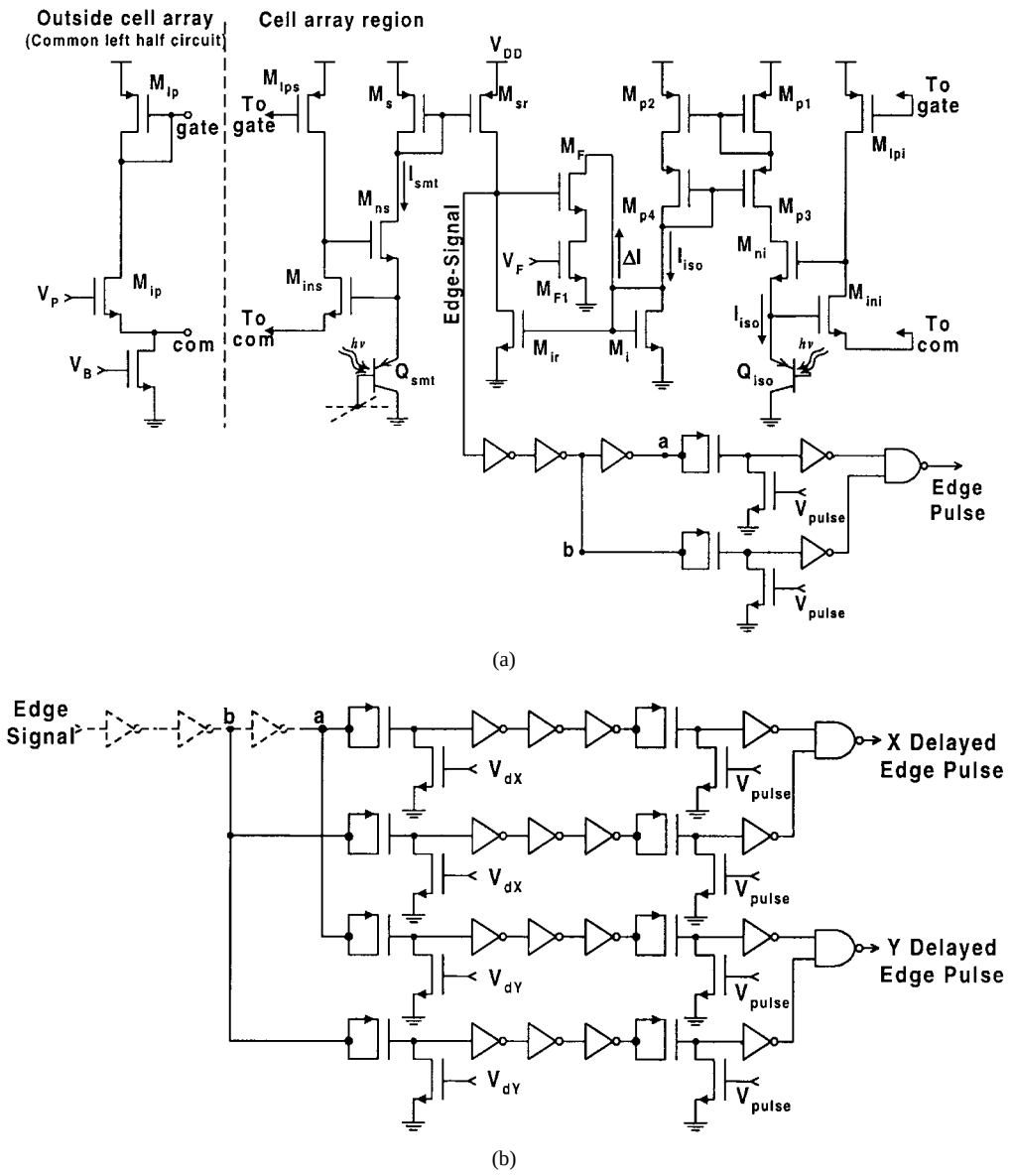


Fig. 3. (a) The edge extractor, which detects the temporal zero-crossings from the edge signals given by the BJT-based silicon retina and generates the edge pulse. (b) The circuit architecture, which is used to realize the element D in Fig. 1 for the generation of delayed edge pulse signals.

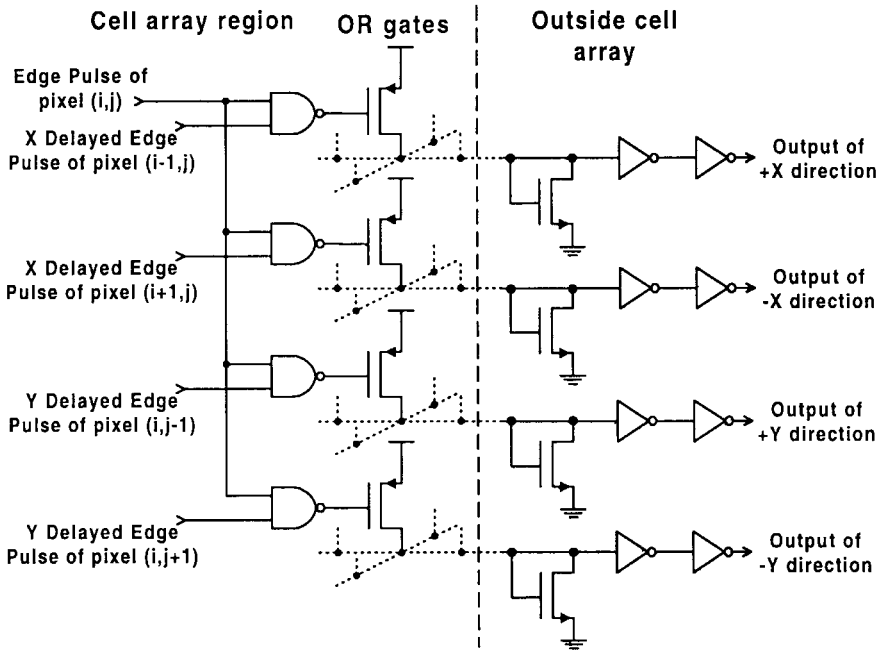
At the falling temporal transition of the input to the transient detector, the negative voltage due to the capacitance coupling makes the drain junction of the nMOSFET forward biased, which inhibits the generation of a large negative voltage pulse. Hence, another set of transient detectors and inverters is used, with an extra inverter at the input to invert the falling temporal transition and generate a positive voltage pulse. Then the outputs of two pulse-conversion circuits are connected to a NAND gate to form a single output. The circuit of Fig. 3(a) realizes the function of the element E in Fig. 1.

C. The Delay Element

Fig. 3(b) shows the circuit architecture used to realize the element D in Fig. 1 for the generation of delayed edge pulse. There are four signal paths in this circuit architecture. The first two paths are used to generate delayed binary narrow pulses at the temporal transitions of signals from the edge extractor along the X direction, whereas the last two paths are used to generate those along the Y direction. In each signal path, there are two transient detectors with the adjustable voltages $V_{\rm dX}, V_{\rm dY}$, and $V_{\rm pulse}$. The first one with $V_{\rm dX}$ $(V_{\rm dY})$ is used to generate specified delay time whereas the second one with $V_{\rm pulse}$ to generate narrow pulses.

D. The Correlator

Since the signals to be correlated are binary pulses, the correlators can easily, compactly, and robustly be implemented by simple NAND gates, as shown in Fig. 3(c). Motion is selectively detected by correlating the edge pulse at a pixel with the delayed edge pulse from a neighboring pixel. Only the preferred moving direction and velocity can enable the correlator to fire a pulse out. Four such correlators are used in each pixel to correlate the edge pulse with the delayed edge pulse from which four neighbors in four directions $\pm X$ and



(c)

Fig. 3. *(Continued.)* (c) The circuit architecture of the correlators.

$\pm Y$ to extract two-dimensional (2-D) velocity and direction. In this work, the outputs of all the correlators in the pixels along each direction are combined into one output terminal via a simple wired OR gate. Therefore, when the object moves with preferred velocity and direction, there are serial pulses to appear at the output terminal.

The detection of a particular velocity and direction can be realized by controlling the delay times of the delay paths along the X-axis and Y-axis with the tuning voltages $V_{\rm dX}$ and $V_{\rm dY}$. For example, if the selected direction of object motion is θ and the velocity is v, the selected delay times $t_{\rm dx}$ and $t_{\rm dy}$ along the X-axis and Y-axis, respectively, can be written as

$$t_{\rm dx} = d/|v\cos\theta| \tag{1}$$

$$t_{\rm dy} = d/|v\sin\theta| \tag{2}$$

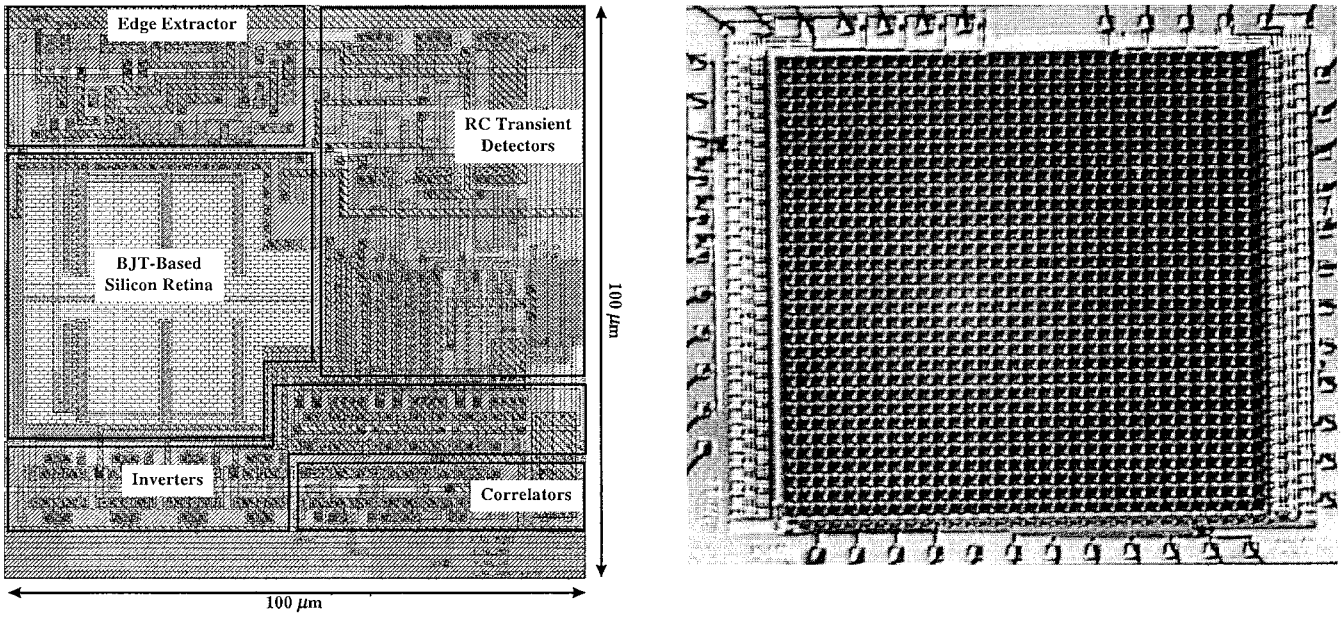
where d is the space between two adjacent BJT-based silicon retina cells. If $0^\circ \le \theta < 90^\circ$ $(90^\circ \le \theta < 180^\circ)$, the outputs $+X\,(-X)$ and $+Y$ in Fig. 3(c) have pulse outputs. If $180^\circ \le \theta < 270^\circ$ $(270^\circ \le \theta < 360^\circ)$, $-X$ $(+X)$ and $-Y$ have pulse outputs.

IV. Measurement Results

An experimental chip was designed and fabricated in a 0.6-μm N-well CMOS technology, which consists of a 32 $\times$ 32 array of the proposed motion-detection cells. Fig. 4(a) shows the layout diagram of the basic cell, whereas Fig. 4(b) shows the photography of the whole chip. Since both image-acquisition elements and computation elements are integrated into one pixel, the wiring will not increase as the size of array increases. Thus, if the die size can be freely increased, the size of array can be freely increased as well.

Fig. 5 shows the measured waveforms in the various computational stages of one motion-detection cell in the fabricated 2-D sensor array. The top traces show the measured emitter currents of isolated BJT and smoothing BJT in the fabricated BJT-based silicon retina cell, where the currents are measured by linearly converting them into voltages via the external circuits. The third trace shows the response at the *Edge-Signal* node in the current-input edge extractor shown in Fig. 3(a). As predicted, the response has sharp transitions when $I_{\rm iso}$ is greater than $I_{\rm smt} + \Delta I$ or $I_{\rm iso}$ is smaller than $I_{\rm smt}$. The fourth trace shows the edge-pulse response of the current-input edge extractor shown in Fig. 3(a). The last two traces show the X and Y delayed edge pulses from the delay element shown in Fig. 3(b). In Fig. 5, the delay time of the first X delayed edge pulse and that of the second X delayed edge pulse are respectively generated via the first two delay paths shown in Fig. 3(b). The component mismatches between these two delay paths induce the mismatch between these two delay times even under the same $V_{\rm dx}$. Fig. 6 shows the measured output waveforms at the four output terminals of the fabricated chip when a bright spot moves in the 45° direction with the preferred speed 1 m/s, where only the outputs $+X$ and $+Y$ have serial pulses as expected.

The interpixel variance of the delay times is one of the important factors that determine the selectivity of the sensor chip. Generally, the interpixel variance of the pulse width and the delay time caused by process variations has a Gaussian distribution with mean value and standard deviation. Through the adjustment of $V_{\rm dX}$ $(V_{\rm dY})$ and $V_{\rm pulse}$, the mean value of the delay time can be set to the desired delay time, whereas the mean value of the pulse width is equal to the standard deviation of the delay time. Then one can obtain around 61% of the overall output pulses with some pulses missing. In this case, the velocity and the direction of the moving objects still can be detected with good selectivity. However, the minimum



(a) (b)

Fig. 4. (a) The layout diagram of the basic detection cell and (b) the photography of the 32 × 32 2-D velocity- and direction-selective sensing chip, which is fabricated by using 0.6-μm N-well CMOS technology.

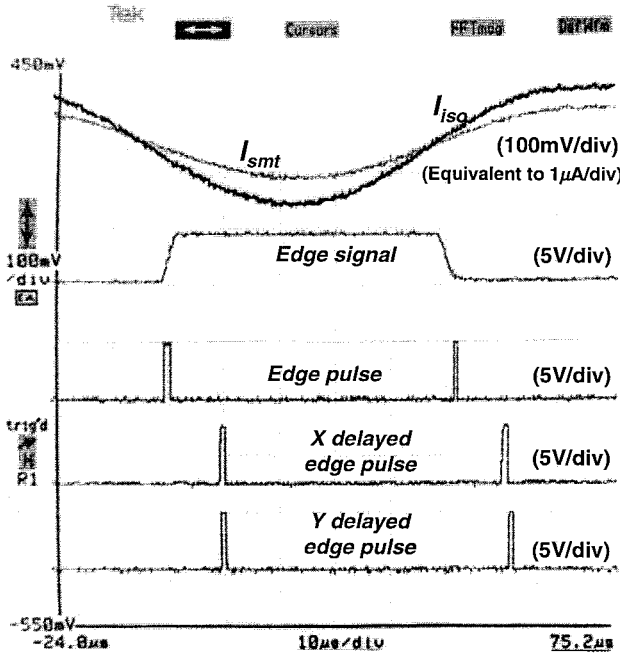


Fig. 5. The oscilloscope traces of the various computational stages of one motion-detection cell in the 2-D array. The emitter currents of the BJT's are read out by using off-array op-amp circuits with negative-feedback resistors to linearly convert them into voltages. The bias voltages are $V_G = 3$ V, $V_B = 1.2$ V, $V_P = 2$ V, $V_F = 0$ V, $V_{\rm pulse} = 0.9$ V, and $V_{\rm dX} = V_{\rm dY} = 0.7$ V.

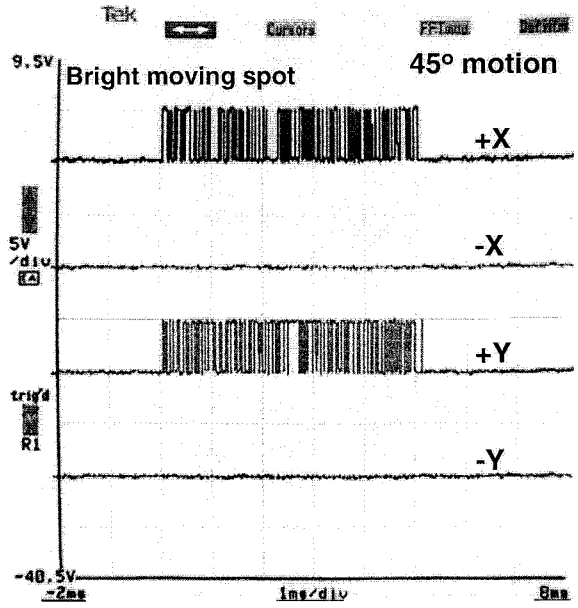


Fig. 6. The measured output waveforms at the four output terminals of the fabricated sensor chip when a bright spot moves in the 45° direction with the preferred speed. The bias voltages are $V_G = 3$ V, $V_B = 1.2$ V, $V_P = 2$ V, $V_F = 0.3$ V, pulse width = 10μs, and delay time = 71μs.

pulse width has a lower limit equal to the standard deviation of the delay time. Fig. 7 shows the measured maximum variance of the delay time of one pixel among eight fabricated chips where the variance percentage is around 16%. The variance is dependent on the mean value of the delay time. Using half of the delay-time variances as the pulse widths to detect the preferred speeds, respectively, the measured selectivity tolerance is around 8% for all preferred speeds with some output pulses missing.

To verify the direction-selective function, a bright spot moving in different directions with the same speed is projected on the chip, and the interpulse delay time of the serial pulses at the four output terminals is measured. The required delay times along the X-axis and Y-axis for the preferred direction are set according to (1) and (2), which are equal to the interpulse delay times of the same direction. Fig. 8 shows the measured interpulse delay times where the negative delay times represent

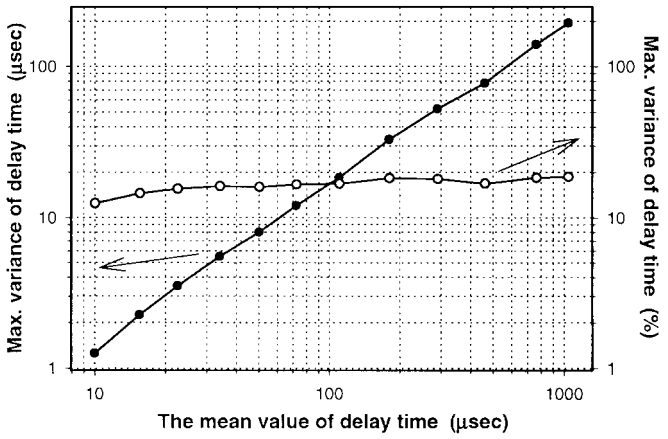


Fig. 7. The measured maximum variance of the delay time of one pixel among eight fabricated chips.

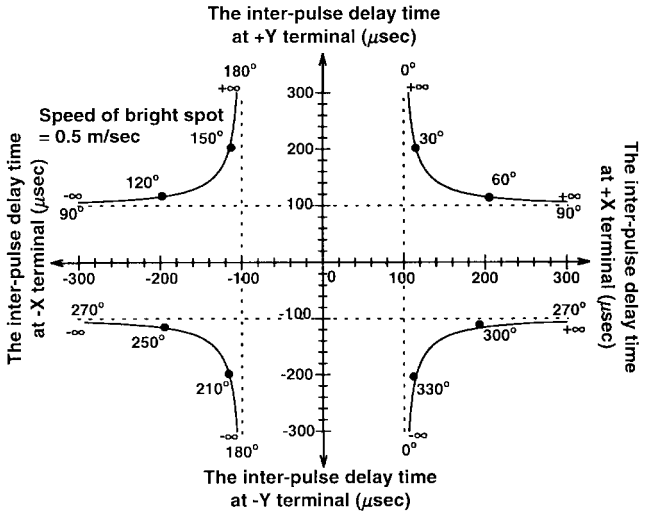


Fig. 8. The measurement of the direction-selective function of the fabricated sensor chip where the interpulse delay time at the four terminals is measured and plotted for different directional angles. The bias voltages in the measurement are $V_G = 3$ V, $V_B = 1.2$ V, $V_P = 2$ V, $V_F = 0.3$ V, and pulse width $= 25\mu$s.

those along the $-X$ or $-Y$ direction. As may be seen from Fig. 8, the motion directions with any angles from 0 to 360° at a fixed speed of 0.5 m/s can be detected by specifying the suitable delay times from 100 to 300 μs in the four directions via the tuning voltages V_{dX} and V_{dY}. If the specified delay time is infinity, the tuning voltage is set to zero to turn off the nMOSFET.

Table I shows the summary on the characteristics of the fabricated motion-selective detection chip. From the measurement results, the correct operations of the proposed visual motion-detection system, which is realized in CMOS technology, have been successfully verified.

V. Conclusion

A 2-D velocity- and direction-selective visual motion sensor with a BJT-based silicon-retina and temporal zero-crossing detector has been proposed, analyzed, and experimentally verified. In this sensor, a token-based delay-and-correlated computational algorithm is adopted, and the motion-selective detection is achieved by correlating two binary edge pulses. Both image-acquisition elements and computation elements are integrated into one cell, and complicated intercell wiring is avoided. Moreover, the robust edge detection in the basic detection cell of the sensor is achieved using the compact structure of the BJT-based silicon retina with the current-input edge extractor, which identifies the temporal zero-crossing points. The operations of the proposed motion sensor have been verified by the measurements on a 32 × 32 CMOS experimental chip. It has been shown that the proposed hardware architecture of the visual motion sensor provides an efficient solution for implementing a dense and robust 2-D visual chip with little power consumption and real-time processing capability.

TABLE I
Summary of the Characteristics for the Fabricated Motion-Selective Detection Chip

Technology	0.6 μm N-well CMOS
Resolution	32 × 32
Chip size	3.6mm × 3.6mm
Cell size	100μm × 100μm
Fill factor	20 %
Space between two adjacent silicon retina cells	50 μm
Power supply	5 V
The measured power dissipation	20 mW
The measured capacitance of PMOS in the transient detector (W/L=6μm/6μm)	0.072 pF
The measured range of selectively detected speed (on-chip speed)	56 mm/sec ~ 5 m/sec (Pulse width: 195 μsec ~ 1.2 μsec)
The measured range of selectively detected direction (On-chip direction)	0° ~ 360°

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