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Barrier Capabilities of Selective Chemical Vapor Deposited W Films and WSiN/WSi$_x$/W Stacked Layers Against Cu Diffusion

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This work investigates the barrier capability of W layers as well as WSiN/WSi$_x$/W stacked layers against Cu diffusion. The W layers were selectively chemical vapor deposited (CVD) in contact holes to a thickness of about 450 nm using SiH_4 reduction of WF_6. We found that the CVD-W layers functioned as effective barriers against Cu diffusion, and the Cu/W(450 nm)/p$^+$-n junction diodes were able to sustain a 30 min furnace annealing up to 650°C without causing degradation in electrical characteristics. The use of WSiN/WSi$_x$/W stacked layers as diffusion layers further improved the thermal stability of Cu/WSiN/WSi$_x$/W(450 nm)/p$^+$-n junction diodes to at least 700°C. The WSi$_x$ layers were deposited by CVD to a thickness of 75 nm using SiH_4/WF_6 chemistry, and the subsequent in situ N_2 plasma treatment produced a very thin layer of WSiN on the WSi$_x$ surface. This thin WSiN layer was very thermally stable and effective in suppressing Cu diffusion. Failure of barrier capability for the W films was presumably due to interdiffusion of Cu and Si along grain boundaries of the W films, and the interdiffusion was probably enhanced by the formation of WSi_2. The formation of WSi_2 consumed the W layer and Si substrate, resulting in a volume change in barrier layer, which, in turn, developed local defects, such as microcracks and stress-induced weak points, and thus provided fast paths for Cu diffusion.
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As device dimensions in integrated circuits are continuously reduced, the requirements imposed on advanced metallization become increasingly stringent. These include reducing electrical resistivity, improving electromigration resistance, and avoiding interdiffusion between metal and Si substrate. Copper (Cu) has a very low resistivity and excellent electromigration resistance,[1,2] and can be deposited conformably using electroplating as well as chemical vapor deposition (CVD) methods.[3–5] Therefore, Cu has been regarded as a potential substitute to replace the widely used Al and Al-alloys for advanced metallization. Unfortunately, Cu diffuses fast in Si and forms Cu–Si compounds at temperatures as low as 200°C.[6,7] In addition, Cu has poor adhesion to interlevel dielectrics and drifts through oxide under field acceleration.[8–10] Therefore, the use of diffusion barriers between Cu and its underlying layers becomes essential to the successful application of Cu in silicon integrated circuits.

Sputter-deposited refractory metals (such as W, Ta, Mo, and Cr) and their nitrides have become more and more attractive in microelectronic applications as diffusion barrier materials because of their high thermal stability, good electrical conductivity, and excellent capability of suppressing reactions between Cu and Si substrate.[11–25] However, it is difficult to deposit barrier layers with excellent barrier properties in contact holes of submicron dimensions using the sputtering technique because of potential step coverage problems. In this respect, selective CVD of tungsten (selective CVD-W) is one of the most attractive techniques for filling deep submicron contact holes in ultralarge-scale integrated (ULSI) interconnect applications.[26,27] The selective nature of the selective CVD-W produces a self-aligned structure and provides a more planar surface for the subsequent metallization process. Thus, it offers a number of potential advantages, including process simplification and possible cost saving.[27]

It was reported that a 73 nm thick selective CVD-W film acted as an effective diffusion barrier between Al and Si substrate at 450°C for 30 min.[28] It was also reported that no discernible reaction took place at the Al/W interface at temperatures up to 500°C for W films deposited by CVD; however, a reaction occurred at the Al/W interface at 450°C for sputtered W and a WAl_{12} compound was formed.[4] In a previous study, we found that a selective CVD-W film of 450 nm thickness was able to retain its barrier capability between Al and Si substrate at 575°C for 30 min, and the barrier capability was effectively improved to 625°C by an in situ N_2 plasma treatment on the surface of the selective CVD-W film.[30] Although these studies have provided much valuable information of selective CVD-W films as a barrier between Al and Si substrate, little study has been made on the barrier capability of selective CVD-W films against Cu diffusion. In one other previous study, we also found that a very thin WSiN layer can be formed on the surface of chemical vapor deposited WSi$_x$ (CVD-WSi$_x$) layer using an in situ N_2 plasma treatment, and the resultant WSiN/WSi$_x$ bilayer was found to possess a much better barrier capability against Cu diffusion than the WSi$_x$ layer itself.[31] Thus, the use of WSiN layers as a Cu barrier is of great interest.

In this study, the barrier capability of selective CVD-W films as well as WSiN/WSi$_x$/W stacked layers used as a diffusion barrier between the Cu and Si substrate was investigated. The CVD-W films were selectively deposited to a thickness of about 450 nm using the SiH_4WF_6 reactant gases, while the WSiN/WSi$_x$/W stacked layers were formed by depositing a thin layer of WSi$_x$ on the CVD-W films by CVD, followed by an in situ N_2 plasma treatment to form a surface layer of WSiN. We found that the WSiN/WSi$_x$/W stacked layer possesses a barrier capability far superior to the single layer of CVD-W film.

Experimental

The barrier properties of selective CVD-W films and WSiN/WSi$_x$/W stacked layers were investigated using a structure of Cu/W/p$^+$-n as well as Cu/WSiN/WSi$_x$/W/p$^+$-n junction diodes. The starting material was (100)-oriented, n-type silicon wafers with 4–7 Ω cm nominal resistivity. After RCA standard cleaning, the wafers were thermally oxidized to grow a 500 nm thick oxide layer. Diffusion areas with sizes of 500 × 500 and 1000 × 1000 μm were defined on the oxide-covered wafers using conventional photolithography. The p$^+$-n junctions with junction depth of 0.3 μm were formed by BF_2^+ implantation at 40 keV to a dose of 3×10^{15} cm^{-2} followed by furnace annealing at 900°C for 30 min in N_2 ambient. After the formation of junctions, the wafers were divided into four groups for the preparation of the following devices: Cu/p$^+$-n, W(450 nm)/p$^+$-n, Cu/W(450 nm)/p$^+$-n, and Cu/WSiN/WSi$_x$(75 nm)/W(450 nm)/p$^+$-n junction diodes. The schematic cross sections of these differently metallized p$^+$-n junction diodes are illustrated in Fig. 1. For the latter three structures of diodes, the contact holes were selectively filled with CVD-W to a thickness of about 450 nm; that is, the 500 nm deep contact holes were nearly filled. This technique offers the advantage of fully self-aligned contacts and barrier formation and also provides a more planar surface for the subsequent metallization process.

Prior to the selective CVD-W deposition, the wafers were dipped in dilute HF (50:1) solution for 30 s followed by a rinse in deionized water for 5 min. The wafers were then loaded into a load-locked coldwall multichamber CVD system (ERA-1000S) within 5 min and transferred by a robot arm to the deposition chamber without exposure to the atmosphere. The ERA-1000S is a fully automatic single-

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wafer CVD system equipped with a cluster of multichambers, including a load/unload, buffer, and two deposition chambers. The system employs a robot unit in the buffer chamber for wafer transfer in vacuum. The reactor, made of aluminum alloy, was water-cooled and was kept at a high vacuum base pressure of 10^{-6} Torr by a turbopump. In this work, the CVD-W films were selectively deposited using SiH_4 reduction of WF_6 chemistry at a condition illustrated as follows: substrate temperature 300°C, total gas pressure 100 mTorr, WF_6 flow rate 40 sccm, SiH_4 flow rate 10 sccm, and H_2 carrier gas flow rate 1000 sccm; the deposition rate was about 5 nm/s.

For the preparation of Cu/WSiN/WSi_x/W(450 nm)/p^+-n junction diodes, the samples deposited with selective CVD-W were transferred to the second deposition chamber, without breaking the vacuum, for further deposition of blanket WSi_x layers to a thickness of about 75 nm. The WSi_x was deposited at the following condition: substrate temperature 250°C, total gas pressure 12 mTorr, WF_6 flow rate 2 sccm, and SiH_4 flow rate 6 sccm; the deposition rate was about 2.5 nm/s. After the CVD-WSi_x deposition, an in situ N_2 plasma treatment was performed on the WSi_x surface for 300 s. The N_2 plasma treatment was performed at 200 W plasma power with N_2 flow rate of 80 sccm and a gas pressure of 25 mTorr. According to this scheme, a very thin WSiN layer was formed on the surface of the WSi_x layer (shown later in Fig. 6). Figure 2 shows the process flow for the Cu/WSiN/WSi_x(75 nm)/W(450 nm)/p^+-n junction diodes.

Finally, Cu metallization was applied to all samples except that the group of W(450 nm)/p^+-n junction diodes were left as they were without a Cu overlayer for comparison. A 300 nm thick Cu film was sputter deposited in Ar ambient at a pressure of 7.6 mTorr using a dc magnetron sputtering system with a base pressure of 1–2 × 10^{-6} Torr and with no intentional substrate heating and bias. After the deposition of Cu films, patterns were defined and Cu was etched using dilute (5 vol %) HNO_3, while the WSiN/WSi_x layer was etched using SF_6/N_2 plasma. To investigate thermal stability of the diodes, samples were thermally annealed in an N_2 flowing furnace for 30 min at a temperature ranging from 200 to 800°C. Reverse bias leakage current measurement on the thermally annealed diodes was used to evaluate the barrier capability of various barrier layers. An HP-4145B semiconductor parameter analyzer was used for the measurement, and at least 30 diodes were measured in each case. Unpatterned samples of Cu(300 nm)/Si, W(450 nm)/Si, Cu/W(450 nm)/Si, and Cu/WSiN/WSi_x(75 nm)/W(450 nm)/Si multilayer structures were also prepared for material analyses. Sheet resistance of the multilayer structures was measured using a four-point probe. Auger electron spectroscopy (AES) was used to determine the composition of WSi_x films. X-ray diffraction (XRD) analysis was used for phase identification, and scanning electron microscopy (SEM) was employed to observe the surface morphology as well as the change of microstructure.

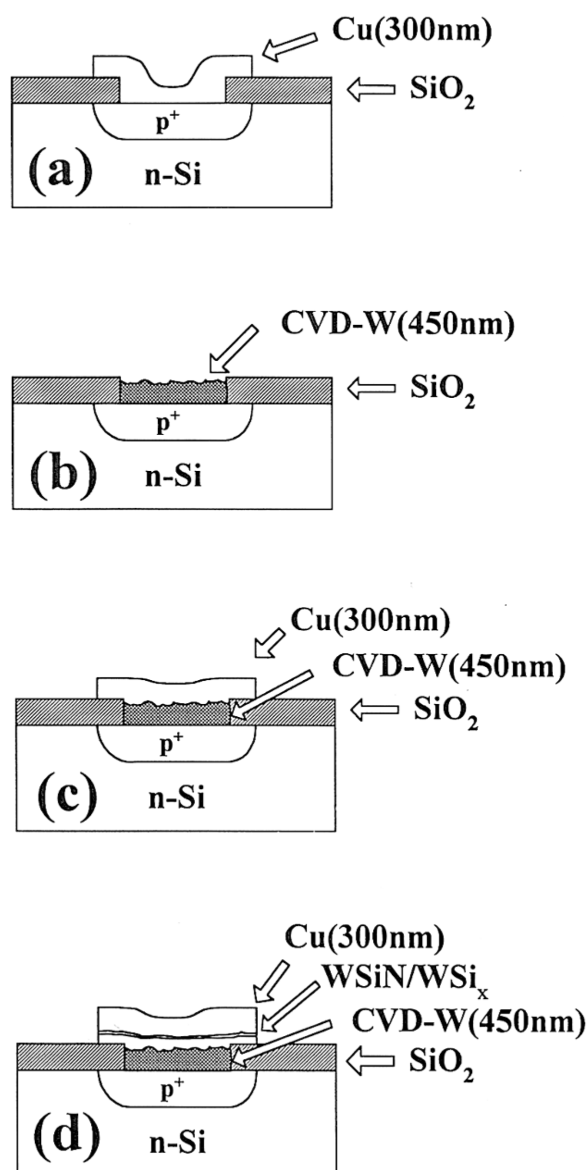

Figure 1. Schematic cross sections of (a) Cu/p^+-n, (b) W(450 nm)/p^+-n, (c) Cu/W(450 nm)/p^+-n, and (d) Cu/WSiN/WSi_x/W(450 nm)/p^+-n junction diodes.

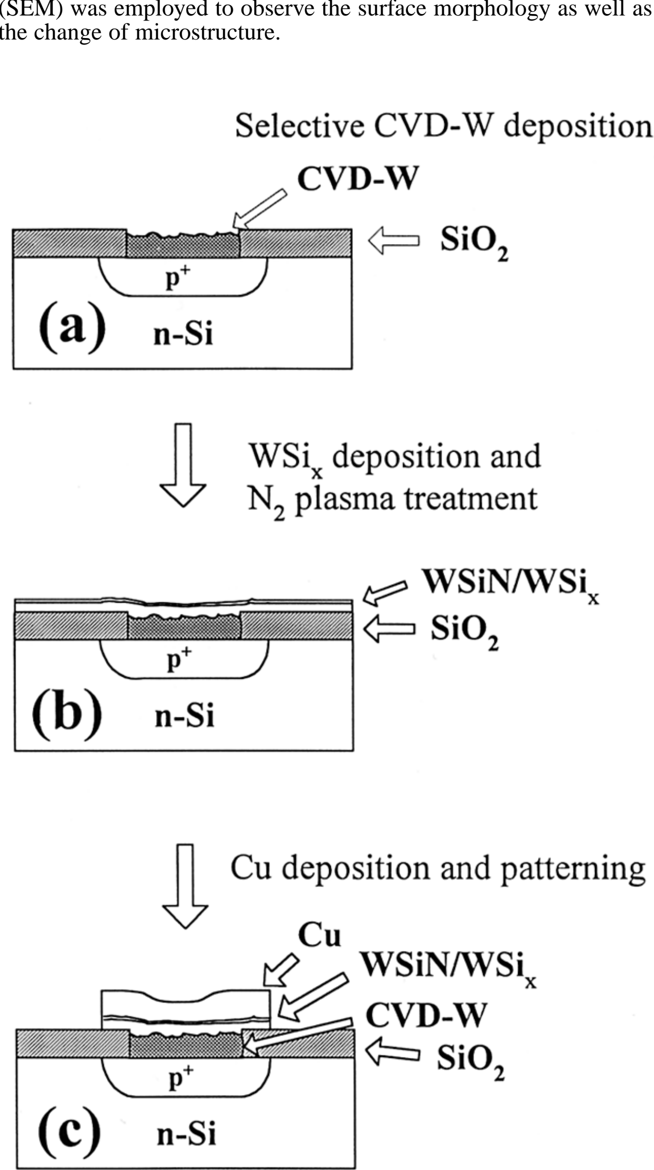

Figure 2. Process flow of Cu/WSiN/WSi_x(75 nm)/W(450 nm)/p^+-n junction diodes: (a) selective CVD-W (450 nm) deposition, (b) blanket WSi_x(75 nm) deposition and in situ N_2 plasma treatment, and (c) Cu deposition patterning.

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Results and Discussion

Deposition of Selective CVD-W films and blanket CVD-WSi_x films.—Figure 3 shows the half-filled and overfilled contact holes of 0.5 μm size using the selective CVD-W technique. Excellent selectivity and uniformity of W film deposition was obtained using the SiH_4/WF_6 chemistry with SiH_4/WF_6 flow rates of 10/40 sccm. Increasing the SiH_4/WF_6 flow rates to 20/40 sccm increased the deposition rate of W but degraded selectivity. Thus, the SiH_4/WF_6 flow rates of 10/40 sccm were used to deposit CVD-W films for the barrier study in this work. Reducing the SiH_4/WF_6 flow rates to 6/2 sccm, we obtained blanket CVD-WSi_x film deposition with complete loss of selectivity. Figure 4 shows the WSi_x films deposited on submicron trenches with an aspect ratio of 4, revealing a highly conformal deposition of CVD-WSi_x.[32]

N_2 plasma treatment.—Figure 5 shows the results of AES depth profiles analysis for the WSi_x films with and without N_2 plasma treatment. Without the N_2 plasma treatment, only a minimal amount of nitrogen was detected near the WSi_x surface (Fig. 5a), presumably due to adsorption of nitrogen gas on the WSi_x surface prior to loading the test sample into the AES chamber. After an in situ N_2 plasma treatment at 200 W for 300 s, a very thin (about 8 nm) WSiN layer was definitely formed (Fig. 5b).

Barrier capability of selective CVD-W films and WSiN/WSi_x/W stacked layers.—*Electrical measurements*.—Barrier capabilities of selective CVD-W(450 nm) films and WSiN/WSi_x(75 nm)/W(450 nm) stacked layers against Cu diffusion were investigated by evaluating the thermal stability of Cu/W(450 nm)/p^+-n and

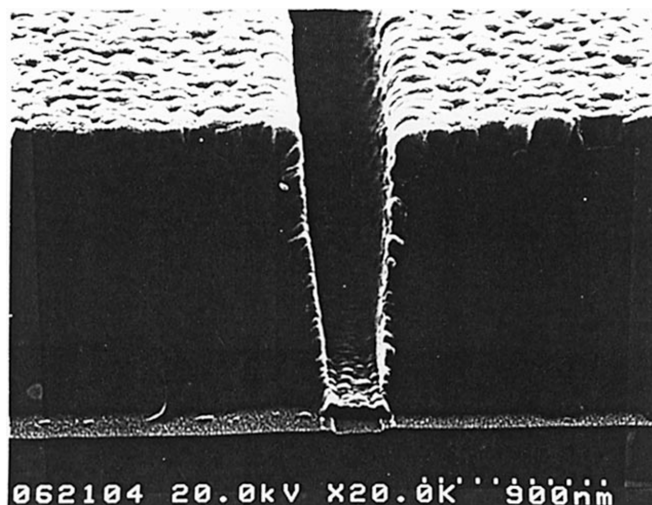
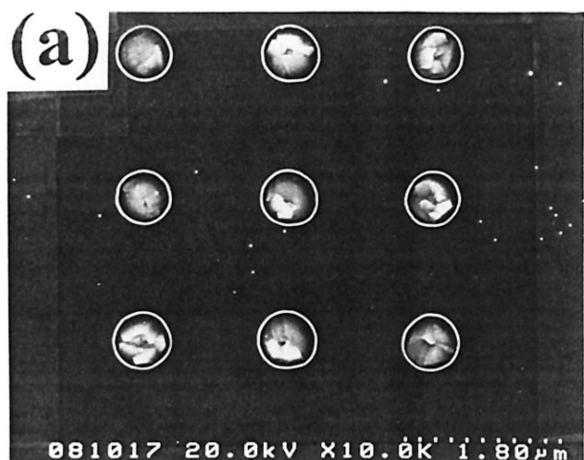


Figure 4. SEM micrographs showing the step coverage of WSi_x films deposited on submicron trenches with an aspect ratio of 4.

Cu/WSiN/ WSi_x(75 nm)/W(450 nm)/p^+-n junction diodes using electrical measurements. Figure 6 illustrates the distributions of reverse bias leakage current density measured at −5 V for the Cu/p^+-n, Cu/W(450 nm)/p^+-n, Cu/WSiN/WSi_x(75 nm)/W(450 nm)/p^+-n and W(450 nm)/p^+-n junction diodes annealed at various tem-



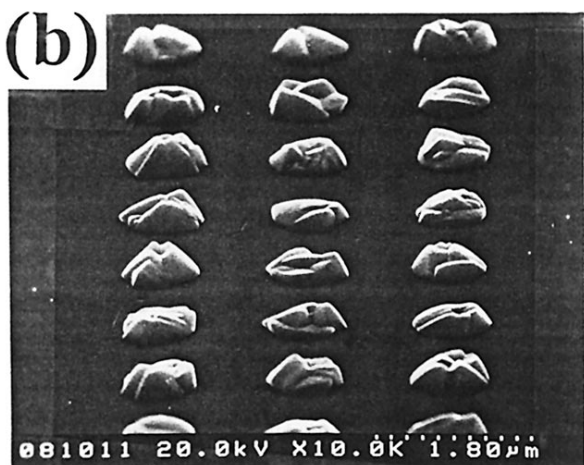
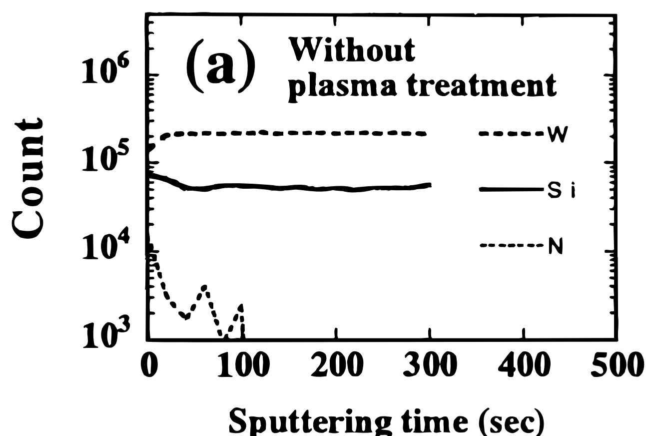


Figure 3. SEM micrographs showing (a) half-filled and (b) overfilled contact holes of 0.5 μm size using the selective CVD-W technique.



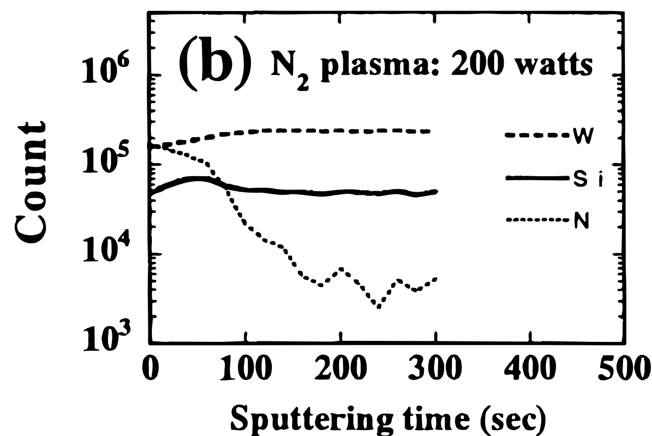


Figure 5. AES depth profiles of as-deposited WSi_x/Si samples (a) without N_2 plasma treatment and (b) with N_2 plasma treatment at 200 W for 300 s.

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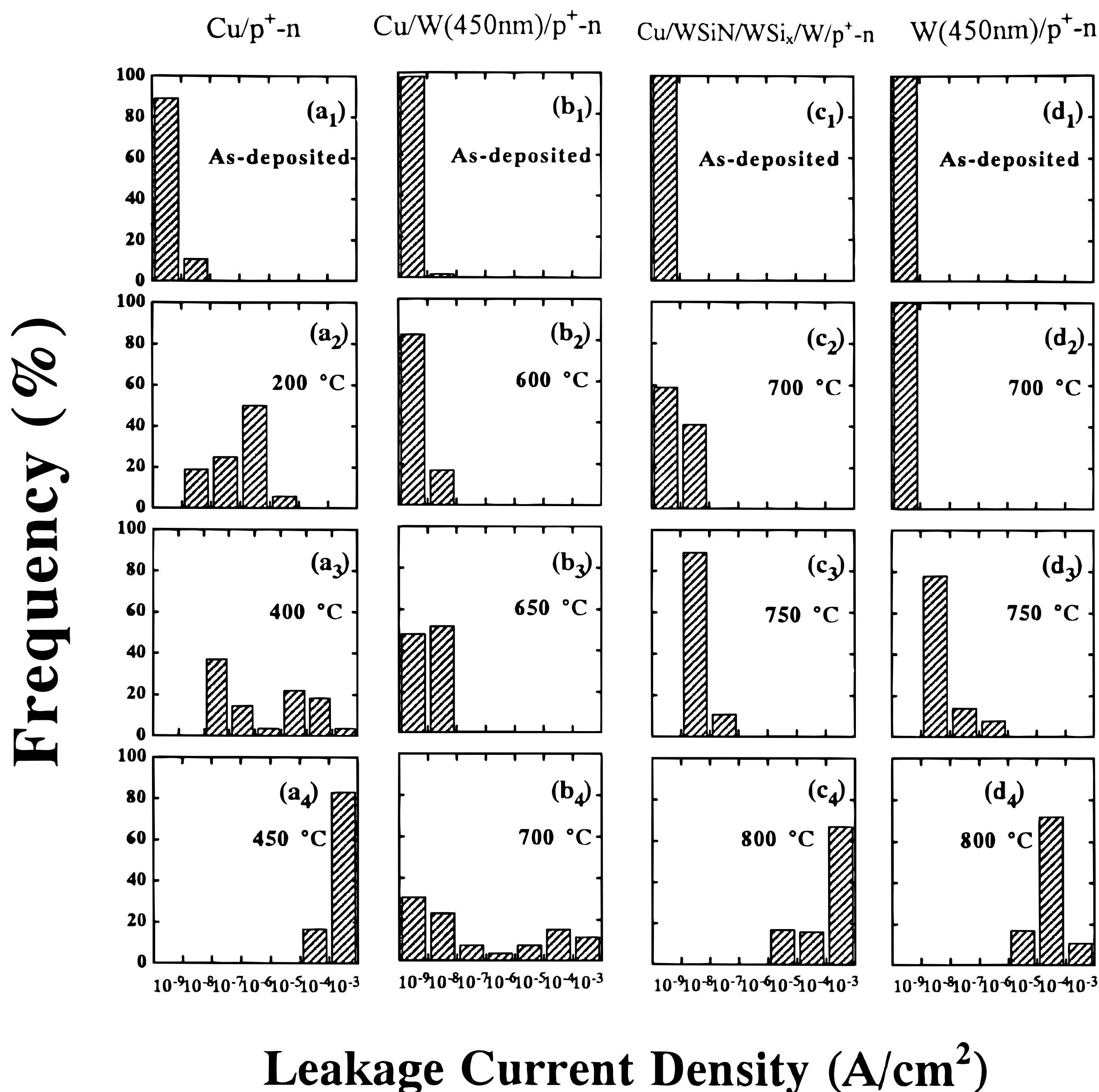

Figure 6. Statistical distributions of reverse bias leakage current density for (a) Cu/p^+-n, (b) Cu/W(450 nm)/p^+-n, (c) Cu/WSiN/WSi_x/W(450 nm)/p^+-n, and (d) W(450 nm)/p^+-n junction diodes annealed at various temperatures.

peratures. For the diodes without any barrier layer between Cu and Si substrate, the Cu/p^+-n junction diodes failed about 200°C annealing (Fig. 6a). With a self-aligned selective CVD-W layer of 450 nm thickness between Cu and Si substrate, the Cu/W/p^+-n junction diodes were able to retain device integrity up to 650°C (Fig. 6b). Nevertheless, about a half number of diodes degraded after annealing at 700°C, and all diodes were degraded upon annealing at 750°C.

For the junction diodes with a WSiN/WSi_x/W stacked layer between Cu and Si substrate, the Cu/WSiN/WSi_x/W/p^+-n diodes remained stable after annealing at 700°C. Even after annealing at 750°C, about 80% of the annealed diodes retained their leakage current density less than 100 nA/cm^2. This suggests that the barrier capability of the CVD-W layer can be significantly improved by adding an N_2-plasma-treated WSiN/WSi_x bilayer on its surface. It was reported that the amorphous structure of reactive-sputter-deposited WSiN layers can be preserved even after annealing at 850°C.[33] It was also reported that a very thin (4 nm) WSiN layer can be formed on the WSi_x surface by ECR N_2 plasma nitridation and that it functioned as an excellent barrier to dopant diffusion.[34] In this work, the very thin and thermally very stable WSiN layers gave a great help to suppress the Cu diffusion. Thus, the barrier capability of CVD-W layers was improved.

For comparison, the thermal stability of W(450 nm)/p^+-n junction diodes without a Cu overlayer were also measured. The W(450 nm)/p^+-n junction diodes retained the integrity of electrical characteristics up to 700°C and revealed only slight degradation after annealing at 750°C; however, severe degradation in electrical characteristics was found after annealing at 800°C (Fig. 6d). The degradation of W(450 nm)/p^+-n junction diodes at 750°C and above was presumably due to a large amount of WSi_2 formation, as confirmed

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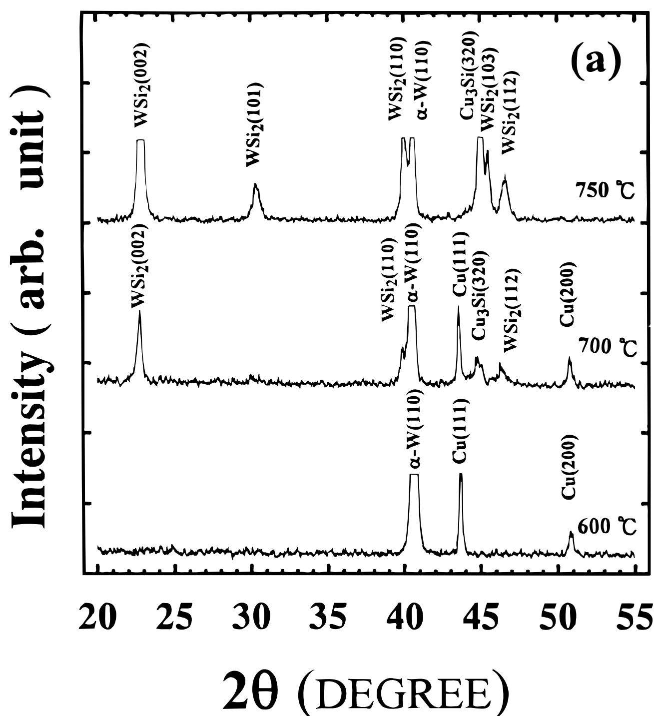
by XRD analysis (to be shown later in Fig. 7). Since each angstrom of tungsten consumed about 2.53 Å silicon for the formation of 2.58 Å thick WSi_2, [35] the large amount of WSi_2 formation resulted in a volume change of the W(450 nm) layer, consumption of Si substrate, and probably, a large residual stress. Because the W(450 nm)/p^+-n diodes remained stable up to 700°C, the degradation of Cu/W(450 nm)/p^+-n diodes at 700°C was attributed to the presence of the Cu overlayer.

XRD analyses.—Figure 7 shows XRD spectra for the W(450 nm)/Si samples annealed at various temperatures. Only an α-W diffraction peak was detected for the as-deposited sample, as well as those annealed at and below 625°C. After annealing at 650°C, weak peaks belonging to the WSi_2 phase were detected, indicating reaction between W and Si substrate. However, the small amount of WSi_2 formation at the W/Si interface did not degrade the electrical characteristics of W/p^+-n junction diodes (Fig. 6d). The peak intensity of the WSi_2 phase increased with increasing annealing temperature and the increase in WSi_2 peaks was also correlated with degradation of electrical characteristics for the W(450 nm)/p^+-n junction diodes (Fig. 6d). After annealing at 800°C, the WSi_2 peaks were further strengthened, while the α-W peak disappeared, indicating that the W(450 nm) layer might have converted into the WSi_2 phase completely.

Figure 8 shows XRD spectra for the samples of Cu/W(450 nm)/Si and Cu/WSiN/WSi_x/W(450 nm)/Si structures annealed at various temperatures. For the Cu/W(450 nm)/Si samples, no peak relating to the WSi_2 phase was observed after annealing at 600°C, indicating integrity of the samples' structure (Fig. 8a). After annealing at 700°C, diffraction peaks of the WSi_2 phase appeared along with a weak peak of the Cu_3Si phase. This indicates that Cu atoms penetrated through the W(450 nm) layers and reacted with the substrate Si, leading to formation of Cu_3Si compound and severe degradation in electrical characteristics of Cu/W(450 nm)/p^+-n junction diodes (Fig. 6b). In addition, the formation of Cu_3Si compound was probably correlated to the large amount of WSi_2 formation at the W/Si interface. Upon annealing at 750°C, the peaks of Cu(111) and Cu(200) disappeared while the peak of Cu_3Si phase was further strengthened (Fig. 8a). This suggested that the Cu overlayer might have converted into the Cu_3Si phase completely.

For the samples of Cu/WSiN/WSi_x/W(450 nm)/Si structure, though many diffraction peaks relating to the WSi_2 phase appeared, no peak relating to the Cu_3Si phase was detected, even after annealing at 750°C (Fig. 8b). This indicated that the WSiN/WSi_x/W stacked layer effectively suppressed Cu diffusion up to at least 750°C, regardless of the reaction at the W/Si interface. Thus, we may conclude that the barrier capability of the WSiN/WSi_x/W stacked layer against CU diffusion is superior to that of a single W layer. Weak diffraction peaks of the W_5Si_3 phase were observed after annealing at 650 and 700°C (Fig. 8b), but they all disappeared after annealing at 750°C.



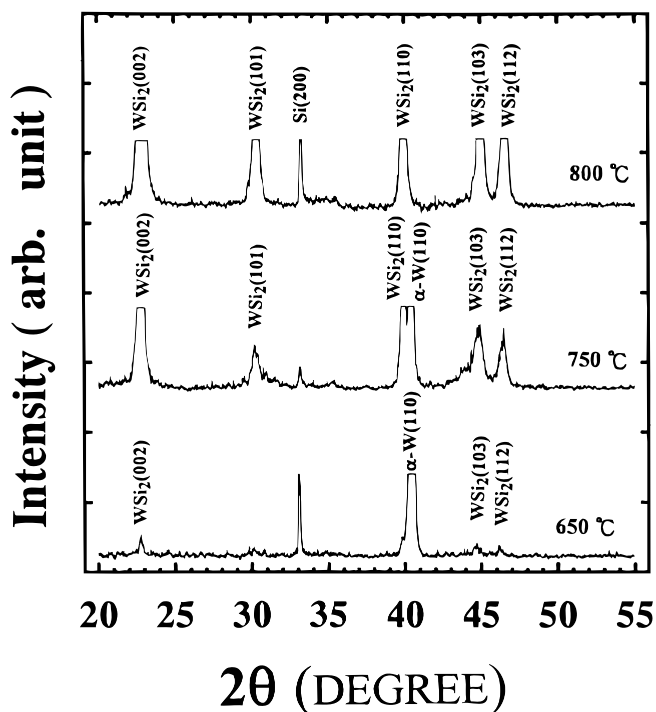


Figure 7. XRD spectra of W(450 nm)/Si samples annealed at various temperatures.

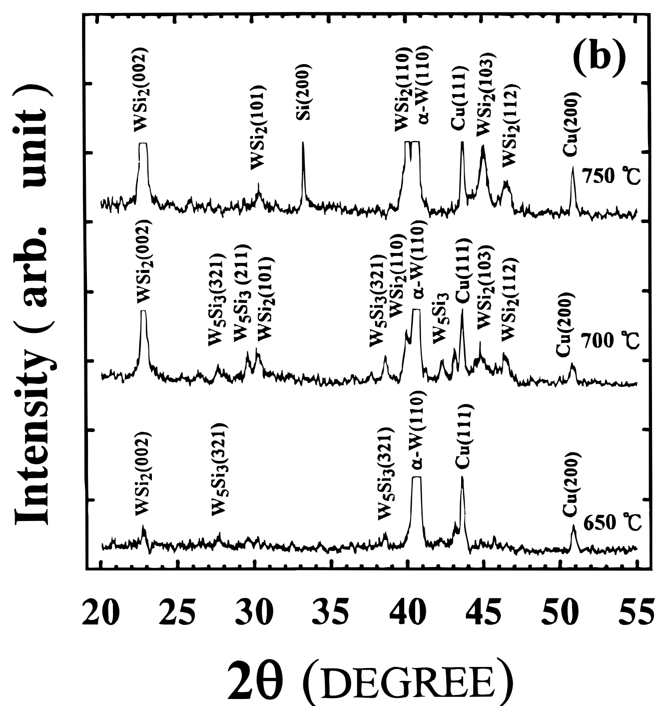


Figure 8. XRD spectra of (a) Cu/W(450 nm)/Si and (b) Cu/WSiN/WSi_x/W(450 nm)/Si samples annealed at various temperatures.

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Sheet resistance measurements.—The sheet resistance change in annealed samples, normalized to the sheet resistance value of as-deposited samples, is denoted as $\Delta Rs/Rs\%$ and defined as follows

$$\frac{\Delta Rs}{Rs}\% = \frac{Rs_{\text{after anneal}} - Rs_{\text{as-deposited}}}{Rs_{\text{as-deposited}}} \times 100\%$$

Figure 9 shows the percentage change in sheet resistance vs. annealing temperature for the samples of Cu(300 nm)/Si, W(450 nm)/Si, Cu/W(450 nm)/Si, and Cu/WSiN/WSi_x(75 nm)/W(450 nm)/Si structures. The sheet resistance of Cu/Si remained constant following anneal at temperatures up to 175°C but increased drastically after annealing at 200°C. The drastic increase in sheet resistance was attributed to the formation of high-resistivity η″-Cu_3Si precipitate and correlated to the degradation in electrical characteristics (Fig. 6a). For the W/Si structure, the increase in sheet resistance after annealing at 700°C reflects the consumption of conductive W films due to the formation of WSi_2, as confirmed by XRD analysis (Fig. 7). For the Cu/W/Si and Cu/WSiN/WSi_x/W/Si samples, the sheet resistance slightly decreased with annealing temperature up to 700°C, presumably due to out-diffusion of impurities atoms, grain growth of Cu films, and the heating up of sputter-induced damage in Cu films. Thermal stability of the Cu/W/Si multilayer structure reached 700°C, and a drastic increase in sheet resistance was found after annealing at 750°C, implying failure of the Cu/W/Si structure. the drastic increase in sheet resistance was attributed to the consumption of conductive Cu layers. It was possible that Si and Cu atoms interacted with each other by diffusing through the grain boundaries or defects in the thermally annealed W films. The XRD spectra for the 750°C-annealed Cu/W/Si samples clearly revealed strong peaks of WSi_2 phase (Fig. 8a). The large amount of WSi_2 formation not only resulted in a net volume change of the W layers, but also developed local defects (seams, microcracks, and stress-induced weak points) in the W layers. These defects in turn offered fast paths for Cu diffusion; thus, the Cu layers were consumed and the Cu_3Si compound was formed. Since the failure of Cu/W/p^+-n junction diodes occurred at 700°C, while the drastic increase in sheet resistance for the Cu/W/Si structure was found at 750°C, it is clear that the technique of electrical measurements is a very sensitive method for the detection of barrier failure. For the Cu/WSiN/WSi_x/W/Si samples, sheet resistance remained stable up to 750°C and only a moderate degradation was observed after annealing at 800°C. The results of sheet resistance measurements further confirmed that the thermal stability of the Cu/W/Si structure can be improved by inserting a WSiN/WSi_x bilayer between Cu and W films.

SEM observation.—To clarify the failure mechanism of barriers subjected to thermal annealing, SEM was used to observe the surface morphology and cross-sectional structure of thermally annealed Cu/barrier/p^+-n junction diodes. Figure 10 shows the top view and cross-sectional view SEM micrographs for the Cu/W(450 nm)/p^+-n junction diodes before and after thermal annealing at various temperatures. The Cu/W/Si structure remained stable after annealing at 650°C as compared with the as-deposited samples (Fig. 10a and b). This is consistent with the results of leakage current and sheet resistance measurements (Fig. 6b and Fig. 9). Even after annealing at 700°C, the surface of annealed samples retained a reddish-yellow Cu color. After annealing at 750°C, cross-sectional SEM observations

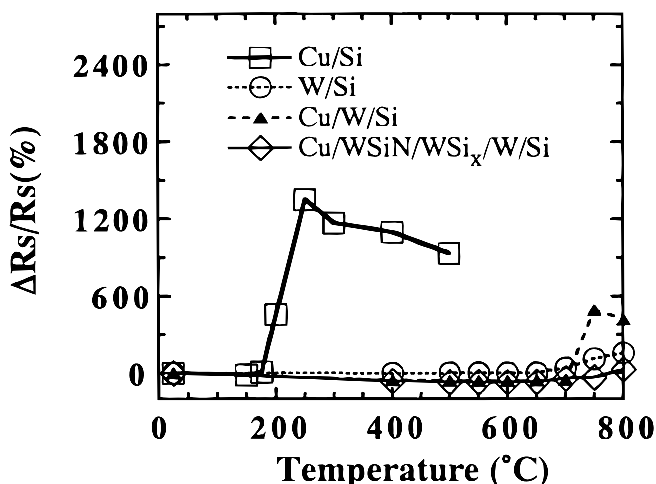

Figure 9. Percentage change in sheet resistance vs. annealing temperature for the samples of Cu(300 nm)Si, W(450 nm)/Si, and Cu/WSiN/WSi_x/W(450 nm)/Si structures.

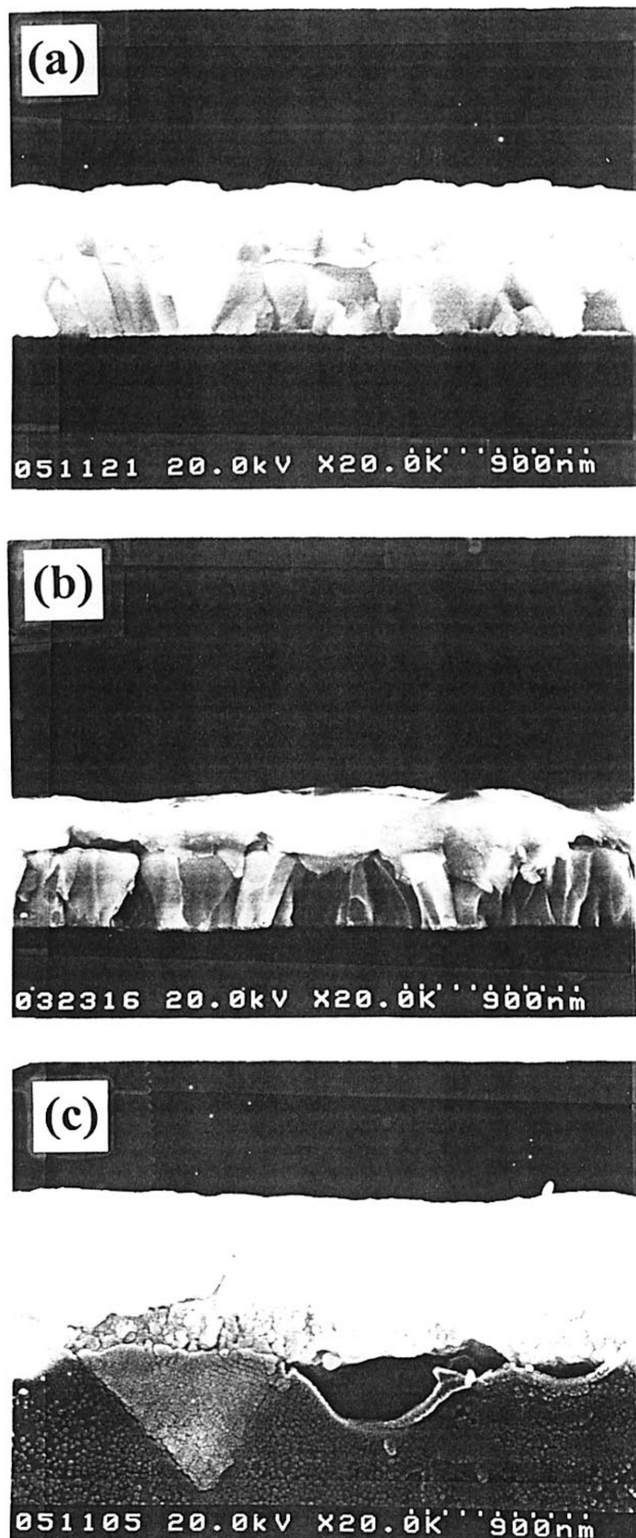

Figure 10. Cross-sectional view SEM micrographs for the Cu/W/p^+-n junction diodes: (a) as-deposited sample, (b) sample annealed at 650°C, and (c) sample annealed at 750°C.

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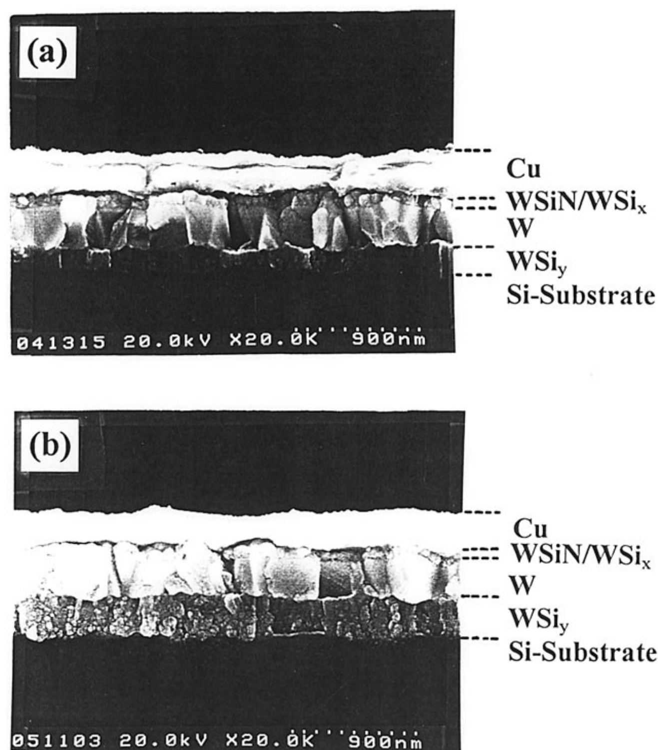

Figure 11. Cross-sectional view SEM micrographs for the Cu/WSiN/WSi_x/W/p^+-n junction diodes annealed at (a) 700 and (b) 750°C.

revealed large precipitates bounded by Si{111} planes and with an inverted pyramid shape (Fig. 10c). From the XRD spectra shown in Fig. 8a, we believe that the precipitates were Cu_3Si phase.[19,20] Moreover, a complete color change from coppery yellow to silver gray on the samples' surface was observed with the naked eye.

Figure 11 shows cross-sectional SEM micrographs for the thermally annealed Cu/WSiN/WSi_x/W(450 nm)/p^+-n junction diodes. For the 700°C-annealed samples, a WSi_y layer was formed between the original W layer and the Si substrate (Fig. 11a), while the observation with the naked eye on the Cu surface revealed no obvious change in coppery color. From the XRD spectra shown in Fig. 8b, we believe that the WSi_y layer was WSi_2 phase. After annealing at 750°C, the WSi_y layer become thicker, but Cu_3Si precipitates were not observed (Fig. 11b).

Conclusion

The barrier capability of selective CVD-W(450 nm) films as well as WSiN/WSi_x(75 nm)/W(450 nm) stacked layers used as a diffusion barrier between Cu and Si substrates against Cu diffusion was investigated. We found that the CVD-W layers functioned as an effective barrier against Cu diffusion, and the Cu/W(450 nm)/p^+-n junction diodes were able to sustain a 30 min furnace annealing up to 650°C without causing degradation in electrical characteristics. Thermal stability of the Cu/W/p^+-n diodes can be significantly improved by inserting an N_2-plasma-treated WSiN/WSi_x bilayer between the W and Cu overlayers, and the Cu/WSiN/WSi_x/W/p^+-n junction diodes were able to retain their integrity in electrical characteristics up to at least 700°C. Various evidences show that the thin WSiN layers formed by N_2 plasma treatment on the surfaces of WSi_x layers efficiently suppressed Cu diffusion and thus resulted in improvement of barrier capability. Failure of barrier capability for the W films was presumably due to interdiffusion of Cu and Si along grain boundaries of the W films, and the interdiffusion was probably enhanced by the formation of WSi_2.

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