Design of dynamic-floating-gate technique for output ESD protection in deep-submicron CMOS technology

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Received 13 May 1998; received in revised form 19 June 1998

Abstract

A novel dynamic-floating-gate technique is proposed to improve ESD robustness of the CMOS output buffers with small driving/sinking currents. This dynamic-floating-gate design can effectively solve the ESD protection issue which is due to the different circuit connections on the output devices. By adding suitable time delay to dynamically float the gates of the output NMOS/PMOS devices which are originally unused in the output buffer, the human-body-model (machine-model) ESD failure threshold of a 2-mA output buffer can be practically improved from the original 1.0 kV (100 V) up to greater than 8 kV (1500 V) in a 0.35-μm bulk CMOS process. © 1998 Elsevier Science Ltd. All rights reserved.

1. Introduction

Electrostatic discharge (ESD) robustness of CMOS IC's had been founded to be seriously degraded by the advanced deep-submicron CMOS technologies [1–3]. It is necessary to improve ESD protection for the output buffers through either process modification or more effective ESD protection circuit design [4]. In the TSMC (Taiwan Semiconductor Manufacturing Company) 0.35-μm CMOS technology, two extra process modifications had been used to improve ESD robustness of the output buffers. One is the modified ESD-implant process and the other uses the resist-protection-oxide (RPO) layer to block the silicided diffusion in the output buffers [5].

The lightly-doped-drain (LDD) structure had been used to reduce the electrical field around the drain region and therefore to overcome the hot-carrier effect of the short-channel transistors in submicron and deep-submicron CMOS technologies. The schematic cross-sectional view of an output NMOS with the LDD structure is shown in Fig. 1(a). But, the LDD structure has a diffusion peak extending from the drain region into the channel. Due to the peak-discharging

effect in the ESD events, the ESD current is often discharged through the LDD peak structure of the drain. Owing to the much shallow junction depth of the LDD structure, the drain of the output NMOS is easily damaged by the ESD current to cause a very low ESD reliability [1–3]. To improve ESD robustness of the output NMOS, the ESD-implant process had been widely used to eliminate the LDD peak structure in the output NMOS [3, 4]. The schematic cross-sectional view of the output NMOS with the conventional ESD-implant process is shown in Fig. 1(b), which is similar to the early long-channel device with a deeper junction depth. In the ESD-implanted output NMOS, the channel length has to be enlarged to reduce the hot-carrier effect on the output NMOS. Such an ESD-implanted output NMOS has a different device parameters to those having the LDD structure. So, the additional *HSPICE* parameters of the ESD-implanted output NMOS have to be extracted for circuit simulation.

In the TSMC 0.35-μm CMOS technology, a modified ESD-implant process is used to lowered the junction breakdown voltage of the drain junction, which is under the drain contact [5]. The schematic cross-sec-
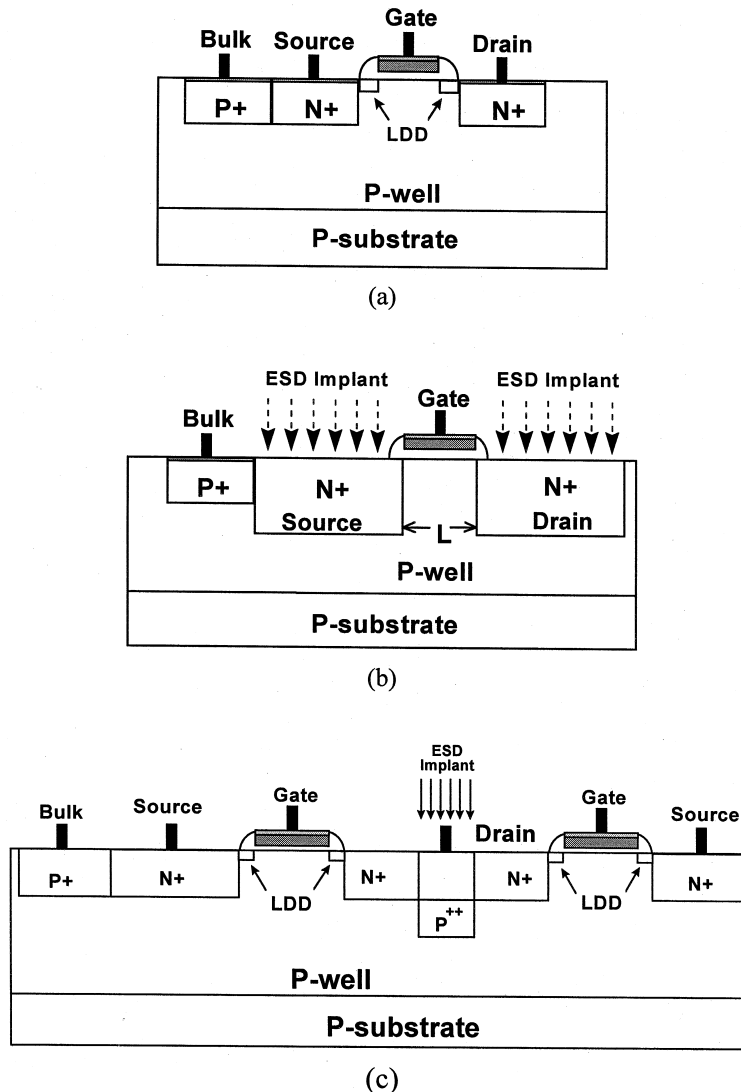
Fig. 1. The schematic cross-sectional views of (a) the output NMOS device with the LDD structure, (b) the output NMOS with the conventional ESD-implant process and (c) the output NMOS with the modified ESD-implant process.

tional view to illustrate the output NMOS with the modified ESD-implant process is shown in Fig. 1(c), where the ESD implantation is deeply implanted into the drain junction only around the drain contact to lower the junction breakdown voltage from the original 8 V to 6.5 V. The output NMOS with the modified ESD-implant process still keeps the LDD structure and a shorter channel length. The lower breakdown voltage of the modified ESD-implanted drain junction causes the ESD current to be discharged through the modified ESD-implanted drain region, which is far away from the LDD peak and the channel of the output NMOS. So, the modified ESD-implant process can effectively improve the ESD robustness of the output NMOS and still keep the LDD structure in the short-channel output NMOS to achieve better hot-carrier reliability.

To improve the operating speed of the integrated circuits in the deep-submicron CMOS technology, the silicided diffusion had been widely used to reduce the sheet resistance of the drain and source of the MOSFET. The sheet resistance of the silicided $N+$ diffusion in the 0.35-μm CMOS process is only 3.39 Ω/ square, whereas the non-silicided $N+$ diffusion in the same process has a sheet resistance of 87 Ω/square. The schematic cross-sectional view of an NMOS with the silicided diffusion is illustrated in Fig. 2(a). Such silicided diffusion can effectively improve the operating speed of the CMOS circuits. But, if the silicided diffusion is used in the output buffers, the ESD current

coming from the output pad is diverted into the drain region and only flows on the drain surface with the low-resistance silicided diffusion. The ESD current flowing through the drain surface easily touches the drain LDD peak structure and the channel of the output NMOS to cause a much lower ESD robustness. In the non-silicided diffusion process, a suitable layout spacing about 3–5 μm from the drain contact to the poly-gate edge is often used to improve ESD robustness of the output buffers [6]. But, in the silicided diffusion process, even a wider spacing from the drain contact to the poly-gate edge still can not improve

ESD level of the output buffers due to the much low sheet-resistance of silicided diffusion on the drain surface.

The process modification in the TSMC 0.35-μm CMOS technology to overcome the negative impact of silicided diffusion on ESD protection is to use an extra resist-protection-oxide (RPO) layer to block the silicided diffusion in the output transistors [5]. The schematic cross-sectional view of the silicided-blocking output NMOS is shown in Fig. 2(b). A finger-type layout example to realize the silicide-blocking output NMOS by using the extra RPO mask layer is shown in
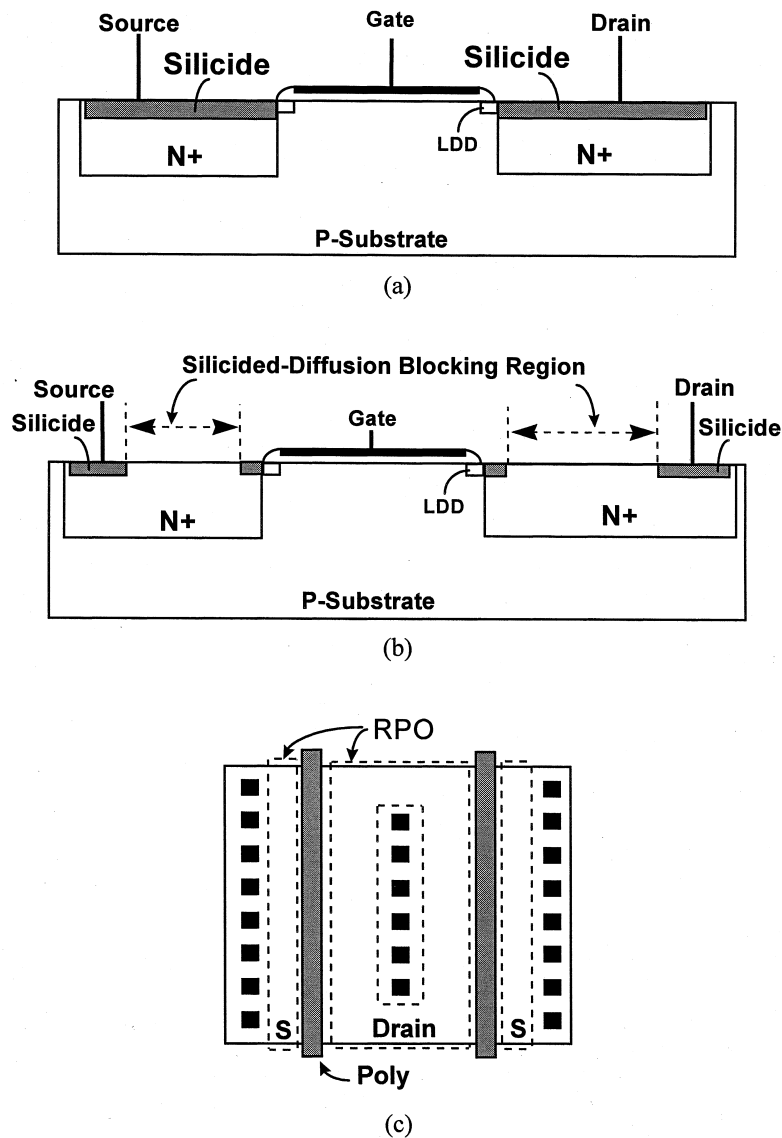

Fig. 2. (a) The schematic cross-sectional view of an NMOS device with the silicided diffusion, (b) the schematic cross-sectional view of an NMOS device with the silicide-blocking diffusion and (c) a layout style for using the RPO layer to block the silicided diffusion in the output NMOS.

Fig. 2(c). The RPO mask layer provides the output NMOS with the non-silicided diffusion in both the drain and source of the output NMOS to rescue ESD level of the output buffer. An output NMOS with a device dimension (W/L) of 420/0.5 (μm/μm) and a spacing from the drain contact to poly-gate edge of 3.4 μm in the 0.35-μm CMOS process without process modification for ESD protection fails to the human-body-model (HBM) ESD stress of 2 kV. But, if the RPO layer and the modified ESD-implant process are used, such an output NMOS can sustain the HBM

ESD stress of above 5 kV. This shows the effectiveness of ESD protection through the advanced process modifications.

Besides the advanced process modifications to improve ESD robustness of the output buffers, the symmetrical layout structure is much emphasized to realize the large-dimension output transistors by ensuring the uniform turn-on phenomenon along the multiple fingers of the output transistor [7]. To more enhance the uniform turn-on phenomenon among the multiple fingers of the output transistors, a gate-
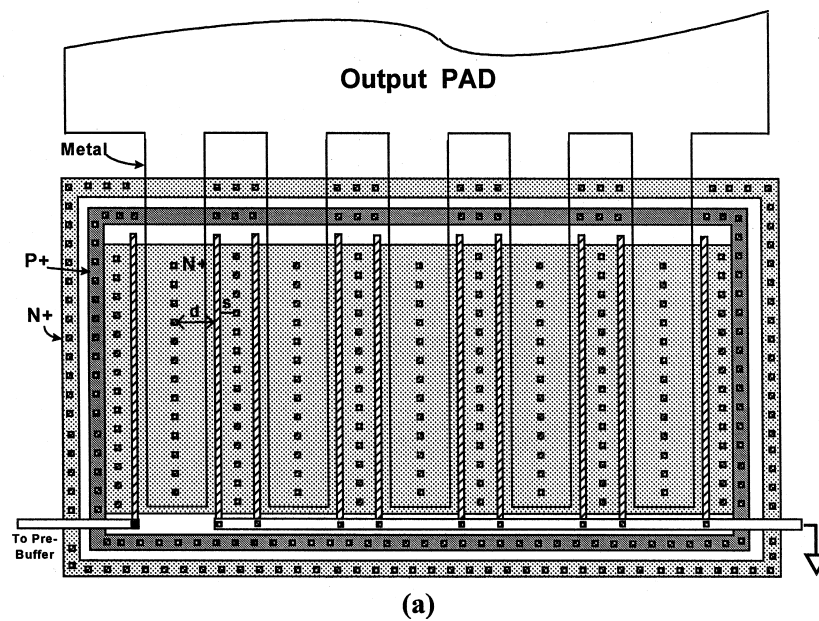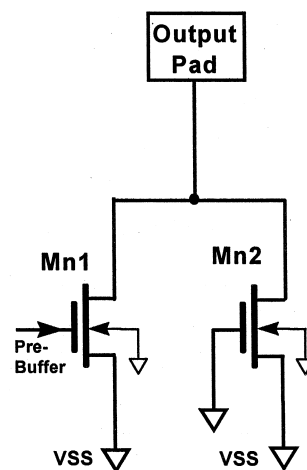
Fig. 3. (a) The schematic layout of an output NMOS in a cell library with a small driving specification. (b) The equivalent circuit of the layout in (a) with a small-driving-current NMOS Mn1 and a large-dimension but unused NMOS Mn2.

coupled design had been reported to achieve uniform ESD power distribution on the large-dimension output transistors [8–12]. But in the practical applications, the output buffers in a cell library have different driving specifications. For example, the output buffers may have the driving capability of 2, 4, 8, ... or 24 mA. But, the cell layouts of the output buffers with different driving capabilities are still drawn in the same layout style and area for programmable application. To adjust different output sinking (driving) currents of the output buffer, different fingers of the poly gates in the output NMOS (PMOS) are connected to the pre-buffer circuit, but the other unused poly-gate fingers are connected to ground (VDD). A typical layout example of the finger-type output NMOS with a small driving current is shown in Fig. 3(a), whereas the equivalent circuit is shown in Fig. 3(b). In Fig. 3(a), there are 10 poly-gate fingers in the NMOS layout, but only a poly-gate finger (Mn1) is connected to the pre-buffer circuit to provide the sinking current from the output pad. The other 9 poly-gate fingers (Mn2) are connected to ground to keep the NMOS (Mn2) off which is unused but inside the cell layout of the output buffer. Due to the asymmetrical connection on the poly-gate fingers of the output NMOS in the layout, the ESD turn-on phenomenon among the fingers becomes quite different even if the layout in Fig. 3(a) is so symmetrical. The output Mn1 is often turned on first and damaged by the ESD voltage, whereas the unused Mn2 with a much larger channel width is always off during the ESD stress. This generally causes a very low ESD level for the output buffer, even if the output buffer has a very large total device dimension (Mn1 + Mn2).

In this paper, a novel dynamic-floating-gate technique is proposed to improve ESD level of the output buffers with different driving specifications in the cell library [13]. The gates of the unused NMOS/PMOS in the output buffer are dynamically floated during the ESD stress, so such unused NMOS/PMOS with large device dimensions can be turned on in time to bypass the ESD current. Thus, the overall ESD level of such output buffers can be significantly improved.

2. Traditional gate-coupled output ESD protection

The ESD test to verify the ESD level of an output pin is shown in Fig. 4, where there are four modes of testing combinations from the output pin to the VDD or VSS pins [14]. In the ND-mode (PS-mode) ESD stress, the output PMOS (NMOS) is reverse biased and broken down by the ESD voltage. But, in the NS-mode (PD-mode) ESD stress, the parasitic drain-to-bulk diode in the NMOS (PMOS) is forward biased to bypass the ESD current. Due to the low operating voltage, the diode in the forward-biased condition can sustain much high ESD stress. However, the NMOS or PMOS in the breakdown condition with high snap-back voltage are easily damaged by the ESD energy. Thus, the worst cases of the ESD stresses on an output buffer are the ND- and PS-mode ESD events.

To enhance the turn-on uniformity of the output buffers by using the traditional gate-coupled technique, the poly gates of the unused NMOS (PMOS) in the output buffers are connected to VSS (VDD) through a small-dimension NMOS Mdn1 (PMOS Mdp1) [11], as shown in Fig. 5. The Mdn1 (Mdp1) cooperated with
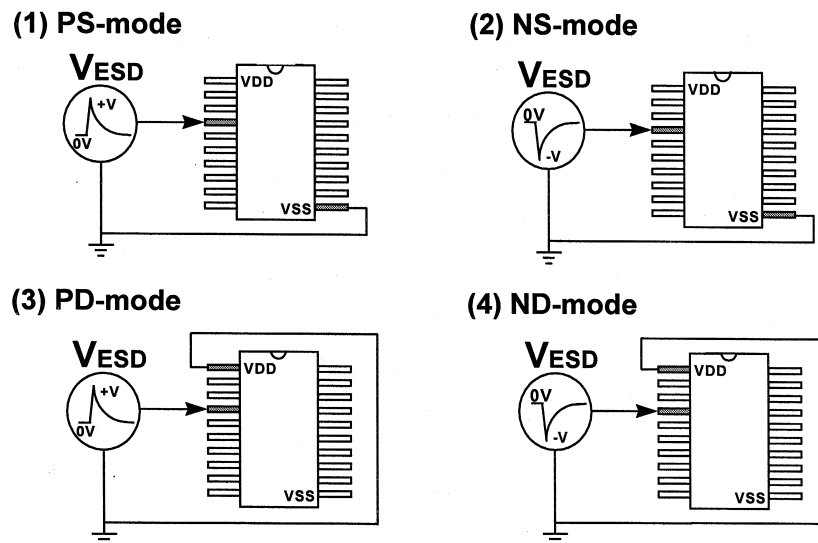
Fig. 4. The combinations of ESD stresses from an output pin to the VDD or VSS pins.

the parasitic drain-to-gate capacitance in the Mn2 (Mp2) performs the gate-coupled effect to turn on the Mn2 (Mp2) during the ESD stress [10–12]. In the normal operating conditions, the gate of Mp2 (Mn2) is connected to VDD (VSS) through the turned-on Mdp1 (Mdn1) to keep the unused Mp2 (Mn2) off. For an output buffer with a smaller driving/sinking current, such as only 2 mA, the device dimension of the Mn1 (Mp1) is much smaller than that of the Mn2 (Mp2). In a 0.35-μm CMOS cell library, the 2-mA output buffer has the device dimension (W/L) of 30/0.5 (μm/μm) for both the Mn1 and Mp1. But, in the cell layout of the 2-mA output buffer, it also has the device dimension of 450/0.5 (690/0.5) for the Mn2 (Mp2). The device dimensions of the Mdn1 and Mdp1 are both designed as 20/0.35 (μm/μm).

In the PS-mode ESD stress shown in Fig. 4, the VDD is floating and the VSS is relatively grounded. When the PS-mode ESD voltage attaches the output pad of Fig. 5, some transient voltage is coupled through the parasitic drain-to-gate capacitor to the gates of Mn1 and Mn2. The coupled voltage is expected to be held on the gates of Mn2 by the Mdn1. Therefore, the unused Mn2 with a large device dimension is expected to be turned on to bypass the ESD current from the pad to VSS. However, the positive ESD voltage on the pad is also diverted into the VDD power line through the parasitic diode Dp2 (Dp1) in the Mp2 (Mp1). The Mdn1 with its gate connected to the VDD power line is quickly turned on during the PS-mode ESD transition. The coupled voltage on the gate of Mn1 is held on its gate, but the coupled voltage on the gate of Mn2 is discharged by the turned-on Mdn1. During the ESD transition, the Mn1 with a

smaller device dimension is actually triggered on and damaged by the ESD energy but the large-dimension Mn2 with the gate-coupled design is still kept off. On the other hand, in the ND-mode ESD stress, the coupled voltage on the gate of Mp2 is discharged by the turned-on Mdp1, because the negative ESD voltage on the pad is conducted into the VSS power line through the parasitic diode Dn2 (Dn1) in the Mn2 (Mn1) to turn the Mdp1 on. The ND-mode ESD current is still mainly discharged through the Mp1 with a smaller device dimension. Thus, such an output buffer with the gate-coupled design still has a very low ESD level even if the modified ESD-implant process and silicided-blocking diffusion are used in the output buffer.

The output buffers with different driving/sinking current specifications are tested in the HBM (human-body-model) ESD event by the *Zapmaster* ESD tester. The advanced process modifications with both the modified ESD-implant process and the silicide-blocking diffusion are used in all the output buffers. The PS-mode and ND-mode ESD test results are summarized in Table 1. Due to the different connections on the gates of the output Mn1 and the unused Mn2, the PS-mode ESD level of the 2-mA output buffer is only 1 kV. But the 8-mA output buffer can sustain the PS-mode ESD voltage of 2 kV. While the driving/sinking current of the output buffer is increased with a larger device dimension on Mn1, the output buffer has a higher ESD level (>2.5 kV). Although the cell layout areas and the total device dimensions (Mn1 + Mn2) of these output buffers (2 mA, 4 mA, …) are all the same in the cell library, the ESD level of these output buffers are quite different. Even if using the NMOS
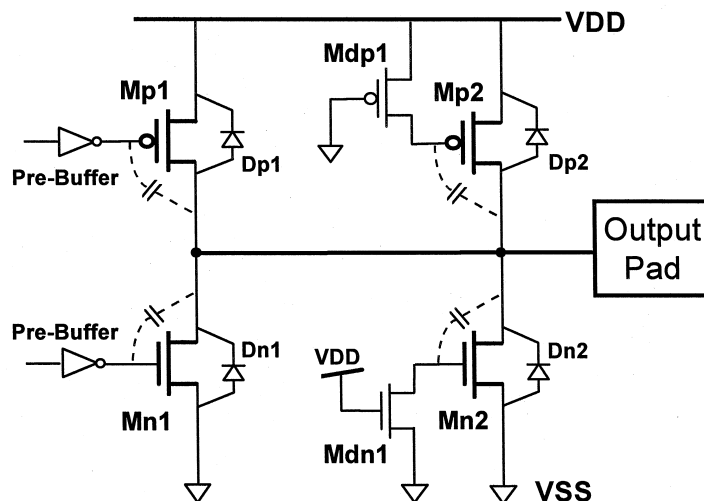

Fig. 5. The output buffer of a small driving/sinking current in a 0.35-μm cell library. The gate of the unused Mn2 (Mp2) is connected to VSS (VDD) through a small-dimension Mdn1 (Mdp1) to perform the gate-coupled effect for ESD protection.

Table 1
The human-body-model (HBM) ESD level of the output buffer protected by the traditional gate-coupled design (Fig. 5)

HBM ESD stress	Output buffers (kV)				
	2-mA buffer	4-mA buffer	8-mA buffer	12-mA buffer	24-mA buffer
ND-Mode	1.5	2	2.5	> 2.5	> 2.5
PS-Mode	1.0	1.5	2.0	> 2.5	> 2.5

Mdn1 (PMOS Mdp1) to perform the gate-coupled effect to help the uniform turn-on between the Mn1 and Mn2 (Mp1 and Mp2), the HBM ESD level of the output buffer with a small Mn1 (Mp1) but a large Mn2 (Mp2) is still below the general industrial HBM ESD specification of 2000 V. Detailed failure analysis by de-layer process is applied to find the ESD failure location on a 4-mA output buffer which is stressed and damaged by a PS-mode ESD voltage of 2 kV. The SEM picture of the ESD failure on the 4-mA output buffer is shown in Fig. 6(a), where the ESD damage indicated by an arrow is located on the Mn1 device of the output buffer. The ESD damage in Fig. 6(a) is zoomed in and shown in Fig. 6(b). The fingers of the Mn2 device have no ESD damage in the de-layered output buffer.

To investigate the gate-coupled effect in more details, the 2-mA output buffer with the circuit configuration in Fig. 5 is simulated by *HSPICE*. In the *HSPICE* circuit simulation, a ramp voltage with a rise time of 10 ns and a pulse height of 7 V is applied to the output pad to simulate the rising edge of the HBM PS-mode ESD voltage. The pulse height in the simulation is set as 7 V to find the gate-coupled effect before the drain of the output NMOS is broken down by the ESD voltage, because the drain breakdown voltage of NMOS in the 0.35-μm CMOS process is about 8 V. The rise time of an HBM ESD pulse has been specified as 2 to 10 ns in the EOS/ESD association standard [14], therefore the rise time of the stress voltage in the *HSPICE* simulation is set as 10 ns. The initial voltage at all nodes of the circuit in Fig. 5 is set to 0 V before the ESD-simulated ramp voltage is applied to the output pad. The simulated gate-coupled voltage waveforms on the gates of Mn1 and Mn2 are shown in Fig. 7(a), whereas the simulated drain current waveforms in the time domain through the Mn1 and Mn2 are shown in Fig. 7(b). During the simulation time period from 10 to 20 ns, the applied ramp voltage is risen from 0 to 7 V. The coupled voltage on the gate of Mn1 is kept at about 0.56 V, but the coupled voltage on the gate of Mn2 is discharged by the Mdn1 to 0 V. In Fig. 7(b), the drain current of Mn1 is increased and kept at about 61 μA. The raising edge of the ramp voltage generates the transient current about 300–400

μA through the parasitic capacitance of the Mn2, but after the rising transition the drain current of Mn2 is dropped to zero. Because the coupled voltage on the gate of Mn2 is discharged by the Mdn1, the Mn2 is almost off during the PS-mode ESD transition. The traditional gate-coupled design on the Mn2 with the Mdn1 device can not really turn the Mn2 on before the Mn1 is triggered on in such CMOS output buffers.

Similar simulation is also applied to investigate the turn-on behavior during the ND-mode ESD stress on the output buffer of Fig. 5. A ramp voltage with a fall time of 10 ns and a pulse height of −7 V is used to simulate the falling edge of the HBM ND-mode ESD voltage before the output buffer is broken down by the ESD voltage. During the ND-mode ESD stress, the VDD is grounded but the VSS is floating. The initial voltage at all nodes is also set as 0 V before the ND-mode ESD voltage is applied to the output pad. The simulated voltage waveforms on the gates of Mp1 and Mp2 are shown in Fig. 8(a), whereas the simulated drain current waveforms of Mp1 and Mp2 are shown in Fig. 8(b). After the triggering of the 10-ns falling edge, the gate voltage of Mp1 is kept at about −0.69 V but that of the Mp2 is returned to 0 V. In Fig. 8(b), The 10-ns falling edge of the simulated ND-mode ESD voltage generates a peak transient current about −750 μA on the drain of Mp2. After the falling-edge triggering, the drain current of Mp2 is returned to zero but that of Mp1 is kept at about −8.5 μA. This verifies that the gate-coupled design in Fig. 5 can not really turn the Mp2 on to bypass the ND-mode ESD current.

Through the detailed investigation, the *HSPICE* simulation and ESD test results have proved that the traditional gate-coupled design in Fig. 5 by only using the Mdn1 (Mdp1) to hold the coupled voltage on the gate of Mn2 (Mp2) can not improve ESD robustness of the output buffers. Such output ESD protection issue due to different connections on the gates of the output Mn1 (Mp1) and the unused Mn2 (Mp2) can not be improved by only using the advanced process modifications. Some circuit design technique has to be invented to really improve ESD robustness of the output buffers with different driving/sinking currents in a cell library.
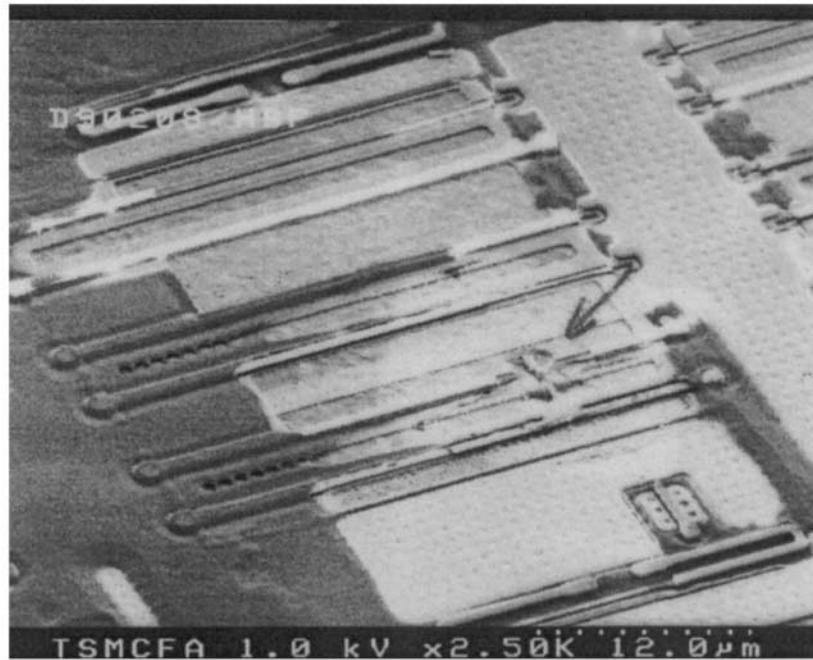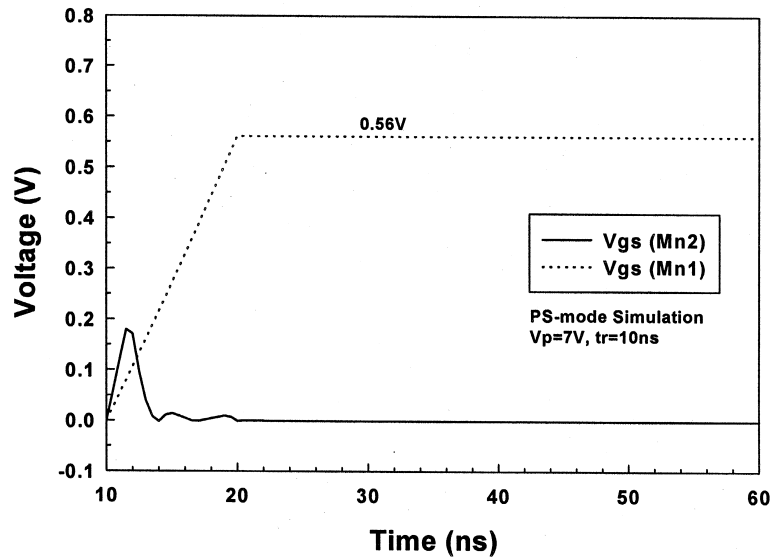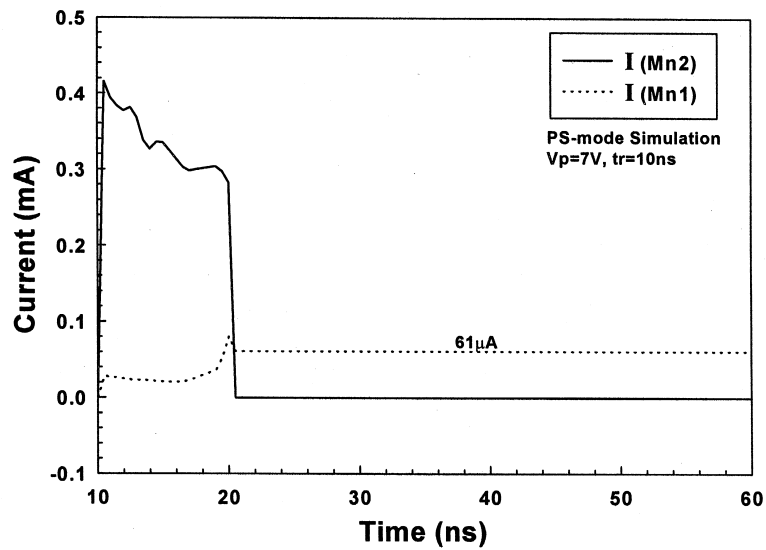
(a)

(b)

Fig. 6. (a) The SEM picture of the ESD damage location on the Mn1 of a 4-mA output buffer in the 0.35-μm CMOS process. (b) The zoom-in picture to show the ESD damage located on the Mn1 due to the PS-mode ESD stress with the HBM ESD voltage of 2 kV.
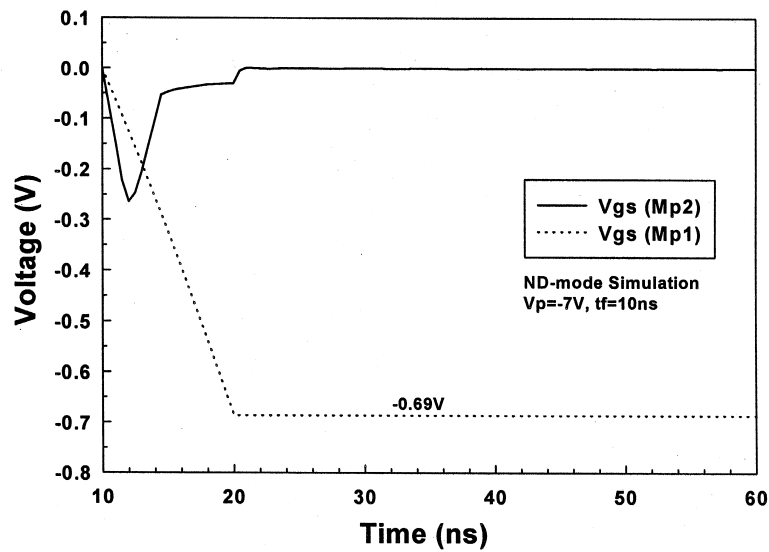
(a)

(b)

Fig. 7. (a) The simulated voltage waveforms on the gates of Mn1 and Mn2 and (b) the simulated drain current waveforms of Mn1 and Mn2, in the output circuit of Fig. 5, due to the triggering of a PS-mode ESD voltage with a rise time of 10 ns and a pulse height of 7 V.

3. Output ESD protection with the dynamic-floating-gate technique

As shown in Section 2, the low ESD level of an output buffer with a small driving/sinking current is due to the loss of the gate-coupled voltage on the gates of the unused Mn2 and Mp2 during ESD transition. If the gate-coupled voltage can be really held on the gates of the Mn2 and Mp2, the output buffer with a small driving/sinking current but with the unused Mn2 and Mp2 of large device dimensions can be effectively improved.
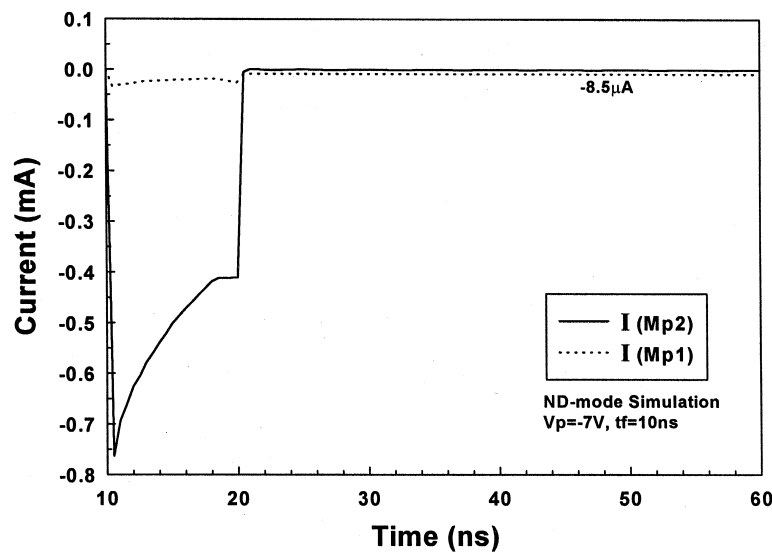
Fig. 8. (a) The simulated voltage waveforms on the gates of Mp1 and Mp2 and (b) the simulated drain current waveforms of Mp1 and Mp2, in the output circuit of Fig. 5, due to the triggering of a ND-mode ESD voltage with a fall time of 10 ns and a pulse height of −7 V.

3.1. Circuit configuration

The proposed dynamic-floating-gate technique to improve ESD robustness of a small-driving output buffer is shown in Fig. 9. As compared to the gate-coupled output buffer in Fig. 5, two additional MR2 and MC2 devices are designed to dynamically float the gate of Mp2 during the ND-mode ESD-stress condition, but the gate of Mp2 is connected to VDD in the normal operating condition. Two additional MR1 and MC1 devices are also used to dynamically float the gate of Mn2 during the PS-mode ESD-stress con-
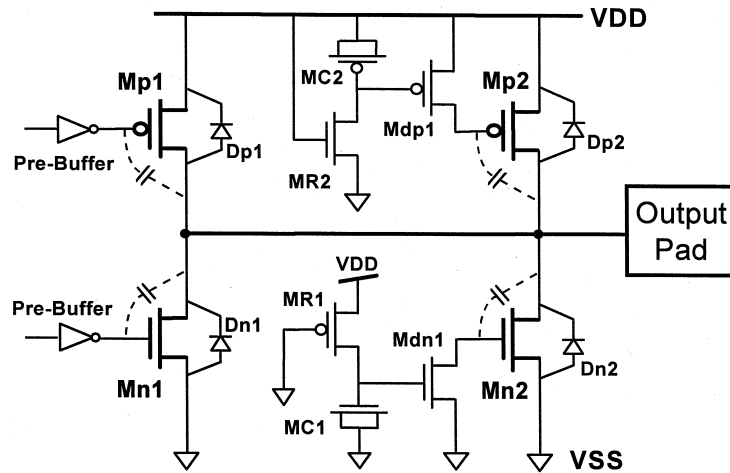
Fig. 9. The dynamic-floating-gate design to improve ESD level of the small-driving output buffers in a 0.35-μm cell library.

dition, but the gate of Mn2 is connected to VSS in the normal operating condition. The MC1 and MC2 devices are functioned as the capacitors and the MR1 and MR2 devices are functioned as the resistors. Because the gate of Mn2 (Mp2) is floated in a time period during the PS-mode (ND-mode) ESD transition, the coupled voltage through the drain-to-gate capacitance can be really held on the gate of Mn2 (Mp2) to turn on the Mn2 (Mp2) to bypass ESD current. Because the Mn2 and Mp2 have large device dimensions, the turned-on Mn2 and Mp2 can sustain a much higher ESD level. Therefore, the ESD robustness

of the output buffers in the 0.35-μm cell library can be significantly improved.

A practical layout example of a 2-mA output buffer with the dynamic-floating-gate design is demonstrated in Fig. 10. The additional MR1 and MR2 have the device dimension (W/L) of 1.7/45 (μm/μm) to perform a high resistance and the MC1 and MC2 have the device dimension of 65/8 (μm/μm) to perform a high capacitance to realize the dynamic-floating-gate design. The typical cell layout of the 2-mA output buffer in a 0.35-μm SPQM CMOS process occupies a total layout area of only 84×235 μm^2 which includes the double guard rings to prevent latchup issue.
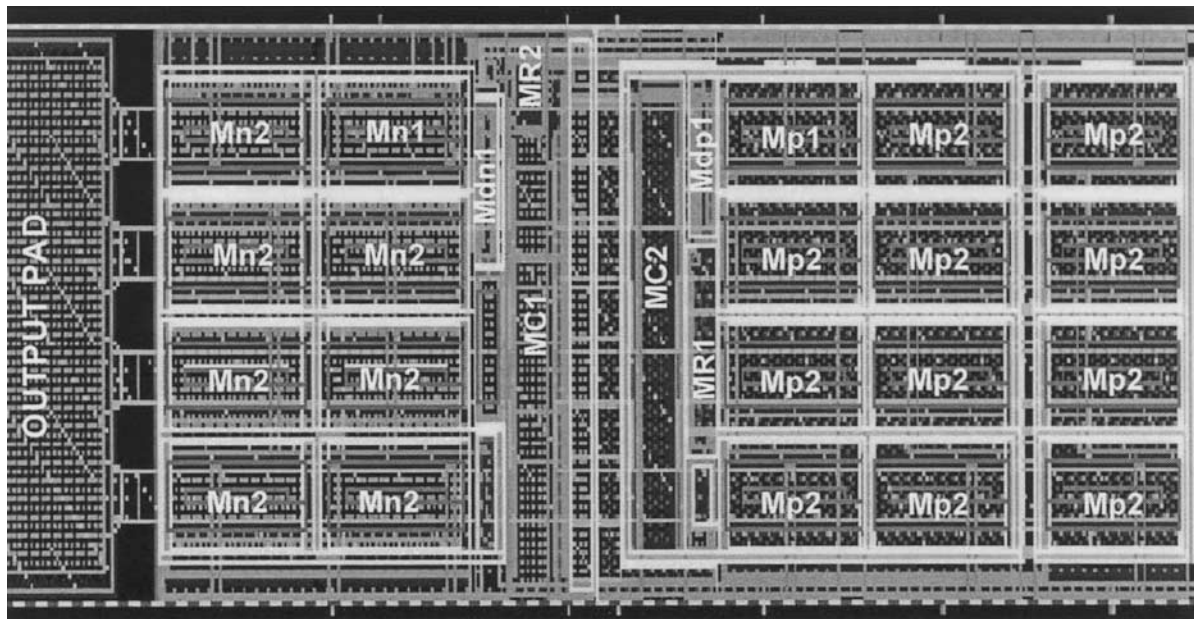

Fig. 10. The layout example of the 2-mA output buffer in the tsmc 0.35-μm cell library with the dynamic-floating-gate design.

3.2. The dynamic-floating-gate mechanism

In the PS-mode ESD stress, the positive ESD voltage is applied to the output pad with grounded VSS but VDD is floating. Due to the sharp rising edge of the ESD voltage, the gates of Mn2 and Mn1 are coupled with some positive voltage through the drain-to-gate parasitic capacitance in the Mn2 and Mn1. During the PS-mode ESD stress, the positive ESD voltage on the pad is also diverted into the floating VDD power line through the parasitic diode Dp2 (Dp1) in the Mp2 (Mp1). The drain of MR1 is therefore charged by the ESD voltage on the VDD power line. The gate-grounded PMOS MR1 functions as a resistor to charge the gate of Mdn1. The NMOS MC1 functions as a capacitor to store the gate voltage of Mdn1. Initially, the voltage stored on the capacitor MC1 is zero before the ESD voltage is applied to the output pad. But, the voltage stored on the capacitor MC1 is increased through the MR1 after the VDD power line is charged by the ESD current through the Dp2 and Dp1. The speed of the increase on the gate voltage, which is stored on the MC1, is strongly dependent on the RC time constant of the resistor MR1 and the capacitor MC1. The MR1 is especially designed with a high resistance and the MC1 is drawn with a large capacitance. Such design causes the gate voltage of Mdn1 to be kept below its threshold voltage in a long time. Because the Mdn1 is kept off in a long time, the gate of the unused Mn2 is therefore dynamically floated in the corresponding time period. A larger resistor MR1 and a lager capacitor MC1 lead to a longer time period to float the gate of the unused Mn2. By using this dynamic-floating-gate design, the coupled voltage through the drain-to-gate capacitance of Mn2 can be held on the gate of Mn2 in an enough long time period. So, the unused Mn2 with a large device dimension in the small-driving output buffer can be instantaneously turned on to bypass ESD current from the output pad to VSS. Owing to the effective turn-on of the unused large-dimension Mn2, the PS-mode ESD level of such a small-driving output buffer can be significantly improved.

In the ND-mode ESD stress, the negative ESD voltage is applied to the output pad with grounded VDD but VSS is floating. The negative ESD voltage on the pad is diverted into the floating VSS power line through the parasitic diode Dn2 (Dn1) in the Mn2 (Mn1). The NMOS MR2 with its gate connected to VDD functions as a resistor, whereas the PMOS MC2 functions as a capacitor. The negative ESD voltage on the VSS power line charges the gate of Mdp1 through the MR2. The speed of the decrease on the gate voltage of Mdp1 is strongly dependent on the RC time consist of the resistor MR2 and the capacitor MC2. A high-resistance MR2 and a large-capacitance MC2 are

therefore designed to keep the Mdp1 off in a longer time, so the gate of the unused Mp2 can be dynamically floated in a longer time period. The dynamic-floating time on the gate of Mp2 can be adjusted by simply changing the RC time constant of the resistor MR2 and the capacitor MC2. By this dynamic-floating-gate design, the negative ESD-coupled voltage through the drain-to-gate capacitance of Mp2 can be held on the gate of Mp2 in an enough long time period. So, the unused Mp2 with a large device dimension can be instantaneously turned on to bypass the negative ESD voltage from the output pad to the grounded VDD. Owing to the turn-on of the unused large-dimension Mp2, the ND-mode ESD level of such a small-driving output buffer can be significantly improved.

3.3. HSPICE simulation

To investigate the efficiency of the dynamic-floating-gate technique in the 2-mA output buffer, the output circuit is simulated by the HSPICE. The device dimensions of the 2-mA output buffer including the additional devices to realize the dynamic-floating-gate design have been described in Section 3.1.

3.3.1. PS-mode ESD-stress condition

An ESD-like ramp voltage pulse is added to the output pad with a pulse height of 7 V and a rise time of 10 ns to simulate the rising edge of the PS-mode ESD voltage. The transient voltages on the gates of Mn1 and Mn2 are monitored and shown in Fig. 11(a), whereas the discharging currents through the drains of Mn1 and Mn2 are shown in Fig. 11(b). As comparing to the simulation waveforms in Fig. 7, the dynamic-floating-gate design really keeps the transient-coupled voltage on the gate of Mn2. The coupled voltages on the gate of Mn1 in Fig. 7(a) and Fig. 11(a) are still the same, but those on the gate of Mn2 between the Fig. 7(a) and Fig. 11(a) are quite different. The gate voltage of Mn2 in Fig. 11(a) can be risen up to 0.96 V, therefore the Mn2 can be turned on to provide a drain current of 52.2 mA in Fig. 11(b). Such a drain current of 52.2 mA in the Mn2 is due to the triggering of a 7-V ramp voltage to simulate the turn-on behavior of the 2-mA output buffer with the dynamic-floating-gate design. In the real ESD events, the ESD voltage can be up to several thousands volts with the ESD current in the order of several Amperes. With such high ESD voltage and current, the Mn2 is triggered into the snapback region to bypass the ESD current. The simulation waveforms shown in Fig. 11 are only used to prove that the coupled voltage can be actually held on the gate of Mn2 during the rising edge of the ESD voltage. So, the Mn2 can be guaranteed to be quickly
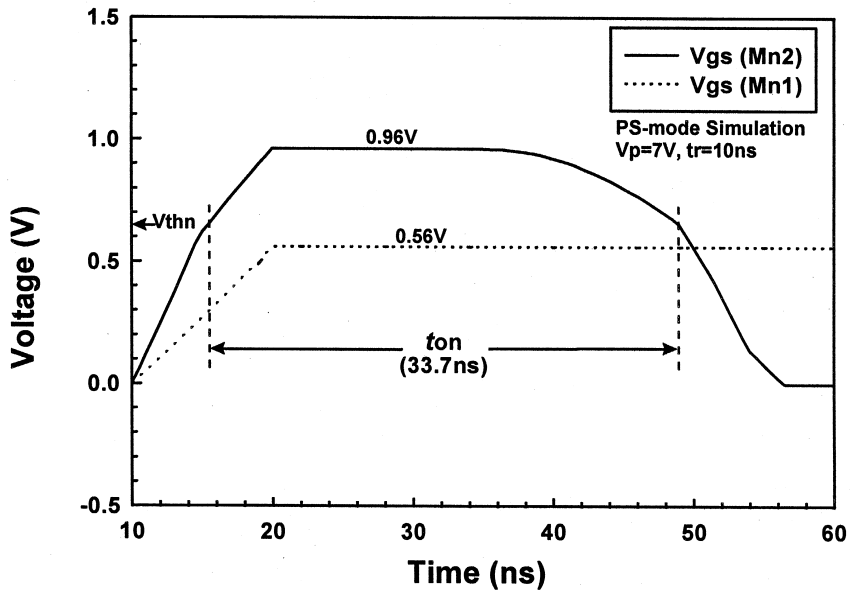
(a)
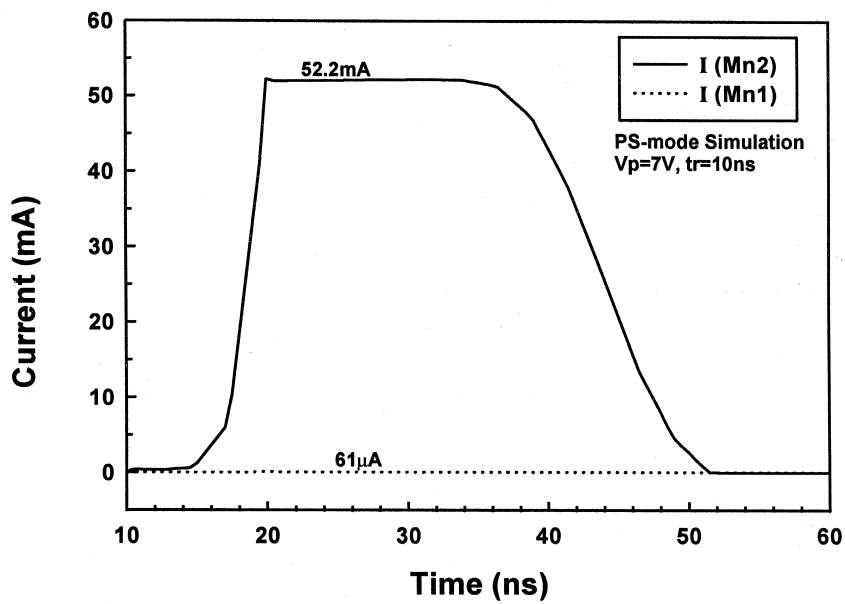
(b)

Fig. 11. (a) The transient voltages on the gates of the output Mn1 and the unused Mn2 and (b) the discharging currents through the output Mn1 and the unused Mn2, during the PS-mode simulation on the 2-mA output buffer with the dynamic-floating-gate design.

turned on to discharge ESD current before the Mn1 is damaged by the ESD voltage.

The turn-on time of Mn2, shown in Fig. 11(a), is defined as the time period when the coupled voltage on the gate of Mn2 is greater than its threshold voltage. The threshold voltage of NMOS in the 0.35-μm SPQM CMOS process under 3.3 V bias is 0.65 V. The turn-on time of Mn2 due to the 7-V PS-mode voltage triggering is about 33.7 ns. A higher ESD voltage on the pad couples a higher voltage to the gate of

Mn2 and also causes a longer turn-on time on the Mn2. Changing the device dimensions of the MR1 and MC1 can modify the *RC* time constant in the dynamic-floating-gate design, therefore the turn-on time of Mn2 can be adjusted. The simulation results on the turn-on time of Mn2 by changing the channel length and width of MR1 with a fixed W/L of 65/8

(μm/μm) in the MC1 are shown in Fig. 12(a). The MR1 with a longer channel length or a narrower channel width leads to a longer turn-on time on the Mn2 due to the 7-V PS-mode voltage triggering. As shown in Fig. 12(a), the turn-on time of Mn2 is linearly dependent on the channel length and the channel width of MR1. The dependence of the turn-on time of
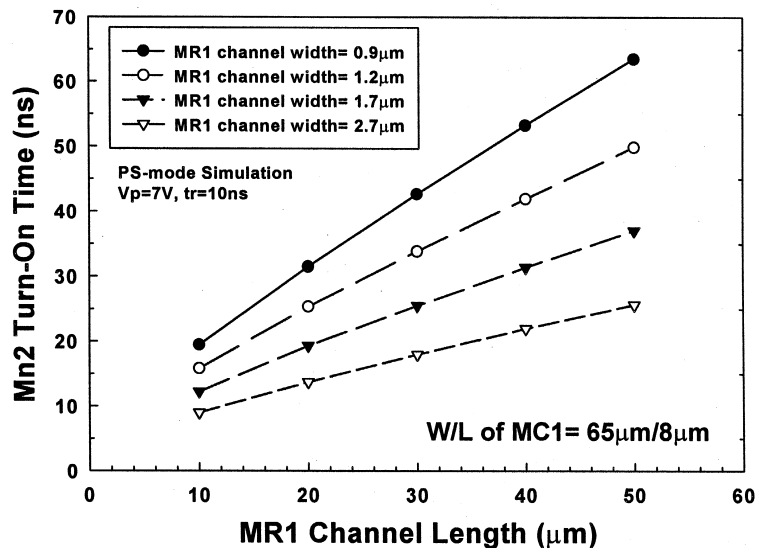

(a)
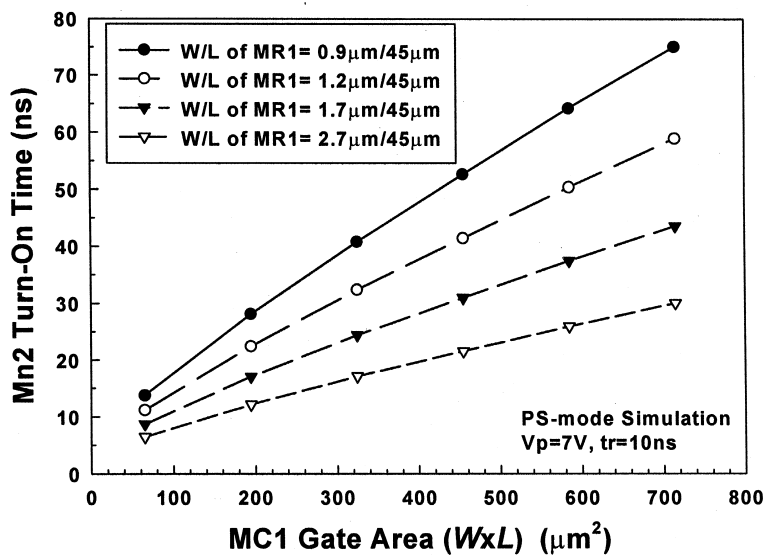
(b)

Fig. 12. The simulation results on the variation of the turn-on time in Mn2 by (a) changing the channel length and width of MR1 with a fixed W/L of 65/8 (μm/μm) in the MC1 and (b) changing the gate area (W × L) of MC1 under different W/L of the MR1, during the PS-mode simulation on the 2-mA output buffer with the dynamic-floating-gate design.

Mn2 on the gate area (W × L) of MC1 due to the 7-V PS-mode triggering is shown in Fig. 12(b) with different device dimensions of the MR1. In Fig. 12(b), the turn-on time of Mn2 is linearly dependent on the gate area of the MC1 in the output buffer with the dynamic-floating-gate design. A larger gate area of
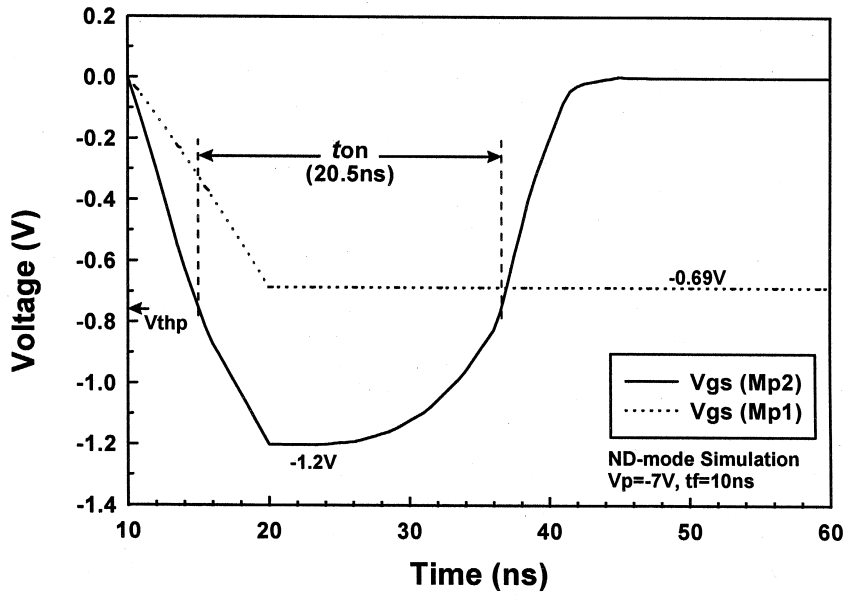
(a)
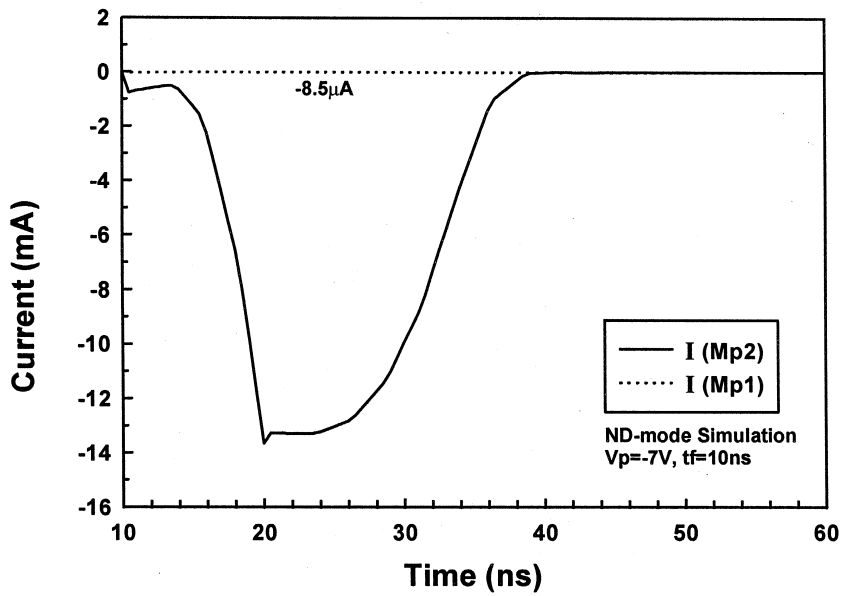
(b)

Fig. 13. (a) The transient voltages on the gates of the output Mp1 and the unused Mp2 and (b) the discharging currents through the output Mp1 and the unused Mp2, during the ND-mode simulation on the 2-mA output buffer with the dynamic-floating-gate design.

MC1, which provides a larger capacitance, leads to a longer turn-on time on the Mn2. Because the turn-on time of Mn2 is linearly dependent on the device dimensions of the MR1 and MC1, it is easy to adjust the turn-on time of Mn2 for different applications by simply changing the device dimensions in the cell layout.

### 3.3.2. ND-mode ESD-stress conduction

The turn-on behavior of a 2-mA output buffer with dynamic-floating-gate design in the ND-mode ESD-stress condition is also simulated by *HSPICE*. An ESD-like ramp voltage with a pulse height of −7 V and a fall time of 10 ns is applied to the output pad of Fig. 9 to simulate the falling edge of the ND-mode ESD voltage, while the VDD is relatively grounded but the VSS is floating. The simulated gate voltages and the drain currents on the output Mp1 and the unused Mp2 are shown in Fig. 13(a) and (b), respectively. The coupled voltage on the gate of Mp1 in Fig. 13(a) is the same as that in Fig. 8(a), but the gate voltage of Mp2 in Fig. 13(a) is quite different to that in Fig. 8(a). The coupled gate voltage in Fig. 13(a) has a peak value of −1.2 V but that in Fig. 8(a) is only −0.27 V. The dynamic-floating-gate design causes the main difference on the coupled gate voltage of Mp2 in the output buffer. As compared to the simulation results in Fig. 8(b), the Mp2 in the output buffer with the dynamic-floating-gate design has a significant drain current during the ND-mode simulation in Fig. 13(b). Such simulation results have theoretically verified that the dynamic-floating-gate design can really hold the coupled voltage on the gate of Mp2 to quickly turn on the Mp2 during the ND-mode ESD stress. Due to the large device dimension of Mp2, the Mp2 can sustain much higher ESD voltage than the output Mp1. By using this dynamic-floating-gate design, the Mp2 can be turned on in time to bypass ESD current before the Mp1 is damaged by the ESD voltage. Therefore, the ESD level of the small-driving output buffer can be significantly improved by the Mp2 with the dynamic-floating-gate design.

The turn-on time of Mp2 is defined as the time period when the negative coupled voltage on the gate of Mp2 is lower than its threshold voltage of −0.75 V. In Fig. 13(a), the turn-on time of Mp2 due to the triggering of the ND-mode simulation with a pulse voltage of −7 V is about 20.5 ns. A larger ESD voltage on the pad couples more voltage to the gate of Mp2 and causes a longer turn-on time on the Mp2. The turn-on time of Mp2 can be also adjusted by changing the device dimensions of the MR2 and MC2 to modify the *RC* time constant in the dynamic-floating-gate design. The simulation results on the turn-on time of Mp2 by
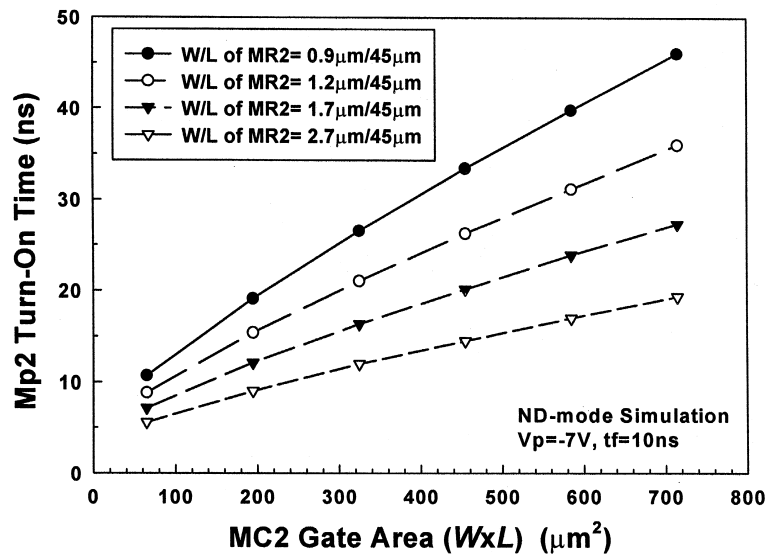
changing the channel length and width of MR2 with a fixed W/L of 65/8 (μm/μm) in the MC2 are shown in Fig. 14(a). The dependence of the turn-on time of Mp2 on the gate area (W × L) of MC2 due to the −7 V ND-mode triggering is shown in Fig. 14(b) under different device dimensions of MR2. As shown in Fig. 14(a) and (b), the turn-on time of Mp2 is linearly dependent on the channel length of MR2 and the gate area of the MC2. The MR2 with a narrower channel width has a higher resistance to cause a longer turn-on time on the Mp2. The turn-on time of Mp2 is linearly dependent on the device dimensions of the MR2 and MC2, so the turn-on time of Mp2 can be easily adjusted by simply changing the device dimensions of such devices in the cell layout.

3.3.3. Normal-operating tri-state condition

In Fig. 9, the dynamic-floating-gate design is used to impermanently float the gate of Mn2 (Mp2) to hold the transient-coupled voltage on the gate of Mn2 (Mp2) under the ESD-stress conditions, therefore the unused Mn2 (Mp2) can be turned on betimes to bypass the PS-mode (ND-mode) ESD current away from the small-dimension output Mn1 (Mp1). But in the normal operating conditions with the 3.3-V VDD and 0-V VSS biases, the gate of Mdn1 (Mdp1) in Fig. 9 is biased at VDD (VSS) through the turned-on MR1 (MR2). So, the Mdn1 (Mdp1) with a device dimension of 20/0.35 is fully turned on to keep the gate voltage of Mn2 (Mp2) at VSS (VDD). The Mn2 (Mp2) has to be guaranteed off when the output buffer is in the normal operating conditions. In some bi-direction I/O applications, the output buffer may be operated in the tri-state condition, where both the output Mp1 and Mn1 are kept off and the output pin becomes an input pin. Under such a tri-state condition, the input signal with a sharp rising/falling edge on the pad may trigger on the unused Mn2 or Mp2 in the output buffer with the dynamic-floating-gate design. To clearly verify this point, the output buffer in Fig. 9 is also simulated by the *HSPICE* in the tri-state condition. An input voltage waveform with both the rise time and fall time of only 2 nS and the pulse height of 3.3 V is applied to the output pad under the tri-state condition. The coupled voltages on the gates of Mn2 and Mp2 are monitored and shown in Fig. 15. The coupled gate-to-source voltage of the Mn2 (Mp2) due to the rising-edge triggering from the input signal is only 11 mV (−84 mV), whereas the coupled gate-to-source voltage of the Mn2 (Mp2) due to the falling-edge triggering is only −11 mV (85 mV). Such coupled gate-to-source voltage on the Mn2 (Mp2) is much smaller than its threshold voltage, so the Mn2 (Mp2)
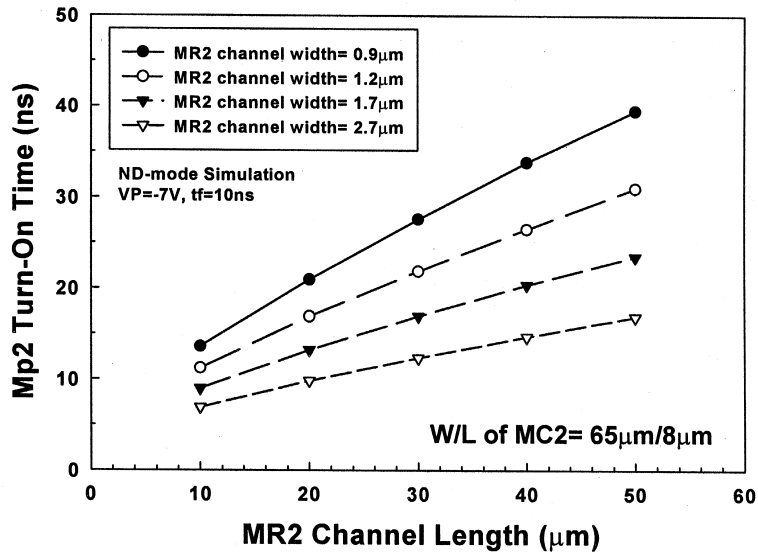
(a)

(b)

Fig. 14. The simulation results on the variation of the turn-on time in Mp2 by (a) changing the channel length and width of MR2 with a fixed W/L of 65/8 (μm/μm) in the MC2 and (b) changing the gate area (W × L) of MC2 under different W/L of MR2, during the ND-mode simulation on the 2-mA output buffer with the dynamic-floating-gate design.

is guaranteed off in the tri-state condition. Moreover, the overshooting (undershooting) voltage pulse attached to the pad can be clamped by the parasitic drain diode Dp2 (Dn2) in the Mp2 (Mn2), when the output buffer is in the normal operating conditions.

Thus, the Mn2 (Mp2) in the output buffer with the dynamic-floating-gate design is not triggered on by the sharply rising or falling voltage waveforms on the pad. This dynamic-floating-gate design on the output buffer does not destroy the output function at all, but it
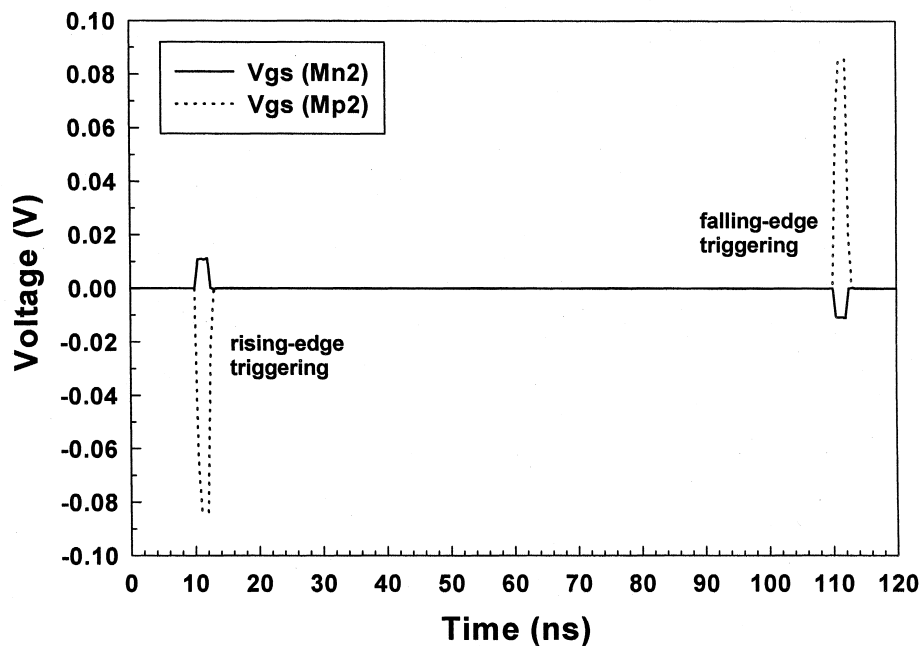
Fig. 15. The simulated gate-to-source voltages of the Mn2 and Mp2 in Fig. 9 due to the triggering of a voltage pulse attached to the output pad with a rise/fall time of 2 ns and a pulse height of 3.3 V when the output buffer is operating in the tri-state condition.

can effectively improve ESD robustness of the output buffer.

4. Experimental results

The output buffers with the dynamic-floating-gate design have been designed and fabricated in a 0.35-μm SPQM CMOS process. The human-body-model (HBM) ESD test results of the output buffers in Fig. 5 with the traditional gate-coupled design has been listed in Table 1. For an output buffer with a higher driving/sinking current, the Mn1 and Mp1 in the output buffer have larger device dimensions, which can sustain higher ESD stress. So, the output buffer in Table 1 with higher driving/sinking current has a higher ESD level. The HBM ESD test results of the output buffers in Fig. 9 with the proposed dynamic-floating-gate de-

sign are listed in Table 2. The Mn1, Mp1, Mn2 and Mp2 devices in both the output buffers of Figs. 5 and 9 have the same modified ESD-implanted drain region and silicide-blocking diffusion. The HBM ND-mode (PS-mode) ESD level of the 2-mA output buffer with the traditional gate-coupled design in Fig. 5 is only 1.5 kV (1.0 kV). But, the HBM ND-mode (PS-mode) ESD level of the 2-mA output buffer with the same device dimensions can be improved greater than 8 kV (8 kV) by using the dynamic-floating-gate design. In Table 2, the dynamic-floating-gate design is not used in the output buffers with the driving/sinking current greater than 12 mA, because the device dimension of the output Mn1 (Mp1) is greater than that of the unused Mn2 (Mp2). With a current specification greater than 12 mA, the Mn1 (Mp1) has a device dimension greater than 240/0.5 (360/0.5), which can sustain the HBM ESD level of greater than 8 kV under the help of the

Table 2
The human-body-model (HBM) ESD level of the output buffer protected by the proposed dynamic-floating-gate design (Fig. 9)

HBM ESD stress	Output buffers (kV)				
	2-mA buffer	4-mA buffer	8-mA buffer	12-mA buffer	24-mA buffer
ND-Mode	> 8	> 8	> 8	> 8	> 8
PS-Mode	> 8	> 8	> 8	> 8	> 8

Table 3
The machine-model (MM) ESD level of the 2-mA output buffer

MM ESD stress	Output buffers (V)	
	2-mA buffer with traditional gate-coupled design (Fig. 5)	2-mA buffer with dynamic-floating-gate design (Fig. 9)
ND-Mode	150	1600
PS-Mode	100	1500

modified ESD-implant process and the silicided-blocking diffusion.

The machine-model (MM) ESD test results of the 2-mA output buffers between the designs in Figs. 5 and 9 are compared in Table 3. The 2-mA output buffer with the traditional gate-coupled design in Fig. 5 can sustain the MM PS-mode (ND-mode) ESD level of only 100 V (150 V), but the 2-mA output buffer with the dynamic-floating-gate design in Fig. 9 can pass the MM ESD stress of 1500 V. These ESD test results have further verified the effectiveness of the proposed dynamic-floating-gate design to improve the ESD robustness of the output buffer with a small-dimension output Mn1 (Mp1) but a large-dimension unused Mn2 (Mp2).

The output buffers with the dynamic-floating-gate design are also tested by the field-induced charged-device-model (CDM) ESD stress. Such output buffers with different driving specifications from 2 mA to 24 mA in the 0.35-μm CMOS process can sustain the field-induced CDM ESD voltage of greater than 4 kV.

5. Conclusion

A dynamic-floating-gate design has been successfully used to improve ESD level of the small-driving output buffers. The gates of the unused NMOS/PMOS in the output buffers are dynamically floated during the ESD stress, so the unused NMOS/PMOS with large device dimensions can be instantaneously turned on to bypass the ESD current. The theoretical principles and the operating mechanism of the dynamic-floating-gate design to improve ESD robustness of the output buffer have been explained in details and verified by *HSPICE* simulation. The turn-on time of the unused NMOS/PMOS in the output buffer can be linearly adjusted by changing the device dimensions in the dynamic-floating-gate circuit. By using the proposed dynamic-floating-gate design, the HBM ND-mode (PS-mode) ESD level of the 2-mA output buffer in a 0.35-μm CMOS process has been significantly improved from the original 1.5 kV (1.0 kV) up to greater than 8 kV. The MM ND-mode (PS-mode) ESD level of the 2-mA output buffer has been also effectively improved from the original 150 V (100 V) up to greater than 1500 V. This dynamic-floating-gate design has been practically used in TSMC 0.35-μm and 0.25-μm CMOS cell libraries to service the ASIC's which are manufactured in TSMC.

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