The effect of native oxide on epitaxial SiGe from deposited amorphous Ge on Si

Y. H. Wu, W. J. Chen, Albert Chin, and C. Tsai

The effect of native oxide on epitaxial SiGe from deposited amorphous Ge on Si

Y. H. Wu

Department of Electronics Eng., National Chiao Tung University, Hsinchu, Taiwan

W. J. Chen

Department of Mechanical Materials Eng., National Huwei Institute of Technology, Huwei, Taiwan

Albert Chin[a)] and C. Tsai

Department of Electronics Eng., National Chiao Tung University, Hsinchu, Taiwan

We have investigated the effect of native oxide on the epitaxial SiGe from deposited amorphous Ge on Si. Instead of epitaxial growth by molecular beam epitaxy or ultrahigh-vacuum chemical vapor deposition, the SiGe layer is formed by this simple process followed by an annealing step. As observed by transmission electron microscopy, the suppression of native oxide plays an important role to achieve epitaxial SiGe. The SiGe quality degrades with increasing native oxide thickness and becomes polycrystalline with a ~ 20 Å interfacial native oxide. On the other hand, single crystalline SiGe can be routinely formed from a HF-vapor treated Si surface. © *1999 American Institute of Physics.* [S0003-6951(99)04504-0]

SiGe alloys have been found to be a very attractive material to fabricate high-speed devices and optoelectronic devices.[1–3] Besides applications in heterojunction bipolar transistors (HBTs), modulation doped field effect transistors (MODFETs), and thin film transistors (TFTs), SiGe material can also be used to improve the complementary metal-oxide-semiconductor (CMOS) device performance,[4] to suppress the floating-body effect in Si-on-insulator (SOI) metal-oxide-semiconductor FET (MOSFETs),[5] or as an etch stop layer in bond and etch-back SOI (BESOI) process. In general, the SiGe/Si heterojunction can be grown by molecular beam epitaxy (MBE)[3] or ultrahigh vacuum chemical vapor deposition (UHVCVD).[6] These techniques provide high-quality heterostructures, but require extremely rigorous control of many process parameters. However, epitaxial SiGe can be also formed by Ge ion implantation followed by an annealing step,[7] or wet oxidation of deposited amorphous Si_xGe_{1-x} layer.[8] In this work, we present a different approach to form single crystalline SiGe from deposited amorphous Ge on Si followed by an annealing step. This method is very simple and compatible to the existing very large scale integrated (VLSI) technology. We have found that the key factor to form the desired epitaxial SiGe, instead of the polycrystalline one, is the suppression of native oxide. We have used HF-vapor passivation to suppress the native oxide formation before depositing the Ge layer. Similar process technique has been applied to low-temperature Si epitaxy[9] and thermal oxide growth with an atomically smooth interface.[10,11] As observed by both x-ray diffraction and transmission electron microscopy (TEM), increasing native oxide thickness degrades the SiGe crystalline quality and single crystalline SiGe can be routinely formed with a HF-vapor treated surface.

Four-inch, *p*-type (100) Si wafers were used in this work with a resistivity of 10 Ω cm. Before loading into a standard electron beam evaporator to deposit Ge, with a background pressure of 2×10^{-6} Torr, the Si substrates were treated with different process steps to study the effect of native oxide. Si wafers, which were RCA cleaned, dipped in a buffered HF solution, rinsed in deionized water, spun dry in nitrogen, and followed by immediately loading into the evaporator, are identified as control samples. The measured native oxide thickness is $5\sim 7$ Å. Another set of wafers is the same as control samples but with additional HF-vapor treatment just before loading into the evaporator. The HF-vapor is generated from the equilibrium vapor pressure of HF and water mixture (HF:$H_2O=1:1$) in a plastic beaker. To study the thickness dependence of native oxide on SiGe quality, we have chemically grown a thick Shiraki oxide. This set of wafers is identical to control samples but with the submergence in a boiling HCl:H_2O_2:$H_2O=3:1:1$ solution for 5 min to grow a ~ 20 Å Shiraki oxide before Ge deposition. The above method was successfully used to form $CoSi_2$ on Si and was referred as oxide mediate epitaxy (OME).[12] Ge thin film was then evaporated to a thickness of 250 Å with a deposition rate of 1 Å/s at room temperature. Then the samples were annealed at 900 °C by rapid thermal annealing (RTA) for 60 s to form a SiGe layer. We have used x-ray diffraction, electron diffraction, and TEM to examine the SiGe layer quality.

Figure 1 presents the x-ray diffraction spectra of SiGe layers with different surface treatments before Ge deposition. The SiGe layer with HF-vapor pretreatment shows strong and sharp diffracted peak that indicates a single crystalline behavior with a calculated Ge composition of 70% in SiGe alloys. The SiGe layer without HF-vapor pretreatment shows a weaker and broader diffracted peak that indicates the crystal structure is highly defective. This may be due to the pres-

---

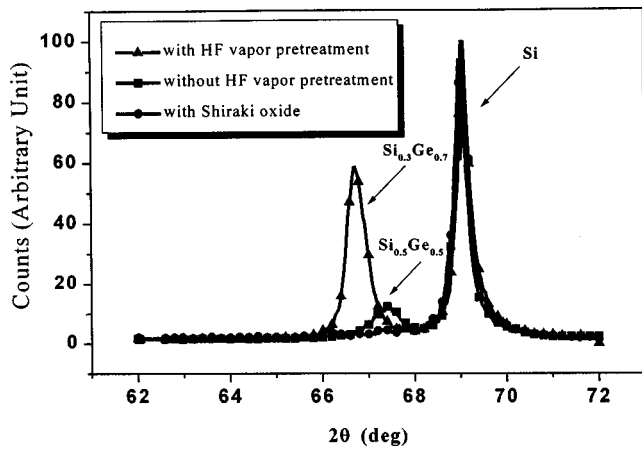a)Electronic mail: achin@cc.nctu.edu.tw

FIG. 1. X-ray diffraction spectra of SiGe layers with different surface treatments before Ge deposition.

(a)

(b)

FIG. 2. Electron diffraction pattern of SiGe layers formed (a) with the presence of Shiraki oxide and taken along the $\langle 001 \rangle$ zone axis (b) with HF-vapor pretreatment and taken along $\langle 011 \rangle$ zone axis.

ence of $5 \sim 7$ Å native oxide. The effect of native oxide on SiGe structure quality can be further understood from the thick chemically grown Shiraki oxide. The signal of SiGe layer with this Shiraki oxide shows a very weak signal that indicates either a polycrystalline structure or no SiGe formation. The Ge and Si interdiffusion may be blocked by this thick oxide. Therefore we have further increased the interdiffusion by increasing the annealing temperature to 1000 °C, but still very weak x-ray diffraction signal is measured. These results suggest that a random polycrystalline or amorphous structure may be responsible to the extremely weak x-ray diffraction signal.

We have further investigated the crystalline structure by using electron diffraction pattern. Figures 2(a) and 2(b) are the electron diffraction pattern of SiGe layers formed with the presence of Shiraki oxide and HF-vapor pretreatment, respectively. The ring pattern in Fig. 2(a) verifies that the extremely weak x-ray diffraction in Fig. 1 appears to be polycrystalline SiGe. Therefore, the existence of Shiraki oxide will strongly degrade the SiGe crystalline quality. In strong contrast, single crystalline electron diffraction pattern is obtained from the highly oriented diffraction pattern in Fig. 2(b) with HF-vapor treatment. This single crystalline behavior is consistent with the sharp and strong x-ray diffraction in Fig. 1.

We have also examined the SiGe layer by cross-sectional TEM. Figures 3(a) and 3(b) present the cross-sectional images of SiGe with or without the HF-vapor pretreatment, respectively. The TEM images show that almost all the deposited Ge materials are transformed into SiGe. The SiGe layer formed without HF-vapor treatment is highly defective, and twins, facet, and dislocations are observed in the SiGe layer. On the contrary, these defects are much reduced in the HF-vapor pretreated sample. This result is consistent with the single crystalline behavior observed in electron diffraction and x-ray diffraction spectra. Therefore, the HF-vapor treatment is of paramount importance to form high quality epitaxial SiGe layer. It is believed that the surface with additional HF-vapor treatment has better H or F termination and is more resistant to native oxide growth than that dipped in HF solution. As native oxide grows thicker, the surface roughness increases, which is confirmed by atomic
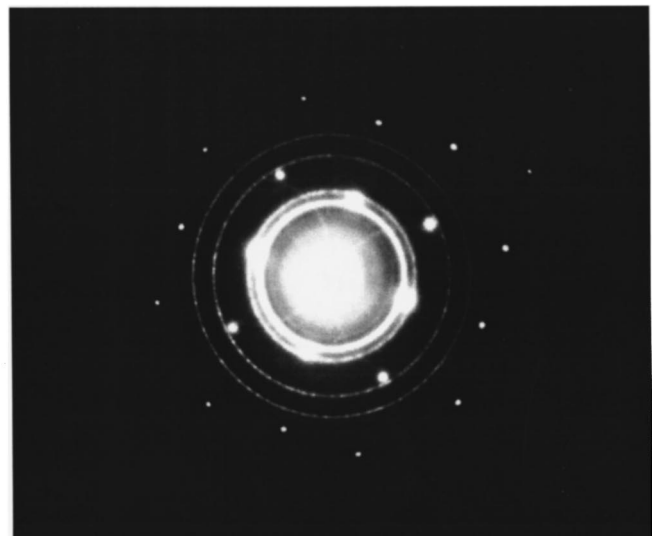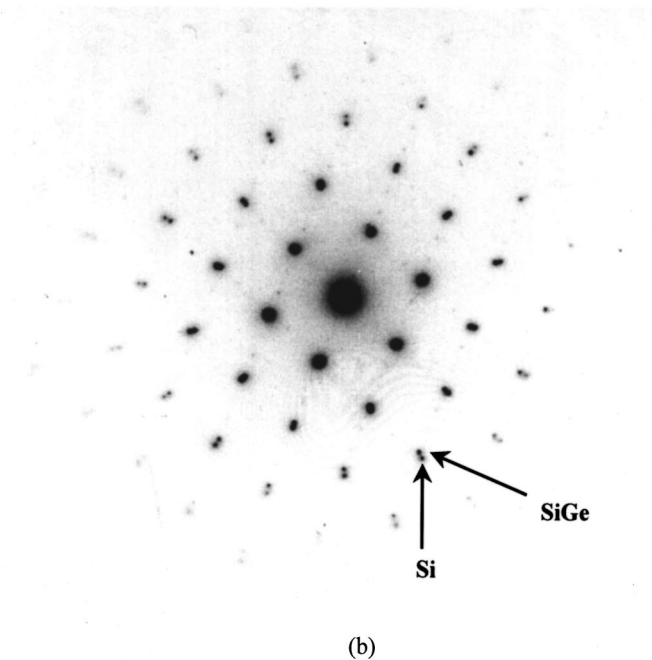
force microscopy (AFM) measurement. The HF-vapor treatment can improve surface root mean square (rms) roughness from standard 3.0 Å to only 1.5 Å. Owing to a cleaner surface, Ge atoms can directly contact the underlying Si lattice and form epitaxial SiGe.

We have measured the secondary ion mass spectroscopy (SIMS) profiles to further understand the formation of SiGe. Figures 4(a) and 4(b) present the SIMS profiles of samples with Shiraki oxide and HF-vapor treatment, respectively. The sample with Shiraki oxide shows a typical Ge diffusion profile. Therefore diffusion alone cannot form single crystalline SiGe. In sharp contrast, a uniform SiGe layer is formed on HF-vapor treated sample that may explain the very sharp SiGe peak in x-ray diffraction spectra. Beyond this region, Si and Ge interdiffusion is observed, while this interdiffusion may be enhanced by defect density, strain, and the high Ge
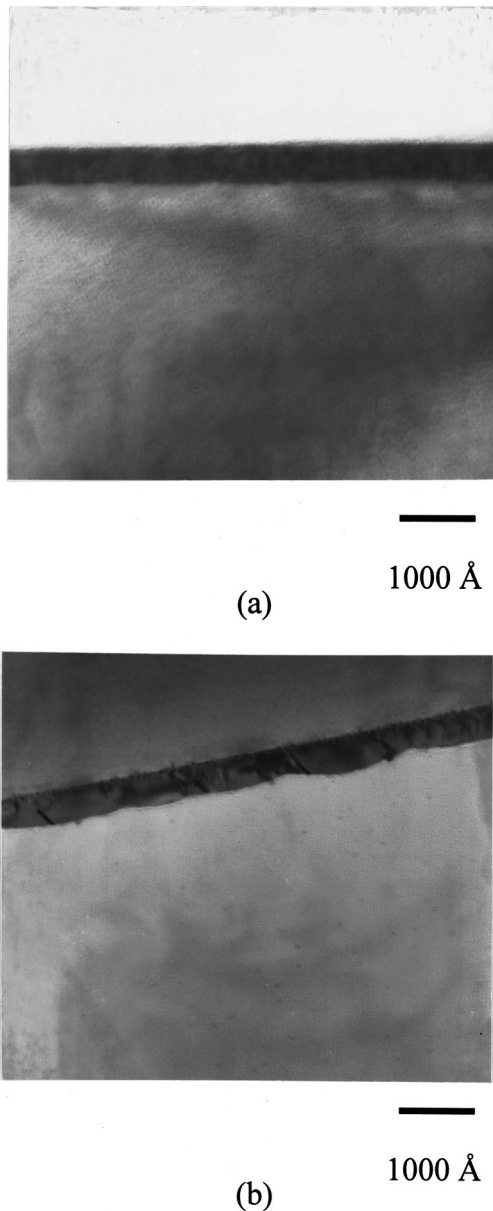
(a)

1000 Å

(a)

(b)

1000 Å

(b)

(b)

FIG. 4. SIMS depth profiles for sample (a) with Shiraki oxide mediated (b) with HF vapor pretreatment.

FIG. 3. Cross-sectional TEM images of SiGe (a) with (b) without the HF-vapor pretreatment.

concentration.[13] Because interdiffusion may be difficult to explain this thick and uniform SiGe layer, possible mechanism may be due to the solid phase epitaxy (SPE) that is very fast and is also responsible to $CoSi_2$ formation. The strong dependence of SiGe quality on interface oxide also suggests that the SPE process may be responsible to epitaxial SiGe from direct contact of Ge and Si. In fact, both SPE and diffusion are the required mechanisms to form $CoSi_2$.[12,14]

In conclusion, we have shown that single crystalline SiGe can be achieved by simple deposited amorphous Ge on Si. Our results reveal that the interfacial condition plays an important role to form epitaxial SiGe, and the SiGe quality is degraded with increasing native oxide thickness. Single crystalline SiGe can be routinely formed with HF-vapor treatment to passivate Si surface from oxidation. By using HF-vapor treatment, we can form SiGe with much simple and inexpensive ways, which is also compatible to the existing VLSI technology.
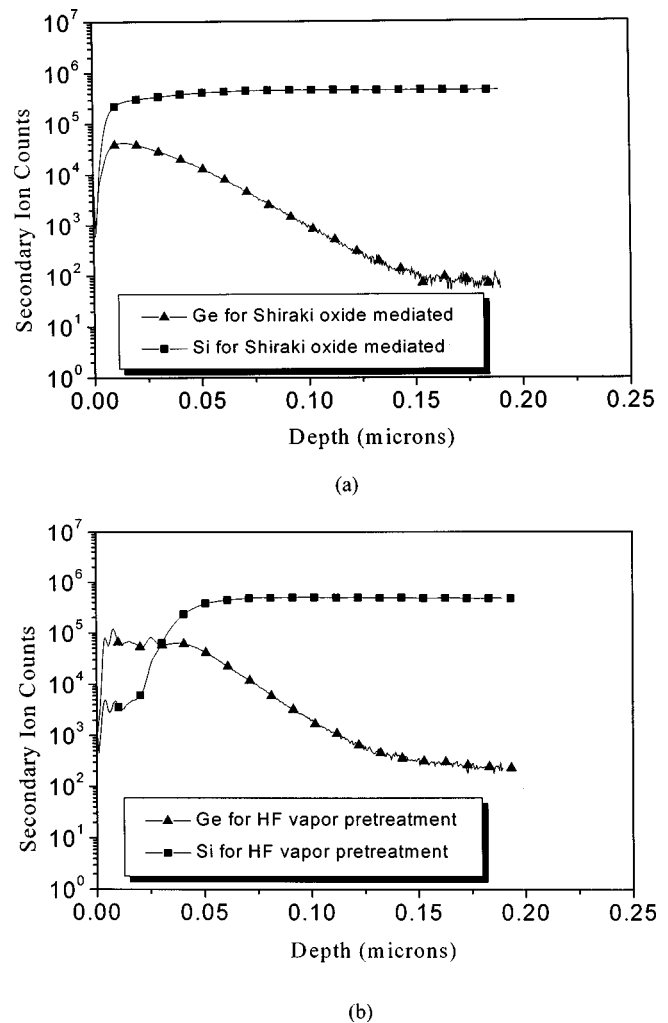
[1] S. S. Lyer, G. L. Patton, J. M. C. Stork, B. S. Meyerson, and D. L. Harame, IEEE Trans. Electron Devices **36**, 2043 (1989).

[2] A. J. Tang, J. A. Tsai, R. Reif, and T. J. King, Tech. Dig. Int. Electron Devices Meet., 513 (1995).

[3] F. Y. Huang, S. G. Thomas, M. Chu, K. L. Wang, and N. D. Theodore, Tech. Dig. Int. Electron Devices Meet., 665 (1996).

[4] N. Kistler and J. Woo, Tech. Dig. Int. Electron Devices Meet., 727 (1993).

[5] M. Yoshimi, M. Terauchi, A. Nishiyama, O. Arisumi, A. Murakoshi, K. Matsuzawa, N. Shigyo, S. Takeno, M. Tomita, K. Suzuki, Y. Ushiku, and H. Tango, IEEE Trans. Electron Devices **44**, 423 (1997).

[6] P. J. Wang, F. F. Fang, B. S. Meyerson, J. Nocera, and B. Parker, Appl. Phys. Lett. **54**, 2701 (1989).

[7] L. Xiang and N. W. Cheung, Appl. Phys. Lett. **69**, 1915 (1996).

[8] S. M. Prokes and A. K. Rai, Appl. Phys. Lett. **60**, 568 (1992).

[9] A. Chin, B. C. Lin, and W. J. Chen, Appl. Phys. Lett. **69**, 1617 (1996).

[10] A. Chin, W. J. Chen, T. Chang, R. H. Kao, B. C. Lin, C. Tsai, and J. C-M. Huang, IEEE Electron Device Lett. **18**, 417 (1997).

[11] A. Chin, B. C. Lin, W. J. Chen, Y. B. Lin, and C. Tsai, IEEE Electron Device Lett. , (1998).

[12] R. T. Tung, Appl. Phys. Lett. **68**, 3461 (1996).

[13] F. K. LeGoues, S. S. Iyer, K. N. Tu, and S. L. Delage, Mater. Res. Soc. Symp. Proc. **103**, 185 (1988).

[14] C. M. Comrie and R. T. Newman, J. Appl. Phys. **79**, 153 (1996).