# Series Resistance of Self-Aligned Silicided Source/Drain Structure

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***Abstract*—The external resistance of the self-aligned silicided source/drain structure is examined by two-dimensional simulation considering recession of the contact interface due to the consumption of silicon during the silicidation process. It is observed that the recessed contact interface forces a significant amount of current to flow into the high-resistivity part of the junction resulting in an increase of resistance as large as several hundred ohms-micrometers in comparison with the surface contact structure. The increase scales up with the scale-down of the minimum feature size, and the expected benefits of the SALICIDE structure become diminished for the sub-half-micrometer devices. A simple analytical explanation is proposed. The error between the analytical calculation and the two-dimensional simulation is within 20%. By considering the recession of the contact interface, the reported high external resistance of the short-channel MOSFET's is explained successfully. Different source/drain contact types are compared, and it is concluded that the conventional SALICIDE process should be modified for the sub-half-micrometer devices.**

## Nomenclature

$A_c$ Area of contact window ($\mu$m$^2$).
$C_b$ Substrate concentration (cm$^{-3}$).
$C_s$ Surface concentration of source/drain junction (cm$^{-3}$).
$C_{s+}$ Surface concentration of heavily doped region (cm$^{-3}$).
$C_{s-}$ Surface concentration of lightly doped region (cm$^{-3}$).
$I_t$ Total current flowing into the contact window (Fig. 2), (A).
$L_c$ Contact length (Fig. 2) ($\mu$m).
$L_{sp}$ Thickness of sidewall spacer (Fig. 2) ($\mu$m).
$L_t$ Transfer length (5) ($\mu$m).
$m_j$ Depth of contact interface (Fig. 2) (Å).
$R_{ac}$ Accumulation layer resistance (Fig. 1) ($\Omega \cdot \mu$m).
$R_c$ Contact resistance ($\Omega \cdot \mu$m).
$R_{ch}$ Channel resistance (Fig. 1) ($\Omega \cdot \mu$m).
$R_{c,sw}$ Contact resistance of sidewall contact interface (Fig. 9) ($\Omega \cdot \mu$m).
$R_{cw}$ Crowding resistance (Fig. 1) ($\Omega \cdot \mu$m).
$R_{ext}$ External resistance of source/drain (Fig. 1) ($\Omega \cdot \mu$m).
$R_f$ Front resistance ($\Omega \cdot \mu$m).
$R_{f,uc}$ Front resistance under the recessed contact interface (Fig. 9) ($\Omega \cdot \mu$m).
$R_{int}$ Internal resistance (Fig. 1) ($\Omega \cdot \mu$m).
$R_{lt}$ Lateral resistance (Fig. 7) ($\Omega \cdot \mu$m).
$R'_{lt}$ Un-normalized lateral resistance ($\Omega$).
$R_{sh}$ Sheet resistance ($\Omega/\square$).
$R_{si}$ Resistance under sidewall spacer (Fig. 1) ($\Omega \cdot \mu$m).
$R_{sh,uc}$ Sheet resistance of the doped Si under the contact interface ($\Omega/\square$).
$R_{sp}$ Spreading resistance (Fig. 1) ($\Omega \cdot \mu$m).
$R_{sx}$ Resistance between sidewall spacer and contact (Fig. 1) ($\Omega \cdot \mu$m).
$R_t$ Total resistance of source/drain (Fig. 1) ($\Omega \cdot \mu$m).
$V_d$ Potential of contact surface (Fig. 2) (V).
$V_{sp}$ Average potential at the spacer edge (V).
$W_c$ Contact width (Fig. 2) ($\mu$m).
$W_{ld}$ Lateral diffusion beyond contact width (Fig. 7) ($\mu$m).
$x_j$ Junction depth ($\mu$m).
$x_{j+}$ Junction depth of heavily doped region (Fig. 2) ($\mu$m).
$x_{j-}$ Junction depth of lightly doped region (Fig. 2) ($\mu$m).
$\delta$ Spacing between sidewall spacer and contact (Fig. 2) ($\mu$m).
$\rho_c$ Specific contact resistance ($\Omega \cdot$ cm$^2$).

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## I. Introduction

With the progress of very-large-scale integrated (VLSI) technology, the minimum feature size has scaled to submicrometer dimensions for higher performance and density. Since the MOSFET channel resistance ($R_{ch}$) decreases with the channel length, the $R_{ch}$ will be on the order of several hundred ohms for the sub-half-micrometer MOSFETs with a channel width of 1 $\mu$m. For such a short-channel device, a small parasitic resistance would substantially degrade the device and circuit performance [1]–[6]. The total resistance of an LDD-structure MOSFET includes the intrinsic channel resistance ($R_{ch}$), the internal source/drain resistance ($R_{int}$), and

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the external source/drain resistance ($R_{ext}$) as shown in Fig. 1. The $R_{int}$ can be modulated by the gate and S/D voltages and is partitioned into three components: the accumulation resistance ($R_{ac}$), the spreading resistance ($R_{sp}$) [3]–[5], and the resistance under the sidewall spacer ($R_{si}$). Recent analyses indicate that to minimize the $R_{int}$, a steep junction profile is necessary [4], [5]. Although a tradeoff between the $R_{int}$ and the hot-carrier effect exists, recent quarter-micrometer MOSFET's with conventional heavily doped S/D junctions (without lightly doped regions) show adequate resistance to hot-carrier degradation for 2.5-V operation [7]. Advanced LDD structures embedding a lightly doped region underneath the gate can also reduce the $R_{int}$ effectively [8]–[12].

On the other hand, many efforts have been made to minimize the $R_{ext}$. The $R_{ext}$ consists of the metal resistance, the metal/silicon contact resistance ($R_c$), the current-crowding resistance under the contact interface ($R_{cw}$), and the resistance between the spacer and the contact ($R_{sx}$) [5]. The resistance of the metal is negligible. The $R_{sx}$ due to the reduction of the S/D junction depth ($x_j$) and the $R_c$ due to the miniaturization of the contact window area ($A_c$) are scaled-up with the scale-down of the minimum feature size. Early studies on the scaling of $x_j$ predicted that the sheet resistance of the S/D junction is proportional to $(1/x_j)^n$, where $n$ is 5 for a boron-doped junction and 10 for an arsenic-doped junction [13], [14]. This has brought about an unacceptably high resistance for the sub-half-micrometer devices. Newly developed shallow junction technologies have overcome this problem [15]–[18]. Shallow junctions with $x_j$ less than 0.1 $\mu$m and sheet resistance lower than 200 $\Omega/\square$ have been obtained for both $n^+/p$ and $p^+/n$ junctions [19]. In 1981, Shibata *et al.* proposed a self-aligned silicided S/D structure (SALICIDE) to reduce the $R_{ext}$ [20]. It is expected that the $R_{sx}$ can be reduced to a negligible level by the shunted silicide layer, and the $R_c$ and $R_{cw}$ can be also reduced due to the fact that the $A_c$ is now extended to be as large as the S/D area. The contact resistivity between the contact metal and silicide is on the order of $1 \times 10^{-8}$ $\Omega \cdot cm^2$ and is negligible. In 1982, Scott *et al.* analyzed the impact of the SALICIDE structure on the performance of VLSI circuits using a transmission line model and predicted that the circuit performance can be improved by a factor of 2 for NMOSFET's and 10 for PMOSFET's [13]. In the past ten years, the SALICIDE technology and the silicides suitable for the SALICIDE structure have attracted a lot of attention [21]. PtSi [20], $TiSi_2$ [22], and $CoSi_2$ [23] have been successfully employed to implement the SALICIDE structure. Although the device performance is improved, the extent of improvement is not as great as that predicted in [13]. Recent studies have indicated that the $R_{sx}$ only makes a small contribution to the $R_{ext}$ even for the non-SALICIDE structure because the spacing between contact and gate scales nearly linearly with the minimum feature size [5]. The main advantage of the SALICIDE structure is thus not to eliminate the $R_{sx}$, but to increase the $A_c$ such that the $R_c$ is reduced. The benefit of the SALICIDE structure is not in doubt. The only drawback is that the allowable thickness of the silicide film over the S/D junction decreases with the reduction of the $x_j$. This seems to contradict the requirement of low sheet resistance of interconnection lines [23].

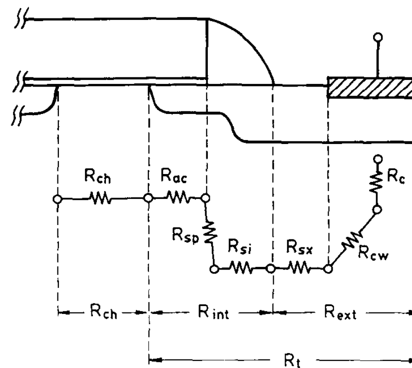


Fig. 1. Cross section of a typical MOSFET showing series resistance components.

In the authors' recent study on the accuracy of the measured contact resistivity ($\rho_c$) of the silicide/silicon interface formed by direct reaction of metal with silicon, it is observed that the measured value will be lower than the true value when the cross-bridge Kelvin-resistor structure is employed [24]. It is explained by the three-dimensional current distribution due to the four additional sidewall contact interfaces. An increase in the front resistance ($R_f$) is also observed in the three-dimensional simulation. This implies that the $R_{ext}$ may increase with the increase of silicide recession into the S/D junction even if the $\rho_c$ value remains constant. In this work, the authors study the impact of the recession of silicide on the $R_{ext}$ by numerical simulation. The results conclude that the $R_{ext}$ may increase with the recession of silicide to an extent of several hundred ohms-micrometers. This drawback compromises the benefit of larger contact area. The simulation structure is described in the next section. The influences of the recession of the contact interface on $R_{ext}$ are presented in Section III and a simple analytical explanation is given in Section IV. In Section V, the measured $R_{ext}$ data reported in two published papers are examined by taking the recession of contact interface into consideration. It is observed that the increase in $R_{ext}$ plays an important role in the S/D resistance. In Section VI, four S/D contact types including self-aligned and non-self-aligned contacts with and without recession of the contact interface are compared in brief. This is followed by the conclusions in Section VII.

## II. Simulation Structure

Since there is no current component which is transverse to the direction of the channel, a two-dimensional simulation is adequate for modeling the drain structure. Fig. 2(a) and (b) shows the top view and cross-sectional view, respectively, of the simulation structure. A box profile is

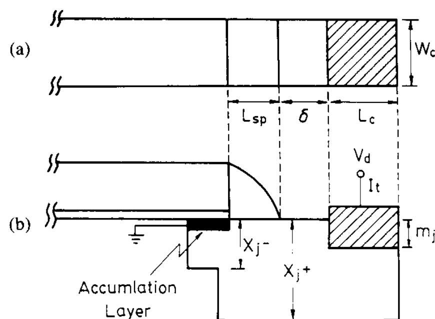


Fig. 2. (a) Top view and (b) cross-sectional view of the structure used for 2D simulation.

used for the junction, though a more realistic metallurgical junction should be rounded. In Section III-A, we will give an explanation that the simplified box profile is not expected to affect the accuracy of the simulation results. In the structure, $L_{sp}$ is the thickness of the sidewall spacer, and $\delta$ is the spacing between contact and spacer edge. For a SALICIDE contact, $\delta = 0$. The contact length and width are $L_c$ and $W_c$, respectively. The resistances mentioned hereafter are all normalized to $W_c$ and the unit is $(\Omega \cdot \mu\text{m})$. The light doping implantation is self-aligned to the gate edge and the heavy doping implantation is self-aligned to the spacer edge. The junction depths of the lightly doped region and the heavily doped region are denoted by $x_{j-}$ and $x_{j+}$, respectively. The doping profile is estimated by the Gaussian distribution of $C(x) = C_s \times \exp(-x^2/k)$, where $C_s$ is the surface concentration and $k$ is a constant. The signs of $C_{s-}$ and $C_{s+}$ are used to represent the surface concentration of the lightly doped and the heavily doped regions, respectively. The lateral diffusion is assumed to be 70% of the vertical junction depth. By adjusting the combination of $x_{j-}$, $x_{j+}$, $C_{s-}$, and $C_{s+}$, LDD and conventional structures can be generated. The doping concentration of the accumulation layer underneath the gate is assumed to be $C_{s+}$ and the thickness of this layer is 100 Å; no voltage modulation effect of both quantities is assumed. In fact, the lateral junction profile and its conduction property only affect the $R_{\text{int}}$ but not the $R_{\text{ext}}$, which is of interest in this work. The metal junction depth $(m_j)$ is defined as the depth of silicon consumption during silicidation. Two types of contacts are then defined: the surface contact $(m_j = 0)$ and the recessed contact $(m_j > 0)$.

The structure is represented as a two-dimensional resistor network. The resistivity of the contact metal has little influence on the results and is arbitrarily chosen to be 30 $\mu\Omega \cdot$ cm. The resistivity of the silicon region is calculated through an approximated mobility-concentration relation [25], [26]. The top surface of the contact metal is kept at $V_d$ and the left boundary of the accumulation layer is kept at 0 V. The structure is partitioned nonuniformly into about 1200 units. The overrelaxation method is used to solve this problem with an overrelaxation parameter of $\omega = 1.86$. The convergence criteria are that the maximum relative change of node voltage between two adjacent iterations is less than $1 \times 10^{-7}$ and the relative difference between the input and output currents is less than $1 \times 10^{-3}$. The total S/D resistance is $V_d$ divided by the total current $(I_t)$ flowing into the structure. The front voltage $(V_{sp})$ is calculated by averaging the potential at the spacer edge. The $R_{\text{ext}}$ is thus defined as

$$R_{\text{ext}} = \frac{V_d - V_{sp}}{I_t}. \tag{1}$$

For the SALICIDE structure, the $R_{\text{ext}}$ is just the so-called front resistance $R_f$. The total S/D resistance $(R_t = R_{\text{int}} + R_{\text{ext}})$ is $V_d/I_t$.

## III. Simulated Results

### A. Current Distribution

Fig. 3 shows the current distribution along the direction of the junction depth at positions of the inner contact edge and 700 Å away from that edge toward the channel (halfway to the edge of the lateral diffusion of the heavily doped junction) for a surface contact and a recessed contact with $m_j = 1000$ Å. The main parameters employed in this simulation are as follows: $L_{sp} = 0.2$ $\mu$m, $\delta = 0$, $L_c = 1$ $\mu$m, $W_c = 1$ $\mu$m, $C_{s-} = 1 \times 10^{18}$ cm$^{-3}$, $C_{s+} = 1 \times 10^{20}$ cm$^{-3}$, $x_{j-} = 0.1$ $\mu$m, $x_{j+} = 0.2$ $\mu$m, and $C_b = 1 \times 10^{16}$ cm$^{-3}$, where $C_b$ is the substrate concentration. For the surface contact, most of the current flows in the upper part of the junction at the contact edge and slightly spreads into the lower part of the junction at the position which is 700 Å away from the contact edge. For the recessed contact, the current distribution at the contact edge is quite different from that of the surface contact. Consistent with our previous work [24], a large amount of the total current is pushed to the lower part of the junction by the recessed contact interface. This forces current to flow in the higher resistivity region and through a longer path. In the following subsections, problems resulting from the unexpected current distribution will be examined. The current distribution at the position which is 700 Å away from the contact edge of the recessed contact is very close to that of the surface contact. This implies that the recession of contact interface almost only affects the $R_{\text{ext}}$ but not the $R_{\text{int}}$. Thus the discussions in the following parts of this work are concentrated on the change of total resistance, which is essentially equal to the change of $R_{\text{ext}}$, and the parameters of the lightly doped region become unimportant. As a result, the results and discussions in the following sections are valid for devices both with and without LDD structure. For the recessed contact, once the current leaves the contact edge it flows toward the upper region of the junction resulting in a similar distribution as in the case of surface contact. Furthermore, since only the change of $R_{\text{ext}}$ is of concern to this study, it is believed that the box profile approximation for the junction as shown in Fig. 2 will have very little effect to the result of simulation.

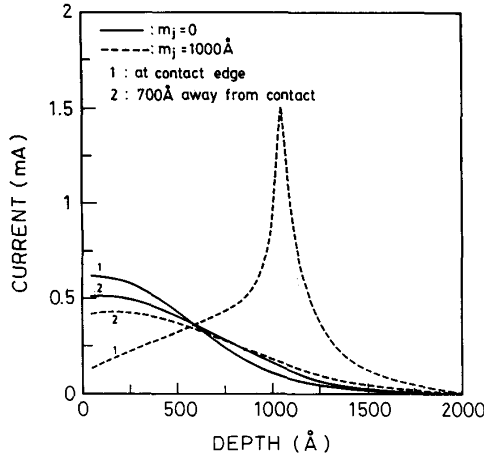


Fig. 3. Current distribution along the direction of junction depth. The main simulation parameters are: $L_{sp} = 0.2$ $\mu$m, $\delta = 0$, $L_c = W_c = 1$ $\mu$m, $x_{j-} = 0.1$ $\mu$m, $x_{j+} = 0.2$ $\mu$m, $C_{s+} = 1 \times 10^{20}$ cm$^{-3}$, $C_{s-} = 1 \times 10^{18}$ cm$^{-3}$, and $C_b = 1 \times 10^{16}$ cm$^{-3}$.

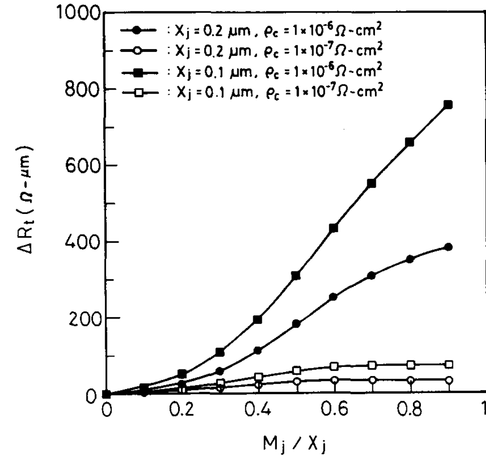


Fig. 4. Change of total resistance ($\Delta R_t$) versus the increase of $m_j/x_{j+}$ ratio. The main simulation parameters are: $L_{sp} = 0.2$ $\mu$m, $\delta = 0$, $L_c = W_c = 1$ $\mu$m, $C_{s+} = 1 \times 10^{20}$ cm$^{-3}$, and $C_b = 1 \times 10^{16}$ cm$^{-3}$.

## B. Metal Junction Depth ($m_j$) Dependence

Fig. 4 shows the change of $R_t$ ($\Delta R_t \approx \Delta R_{ext}$) with the increase of the $m_j/x_{j+}$ ratio. Two junction depths of $x_{j+} = 0.1$ and 0.2 $\mu$m and two $\rho_c$ values of $1 \times 10^{-6}$ and $1 \times 10^{-7}$ $\Omega \cdot$ cm$^2$ are considered in this simulation. The $L_{sp}$ is 0.2 $\mu$m and the $C_{s+}$ and $C_b$ are $1 \times 10^{20}$ and $1 \times 10^{16}$ cm$^{-3}$, respectively. It is observed that $\Delta R_t$ increases monotonically with increasing $m_j/x_{j+}$. In the case of $\rho_c = 1 \times 10^{-6}$ $\Omega \cdot$ cm$^2$, an $m_j = 1000$ Å increases $R_{ext}$ by 180 $\Omega \cdot \mu$m for $x_{j+} = 0.2$ $\mu$m and an $m_j = 500$ Å increases $R_{ext}$ by 300 $\Omega \cdot \mu$m for $x_{j+} = 0.1$ $\mu$m. This phenomenon imposes a challenge to the sub-half-micrometer devices. In those devices the junction depth has been scaled to about 0.1 $\mu$m. The silicide thickness also has been scaled downward. However, as the silicide thickness decreases to 500 Å or less, the sustainable process temperature lowers to 800°C for both $TiSi_2$ and $CoSi_2$ [27]. For these two silicides, a 500-Å thickness results in an $m_j$ of 450 Å and 520 Å for $TiSi_2$ and $CoSi_2$, respectively. The tremendous increase of $R_{ext}$ may outweigh the expected benefits of the SALICIDE structure.

## C. Specific Contact Resistance ($\rho_c$) Dependence

Fig. 5 shows the $\Delta R_t$ versus $\rho_c$ of the recessed contact with $m_j/x_{j+} = 0.5$, where $x_{j+}$ is 0.1 and 0.2 $\mu$m. It is observed that decreasing the $\rho_c$ value can decrease the $\Delta R_t$ effectively. However, since the $R_t$ value also decreases with decreasing $\rho_c$ value, the relative increase of $R_t$, i.e., $\Delta R_t/R_t$, is in fact increased with the decrease of $\rho_c$. In the conventional concept, the SALICIDE contact is treated as a surface contact and the $R_{ext}$ is expected to be insignificant as the $\rho_c$ is lower than $1 \times 10^{-7}$ $\Omega \cdot$ cm$^2$ [5]. When the influence of the contact recession is considered, it is quite different.

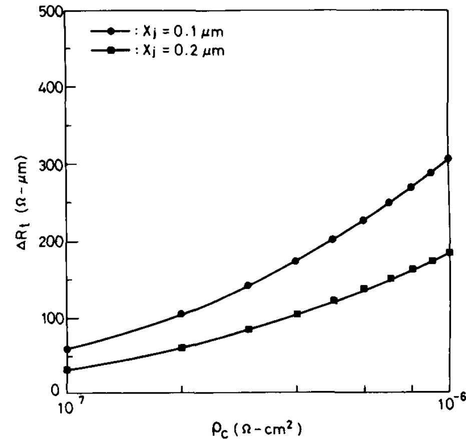


Fig. 5. Change of total resistance ($\Delta R_t$) versus specific contact resistance ($\rho_c$) with $m_j/x_{j+} = 0.5$. The main simulation parameters are: $L_{sp} = 0.2$ $\mu$m, $\delta = 0$, $L_c = W_c = 1$ $\mu$m, $C_{s+} = 1 \times 10^{20}$ cm$^{-3}$, and $C_b = 1 \times 10^{16}$ cm$^{-3}$.

## D. Contact Length ($L_c$) Dependence

Fig. 6 shows the $R_t$ versus $L_c$. In this simulation, the S/D structure is assumed to be the conventional heavily doped structure. The S/D implantation is self-aligned to the gate edge with $L_{sp} = 0.2$ $\mu$m and $C_{s+} = 1 \times 10^{20}$ cm$^{-3}$ with $x_{j+} = 0.2$ $\mu$m. Two $\rho_c$ values of $1 \times 10^{-6}$ and $1 \times 10^{-7}$ $\Omega \cdot$ cm$^2$ are considered and for each case, both the surface contact and the recessed contact with $m_j = 1000$ Å are simulated for comparison purposes. Since the current distributions near the end of the junction are nearly equal for the above four conditions as shown in Section III-A, the differences of $R_t$ between the above four conditions should come from the difference of $R_{ext}$. The most important difference of these $R_t - L_c$ curves between the surface contact and the recessed contact is that the $R_t$ of

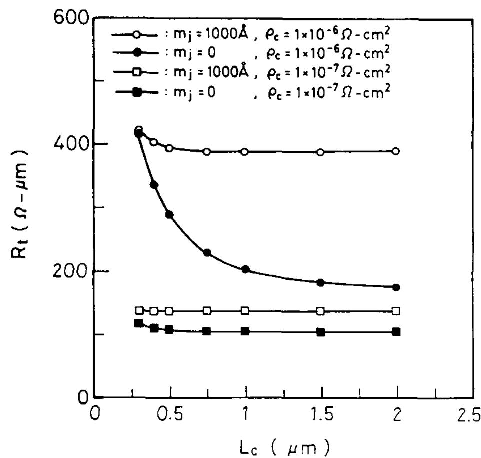


Fig. 6. Total resistance ($R_t$) versus contact length ($L_c$) with $W_c$ = 1 μm. The main simulation parameters are: $L_{sp}$ = 0.2 μm, δ = 0, $C_{s+}$ = 1 × $10^{20}$ $cm^{-3}$, $C_b$ = 1 × $10^{16}$ $cm^{-3}$, and $x_{j+}$ = 0.2 μm.

the surface contact increases rapidly as the $L_c$ decreases to less than 1 μm for $\rho_c = 1 \times 10^{-6}\ \Omega \cdot cm^2$ and 0.5 μm for $\rho_c = 1 \times 10^{-7}\ \Omega \cdot cm^2$, while the recessed contact interface seems to effectively retard the increasing tendency. The increase in $R_f$, i.e., $R_{ext}$ in the SALICIDE structure, with the decrease in $L_c$ for the surface contact has been derived by the 1D TLM model through the concept of transfer length ($L_t$) [28]. The increase in $R_t$ results from an increase in $R_f$. The retardation of the increase in $R_t$ for the recessed contact implies a decrease in $L_t$ for this contact type. This will be discussed in the next section.

### E. Contact Width ($W_c$) Dependence

Perera and Krusius have reported a significant increase in $R_{ext}$ with a decrease in $W_c$ by the measurement of contacts with different $W_c$ values [29]. Such a contact width dependence is not observed in the 1D TLM model. They attribute this to the lateral current-crowding effect. To monitor the relation between $R_{ext}$ and $W_c$, the simulation program is extended to be a 3D simulator. Although the silicide is self-aligned to the S/D region, the silicide does not cover the entire diffused S/D region due to the lateral diffusion of the S/D junction. Fig. 7 shows the top view of the structure for the 3D simulation. The side view of the structure is the same as that shown in Fig. 2(b). Fig. 8 shows the relation between $R_{ext}$ and $W_c$ with $L_c$ = 1 μm. The lateral diffusion ($W_{ld}$) is assumed to be 0.2 μm. The other parameters used in this simulation are the same as those used in Section III-D. It is observed that $R_{ext}$ decreases with the decrease of $W_c$ for both the surface contact and the recessed contact, which contradicts the results reported in [29]. This can be reasonably understood as follows. The resistance due to the lateral diffusion of the S/D junction ($R'_{lt}$, unnormalized value) is in parallel with that of the silicided region. As the width of the silicided region decreases, the resistance of this region increases,

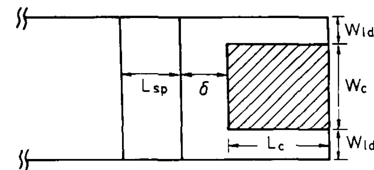


Fig. 7. Top view of the structure for 3D simulation; the diffused S/D junction is wider than the contact width.

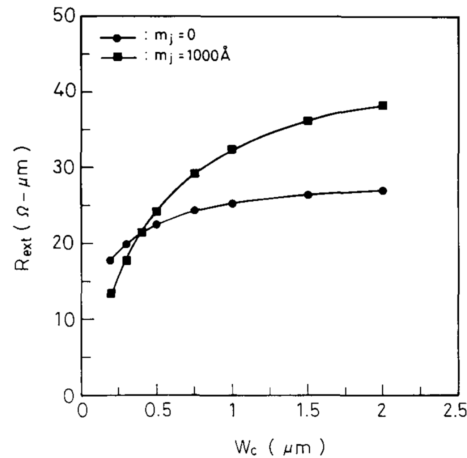


Fig. 8. External resistance ($R_{ext}$) versus contact width ($W_c$) with $L_c$ = 1 μm. The main simulation parameters are: $L_{sp}$ = 0.2 μm, δ = 0, $C_{s+}$ = 1 × $10^{20}$ $cm^{-3}$, $C_b$ = 1 × $10^{16}$ $cm^{-3}$, $x_{j+}$ = 0.2 μm, and $\rho_c$ = 1 × $10^{-6}$ Ω · $cm^2$.

while the $R'_{lt}$ does not change. When these resistances are normalized to $W_c$ (multiplied by $W_c$), the resistance contributed by the silicided region becomes independent of the $W_c$ while the $R_{lt} = R'_{lt} \times W_c$ is proportional to the $W_c$. Thus the combined normalized resistance—$R_{ext}$—should be lower for the narrower $W_c$. If the resistance is normalized to the width of the diffused S/D region ($W_c + 2 \times W_{ld}$) instead of the $W_c$, the $R_{ext}$ increases with the decrease of $W_c$. The rapid increase in $R_{ext}$ with the decrease in $W_c$ in [29] is likely due to the process deviation during the formation of narrower contacts.

## IV. A Simple Analytical Explanation

It has been shown in Section III-A that a significant amount of current is pushed into the high-resistivity region of the junction due to the recession of the contact interface. It is also shown that only a short distance (700 Å) away from the contact edge, the current distributions of the recessed contact and the surface contact become almost identical. Thus it is possible to estimate the increase of $R_{ext}$ by considering the change in resistance from the metal to the edge of the contact only, i.e., by considering the increase in $R_f$. Fig. 9 shows the simplified current path of the recessed contact structure. The current flowing in the silicide can flow into the silicon region only through the two interfaces: the sidewall contact and the

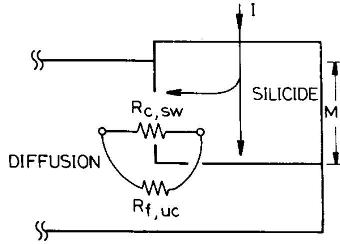


Fig. 9. Schematic diagram showing the simplified current path of the recessed contact structure.

planar contact. Thus the $R_f$ of the recessed contact structure is the contact resistance of the sidewall contact ($R_{c,sw}$) in parallel with the front resistance ($R_{f,uc}$) contributed by the planar contact and the silicon region under the planar contact

$$\frac{1}{R_f} = \frac{1}{R_{c,sw}} + \frac{1}{R_{f,uc}}. \tag{2}$$

The $R_{c,sw}$ can be calculated by

$$R_{c,sw} = \frac{\rho_c}{m_j}. \tag{3}$$

Based on the 1D TLM model, the $R_{f,uc}$ is expressed as

$$R_{f,uc} = \frac{\sqrt{R_{sh,uc} \times \rho_c}}{\tanh\left[\frac{L_c}{L_t}\right]} \tag{4}$$

where $R_{sh,uc}$ is the sheet resistance of the silicon region under the planar contact interface and $L_t$ is the transfer length defined as

$$L_t = \sqrt{\frac{\rho_c}{R_{sh,uc}}}. \tag{5}$$

Before applying (4), we first examine its validity in the case of nonuniform doping of the underlying Si layer. Fig. 10 compares the $R_f$ versus sheet resistance of the doped silicon ($R_{sh}$) for the surface contact obtained by 2D simulation and that calculated by 1D TLM model. Different doping profiles were generated by varying the combination of $x_{j+}$, $C_{s+}$, and $C_b$. The $R_{sh}$ is then obtained by integrating the resistivity during simulation. The calculated $R_f$ values are very close to the 2D simulated values and in most cases the error is within 5%. This implies that the 1D expression of $R_f$ is still accurate enough in the 2D case if the doped Si layer is represented by an effective value of sheet resistance.

Fig. 11 compares the $\Delta R_t$–$m_j$ curve shown in Fig. 4 with the $\Delta R_f$–$m_j$ curve obtained by 2D simulation and that calculated by (2)–(5). The $\Delta R_f$–$m_j$ curves are lower than the $\Delta R_t$–$m_j$ curves due to the neglect of resistance beyond the contact edge. The underestimation obtained by the simplified circuit shown in Fig. 9 is within 20%. The $R_{f,uc}$

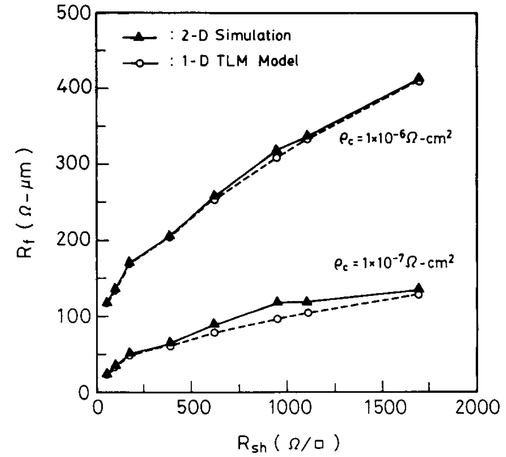


Fig. 10. Comparison of the $R_f$ versus $R_{sh}$ obtained by 1D TLM model and 2D simulation.

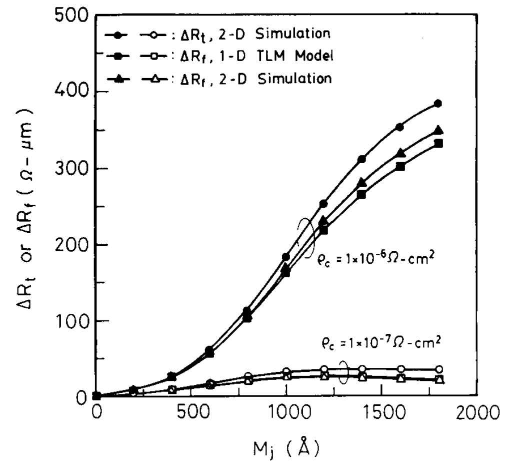


Fig. 11. Comparison of the $\Delta R_t$–$m_j$ curves shown in Fig. 4 with the $\Delta R_f$–$m_j$ curves obtained by 1D TLM model and 2D simulation.

increases rapidly with the increase of $m_j$ because of the dramatic increase in $R_{sh,uc}$ as the heavily doped Si region is consumed. Although the $R_{c,sw}$ decreases with the increase in $m_j$ because of the increase of the sidewall contact area, the $R_{c,sw}$ is still higher than the $R_{f,uc}$ in most cases since the area of the sidewall contact is very small. Therefore, the $\Delta R_t$ increases with the increases of $m_j$ in all of the simulated cases.

The increase in $R_{sh,uc}$ due to the increase of $m_j$ decreases the $L_t$ according to (5). Fig. 12 shows the $L_t$–$m_j$ relation. It is observed that as the contact interface recesses into the silicon, the $L_t$ decreases rapidly. In the present simulation condition, the $L_t$ decreases from 1 to 0.35 $\mu$m as $m_j$ increases from 0 to 1000 Å for $\rho_c = 1 \times 10^{-6}\ \Omega \cdot \text{cm}^2$ and decreases from 0.35 to 0.08 $\mu$m as $m_j$ increases from 0 to 1000 Å for $\rho_c = 1 \times 10^{-7}\ \Omega \cdot \text{cm}^2$. This explains the retarded increase of $R_t$ with the decrease of $L_c$ for the recessed contact shown in Fig. 6.

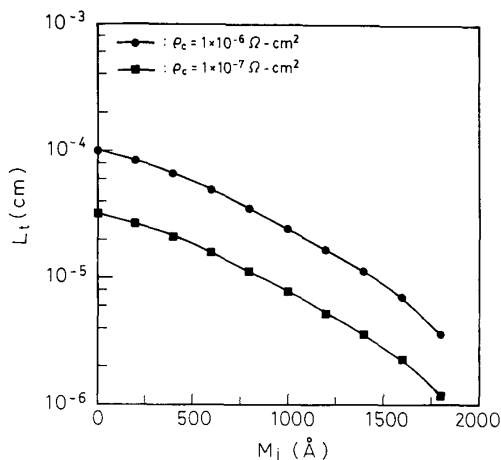


Fig. 12. Transfer length ($L_t$) versus depth of contact interface ($m_j$). The main simulation parameters are: $L_c = W_c = 1\ \mu$m, $x_{j+} = 0.2\ \mu$m, $C_{s+} = 1 \times 10^{20}$ cm$^{-3}$, and $C_b = 1 \times 10^{16}$ cm$^{-3}$.

## V. Examination of Measured Results

In this section, we take the recession of contact interface into consideration to explain the measured $R_{ext}$ data reported recently. Two sets of data presented at the IEEE International Electron Device Meeting (IEDM) are examined. The reported $R_{ext}$ values seem to be rather high and have not been appropriately explained. Both n- and p-type contacts were fabricated in these reported works, but only the n-type contact is discussed here.

### *A. Davari et al., in IEDM '88* [7]

In that paper the authors presented a high-performance 0.25-$\mu$m CMOS technology. The S/D structure is a conventional heavily doped structure and the operating voltage is 2.5 V. The gate oxide is 70 Å thick, the effective channel length is 0.25 $\mu$m, the channel concentration is $1 \times 10^{17}$ cm$^{-3}$, and the threshold voltage is 0.4 V. The junction depth is only 0.11 $\mu$m and the $TiSi_2$ SALICIDE process consumes 300 Å of the junction. The minimum channel resistance at a gate voltage of 2.5 V is about 650 $\Omega \cdot \mu$m. However, the measured S/D resistance shows a rather high value of $2 \times R_t = 600\ \Omega \cdot \mu$m. Such a high parasitic resistance should substantially affect the performance of the device, such as the low electron mobility of 370 cm$^2$/V/cm.

The $R_t$ is first simulated ignoring the recession of contact interface. The dopant profile of the S/D junction measured by SIMS is shown in that paper. The profile can be reasonably approximated by the Gaussian distribution. Assuming a 50% activation, the surface concentration is about $1 \times 10^{20}$ cm$^{-3}$ and the electrical junction depth is about 0.1 $\mu$m. The thickness of the sidewall spacer is not shown in that paper and is assumed to be 0.1 $\mu$m in this simulation. Also lacking is the value of $\rho_c$. Since they referred to the $\rho_c$ in their previous work and the $\rho_c$ in that paper is on the order of $10^{-7}$–$10^{-6}\ \Omega \cdot$ cm$^2$, $\rho_c$ of $1 \times 10^{-6}\ \Omega \cdot$ cm$^2$ is chosen in this simulation [30]. Finally, an $L_c$ of 1 $\mu$m is assumed. It should be noted that the simulation parameters chosen here are intended to increase the simulated $R_t$. The simulation gives a $2 \times R_t$ of 400 $\Omega \cdot \mu$m only, which is 200 $\Omega \cdot \mu$m lower than the reported value. However, if the recession contact interface with $m_j = 300$ Å is taken into consideration, a $2 \times R_t$ of 580 $\Omega \cdot \mu$m is obtained. This implies that if the $m_j$ could be reduced, the performance of the device and circuit could be improved further.

### *B. Perera and Krusius in IEDM '89* [29]

Perera and Krusius measured the $R_{ext}$ of the SALICIDE structure using a depletion-mode MOSFET test structure. The extracted $R_{ext}$ of that structure is identical to the $R_f$. The $L_c$ and $W_c$ of the S/D areas are varied from 0.3 to 1.7 $\mu$m and from 0.2 to 2 $\mu$m, respectively, and an obvious $W_c$ dependence of $R_{ext}$ is reported. This has been discussed in Section III-E of this paper and is likely due to the process deviation. Thus only the result of $W_c = 1\ \mu$m is discussed here. The junction depth is 0.12 $\mu$m. The thickness of $TiSi_2$ employed is 550–600 Å which implies a silicon consumption of about 500 Å. The measured $\rho_c$ values are $3$–$6 \times 10^{-7}\ \Omega \cdot$ cm$^2$. The extracted $2 \times R_{ext}$ for a long $L_c$ of 1.7 $\mu$m is about 235 $\Omega \cdot$ cm and it increases as $L_c$ is decreased to less than 1 $\mu$m. The resistance seems too high for the low $\rho_c$ value of $3$–$6 \times 10^{-7}\ \Omega \cdot$ cm$^2$.

Due to the lack of parameters regarding the doping concentration, the following assumptions are made. The substrate concentration is assumed to be $1 \times 10^{17}$ cm$^{-3}$. The junction profile is still approximated by the Gaussian function. A $\rho_c$ of $4 \times 10^{-7}\ \Omega \cdot$ cm$^2$ is selected. With the $L_t$ declared in that paper of 0.6–0.8 $\mu$m, the $R_{sh}$ of the junction can be calculated by (5) to be 63–110 $\Omega/\square$. The surface concentration is then tuned so that the $R_{sh}$ is within the range of 63–110 $\Omega/\square$ and a value of $2 \times 10^{20}$ cm$^{-3}$ is selected. With these selected parameters, the $R_{sh}$ is 79 $\Omega/\square$ and the $L_t$ is 0.71 $\mu$m, both of which are consistent with those declared in that paper. Ignoring the recession of the contact interface, the simulated $2 \times R_{ext}$ is only 115 $\Omega \cdot \mu$m with $L_c = 1.7\ \mu$m, which is 50% lower than the measured value. Selecting other values of surface concentration which make $L_t$ within 0.6–0.8 $\mu$m results in a very limited change of the $2 \times R_{ext}$ value. However, if a recession of the contact interface of $m_j = 500$ Å is taken into consideration, the $2 \times R_{ext}$ value of 262 $\Omega \cdot \mu$m is obtained.

In [29] the increase of $R_{ext}$ with the decrease of $L_c$ is reported, but the extent is lower than that predicted by the TLM model if the $L_t$ is within 0.6–0.8 $\mu$m. Fig. 13 compares the $2 \times R_{ext}$ versus $L_c$ of the measured results to that of the simulated results with $m_j = 0$ and $m_j = 500$ Å. The results by 2D simulation considering the recession of contact interface are consistent with the experimental results. This consistency further confirms that the consideration of the contact interface recession plays an important role in the determination of $R_{ext}$.

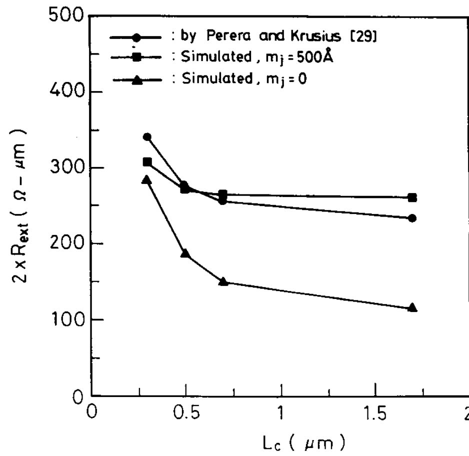


Fig. 13. Comparison of the 2 × $R_{ext}$-$L_c$ relation of the experimental results ([29]) with the simulated results. The main simulation parameters are: $L_c$ = 1.7 μm, $W_c$ = 1 μm, $x_{j+}$ = 0.12 μm, $C_s^+ = 2 \times 10^{20}$ cm$^{-3}$, $C_b = 1 \times 10^{17}$ cm$^{-3}$, and $\rho_c = 4 \times 10^{-7}$ Ω · cm$^2$.

## VI. Comparison of Different Contact Types

Based on the results and discussions in the previous sections, different contact types are compared briefly in this section. There are four S/D contact types: the self-aligned recessed contact (SR-type), the self-aligned surface contact (SS-type), the non-self-aligned recessed contact (NR-type), and the non-self-aligned surface contact (NS-type). It is assumed that the same $\rho_c$ value can be obtained for both of the surface and recessed contacts. The schematic top view and cross-sectional view of these four contact types are shown in Fig. 14.

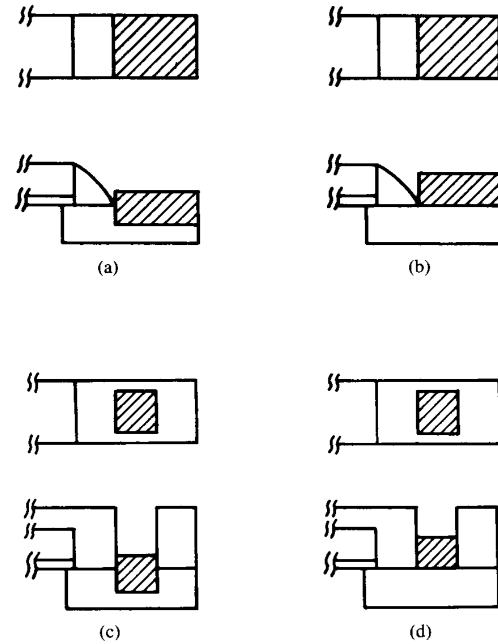


Fig. 14. Schematic top view and cross-sectional view of the four contact types: (a) SR-type, (b) SS-type, (c) NR-type, and (d) NS-type.

### A. SR-Type

The SR-type is the contact type formed by the standard SALICIDE process. Previous studies on the structure were aimed at its benefit of larger contact area relative to the non-SALICIDE structure. In this work, the increase in resistance due to the recession of the contact interface is explored. This would affect the performance of sub-half-micrometer devices but has not been considered until now. This effect will become more and more severe as the minimum feature size is further scaled down, and the benefit of the typical SALICIDE structure may disappear completely. Scaling the thickness of silicide film faster than that required by the scaling of junction depth can relax the problem. However, the high-temperature stability of the thin silicide film should be of concern. Furthermore, since a thick silicide layer is needed to reduced the sheet resistance, thinning the silicide on the S/D implies that an additional silicide process must be employed to satisfy the requirement of interconnection. It seems that the SR-type contact should be modified for the sub-half-micrometer regime.

### B. SS-Type

The SS-type contact takes full advantages of the SALICIDE structure. The spacing between the contact and gate is minimized and the contact area is as large as the S/D area. No silicon is consumed during contact formation, thus the high-conductivity layer of the junction is preserved. The problem is how to realize the structure. Conventional SALICIDE process forms the SR-type contact instead of the SS-type. Using metal or co-deposited silicide as a contact material needs an additional mask to separate the gate and the S/D; thus it is not the self-aligned scheme. A possible method to form the SS-type contact is to utilize the technique of selective growth of Si [31], [32]. After the S/D formation, a thin layer of silicon is selectively grown on the S/D region followed by the standard SALICIDE process. The thickness of the selectively grown silicon layer is designed such that the raised silicon layer is fully consumed during the silicidation process. In this proposed technology, the thickness of the silicide layer has a wide tunable range. The problem of high-temperature stability of the thin silicide film is avoided and the requirement of a thick silicide film by the interconnection line is satisfied. Certainly, some processing problems still remain to be solved, such as the immaturity of the technique of selective growth of Si and the bridging between the gate and the raised S/D contact.

### C. NR-Type and NS-Type

The main disadvantages of the non-self-aligned contacts are smaller contact area and larger spacing between gate and contact (δ) relative to the self-aligned contact. Since the δ value decreases with the scale down of the minimum feature size, the resistance contributed by the spacing becomes more and more insignificant. The only

major disadvantage of the non-self-aligned contact is the smaller contact area, but it has the benefit of easy processing. Besides the smaller contact area, the NR-type contact also suffers from an increase of resistance due to the recession of the contact interface. It is the worst contact among the four contact types. To compare the SR-type contact with the NS-type contact is rather complex. The larger contact area of the SR-type decreases the contact resistance; however, this advantage may be outweighed by its recessed structure. Table I lists the $R_t$ values of the four contact types under the same processing technology—a minimum feature size of 0.3 $\mu$m. The junction is a conventional heavily doped structure with a junction depth of 0.1 $\mu$m. The surface and substrate concentration are $1 \times 10^{20}$ and $1 \times 10^{16}$ cm$^{-3}$, respectively. For the non-self-aligned contact, the contact length, the spacing between the gate and contact, and the spacing between the contact and drain edge (i.e., spacing between contact and field oxide) are all 0.3 $\mu$m and the drain length becomes 0.9 $\mu$m. For the self-aligned structure, the thickness of the sidewall is assumed to be 0.1 $\mu$m; thus the $L_c$ is 0.8 $\mu$m. For the recessed contact, $m_j$ is assumed to be 500 Å. The contact resistivity is assumed to be $1 \times 10^{-6}$ $\Omega \cdot$ cm$^2$ for all of the four contact types. It is shown that the SS-type contact has the lowest $R_t$, while the NR-type contact has the highest $R_t$. The $R_t$ of the NS-type contact is lower than that of the SR-type contact for the given conditions, which implies that the NS-type contact is still available in the sub-half-micrometer regime due to its ease and flexibility of processing in comparison with the self-aligned contact. This result seems to indicate that the necessity of a typical SALICIDE structure in the sub-half-micrometer regime needs careful consideration. It should be noted that the actual contact width of the self-aligned contact is wider than that of the non-self-aligned contact but the difference is very limited except for the narrow-width devices.

TABLE I
COMPARISON OF $R_t$ OF FOUR CONTACT TYPES
(Main simulation parameters are: $x_j = 0.1$ $\mu$m, $C_{s+} = 1 \times 10^{20}$ cm$^{-3}$, $C_b = 1 \times 10^{16}$ cm$^{-3}$, and $\rho_c = 1 \times 10^{-6}$ $\Omega \cdot$ cm$^2$. For the non-self-aligned contacts (NS- and NR-types), $L_c = 0.3$ $\mu$m and the spacings between contact and gate and between contact and drain edge (i.e., between contact and field oxide) are all 0.3 $\mu$m. For the self-aligned contacts (SS- and SR-types), $L_{sp} = 0.1$ $\mu$m and $L_c = 0.8$ $\mu$m.)

| | Surface Contact ($\Omega \cdot \mu$m) | Recessed Contact ($\Omega \cdot \mu$m) |
|---|---|---|
| Self-aligned | 217 | 531 |
| Non-self-aligned | 444 | 592 |

### D. Improvement of the Recessed Contact

There are several possible approaches which could relax the increase of $R_{ext}$ of the recessed contact. The first approach is to make use of a steep junction profile; however, to obtain a junction profile steeper than the Gaussian profile with junction depth less than 0.1 $\mu$m is very difficult because the as-implanted profile is nearly Gaussian. The second approach is to scale down the thickness of silicide; however, thin silicide contradicts the low-sheet-resistance requirement by the interconnection line. Another problem associated with the thin silicide is its high-temperature stability. The highest sustainable temperature of $TiSi_2$ and $CoSi_2$ of less than 500-Å thickness has decreases to 800°C. The high-temperature stability superiority of refractory metal silicides to that of noble silicides disappears. From this viewpoint, the silicide with the greatest silicide thickness to silicon consumption ($T_s/T_{si}$) ratio becomes the most suitable material for the SALICIDE structure. Cobalt silicide may be ruled out due to its low $T_s/T_{si}$ ratio of 0.97. Platinum silicide, with the highest $T_s/T_{si}$ ratio of 1.5 among the self-aligned silicides, might be a candidate in the future. Another approach is to make use of the technology of selective growth of Si. The S/D is raised by selective growth of Si and the raised Si is then converted to silicide. This forms the SS-type contact which can take the full advantages of the SALICIDE structure but the process is more complex than that of the conventional SALICIDE structure. More work is needed to evaluate this process but it is beyond the scope of this paper.

## VII. CONCLUSIONS

In this paper, the authors report for the first time that the external resistance of the self-aligned silicided source/drain structure increases with the recession of the contact interface during the silicidation process because a significant amount of current is forced into the low-resistivity region of the junction due to the recessed contact interface. The increment of $R_t$ can be estimated by a simple analytical expression to an accuracy within 20%. From the simulated current distribution, it is observed that the increase of $R_t$ is almost independent of the corner shape of the junctions, whether it is LDD structure or not. Parameters which influence the increase in $R_t$ such as the recession of the contact interface, the specific contact resistance, the depth and the resistivity of the junction, as well as the contact length and width are all examined. It is observed that the increase in $R_t$ is strongly dependent on the doping profile and the recession of the contact interface. The increase in $R_t$ may be as high as several hundred ohms-micrometers. This problem becomes worse with the scaling of the minimum feature size. In this work, the $\rho_c$ value is assumed to be independent of $m_j$. In fact, the $\rho_c$ value should change with the increase of $m_j$. The relation between the $\rho_c$ and the interface concentration has been calculated by Ng and Liu [33]. It is shown that the $\rho_c$ value is a very strong function of the interface concentration. Once the high doping region is consumed during silicidation, the $\rho_c$ value will increase with the increase of $m_j$. Thus the increase of $R_{ext}$ due to silicidation in reality may be more severe than those predicted here. A steep junction can relax the problem, but it is very difficult to obtain a steep junction with a depth of less than 0.1 $\mu$m. New technologies which could form the contact structure

close to the surface contact should be developed. Before that happens, the non-self-aligned surface contact is still available in the sub-half-micrometer regime.

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