A Class-B Output Buffer for Flat-Panel-Display Column Driver

Pang-Cheng Yu and Jiin-Chuan Wu

***Abstract*— Due to the large number of output buffers on a column driver chip of a flat-panel display, the quiescent current and die area of the output buffer must be minimized. This paper presents a low static power, large output swing, and wide operating voltage range class-B output buffer amplifier for driving the large column line capacitance in flat-panel display. A comparator is used in the negative feedback path to eliminate quiescent current in the output stage. The proposed output buffer circuit was implemented in a 0.8-μm CMOS process. Its output voltage swing is from 1 V to the supply voltage. With 5-V supply and 600-pF load, the maximum tracking error is ± 7 mV. The measured static current is 24 μA. The settling time for 4-V swing to within 0.2% is 8 μs, which is more than adequate for driving 1280 $\times$ 1024 pixels liquid crystal displays with 86-Hz frame rate and 256 gray levels in each color.**

***Index Terms*— Class-B amplifier, flat-panel display, output buffer.**

I. Introduction

THERE are three special requirements for the output buffer for a flat-panel-display column driver [1], [2]. First, a large number of output buffers are needed. For a 640 $\times$ 480 pixels color panel, the number of analog buffers needed is $640 \times 3 = 1920$. For a high-end 1280 $\times$ 1024 color panel, the number of output buffers is 3840. Many column-driver IC's must be used to achieve the number of outputs needed. However, to reduce system cost and increase reliability, the total number of driver IC's used should be minimized. Thus, the first requirement of the output buffer is that its die area must be minimized in order to put more output drivers on one chip. Second, since the liquid crystal displays (LCD's) are commonly used in portable systems that are battery powered, the power dissipation must be minimized to extend the battery lifetime. Thus, the second requirement is low power dissipation. Third, the input to the output buffer is always step function because the pixels are updated row by row. The output voltage must settle within a horizontal scanning time. The horizontal scanning frequency ranges from 31.5 to 97.8 KHz. With stepwise input, the theoretical lower limit of the output buffer is 0.5 $fC_LV_SV_{\rm DD}$, where f is the signal frequency, C_L is the load capacitance, V_S is the voltage swing of the column signal, and $V_{\rm DD}$ is the supply voltage. The power dissipation of a column driver is dependent on the image displayed. The maximum power dissipation occurs when the image on a column is alternating black and white pixel by pixel, i.e., both the frequency and the signal voltage swing are maximum. On the other hand, when the image on a column is a constant gray level, the theoretical dynamic power is zero because both f and V_S are zero.

To reduce power dissipation, a class-A amplifier with variable bias current was used [3]. The amplitude of the output-stage bias current is controlled by a digital pulse. In the first one-third of the scan-line period, a large bias current is used to make sure the output is settled within this period. For the rest of the scan-line period, a much smaller bias current is used to hold the output value. However, when the gray level does not change much in a column, this scheme wastes too much power. A dynamic biasing technique [4] was proposed to increase the bias current of the differential input stage of a two-stage amplifier, when the input voltage difference is large. This technique does not reduce the output-stage bias current. A class-B amplifier [5], [6] has a better power efficiency. But the sizes of the output transistors are large because the gate-to-source voltages are smaller than the supply voltage. To reduce both die area and power dissipation, another scheme [7] precharges the output to the supply voltage at the beginning of each scan-line period. Then the output voltage is discharged toward 0 V, and the output voltage is compared with the input voltage using a comparator. The discharging stops when the output voltage is equal to the input voltage. This scheme has no static power and is compact. However, it wastes dynamic power when the gray level in a column does not change much. Furthermore, its final voltage is always smaller than the input, due to the finite response time of the comparator.

In this paper, a class-B CMOS output buffer is proposed because it has a better power efficiency. To reduce the size of the output stage, nonlinear elements (the comparators) are included in the series-shunt feedback path. In Section II, the output buffer design is described. The experimental results are shown in Section III. A conclusion is given in Section IV.

II. Design of Buffer Amplifier

Fig. 1 is the block diagram of the proposed class-B output buffer. It has a common source output stage, which offers good swing characteristics, high efficiency, and low nonlinear distortion. The basic structure of this buffer is not new [5], [6]. The main difference is that the error amplifiers in [5] and [6] are replaced by the comparators and an inverter, which are nonlinear. The comparators and inverter serve as series-shunt negative feedback to reduce the output resistance. The output of the comparator is designed to be either $V_{\rm DD}$ or 0 V, i.e., when the output transistor is turned on to charge or discharge the output node, the gate-to-source voltage is always $V_{\rm DD}$. In this way, a smaller output transistor can be used. The two comparators, Cmp1 and Cmp2, are identical. For ease of discussion, assume that the offset voltages of the comparators are zero and that the process model is typical.

Manuscript received November 3, 1997; revised April 6, 1998. This work was supported by the National Science Council under Contract NSC86-2215-E-009-053 and by the Chip Implementation Center, Taiwan, R.O.C.

The authors are with the Integrated Circuit and Systems Laboratory, Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan 300 R.O.C. (e-mail: jcwu@alab.ee.nctu.edu.tw).

Publisher Item Identifier S 0018-9200(99)00407-2.

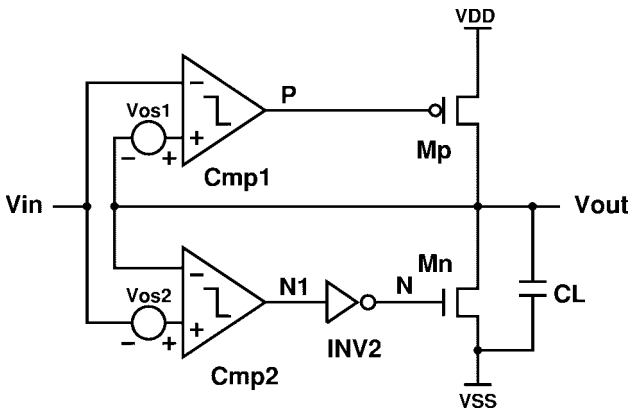

Fig. 1. Block diagram of class-B output buffer.

Fig. 2 shows the complete circuit diagram of the buffer amplifier. The comparator Cmp1 consists of an NMOS-input differential amplifier (M1–M6) and an inverter INV1 (M9 and M10). To eliminate quiescent current when $V_{\rm OUT}$ is equal to $V_{\rm IN}$, the outputs of the comparators $V_{\rm CMP}$ should be $V_{\rm DD}$, so that both output transistors M_p and M_n are completely turned off. To make $V_{\rm CMP} = V_{\rm DD}$ when $V_+ = V_-$—where V_+ and V_- are the noninverting and inverting inputs of the comparator, respectively—the common-mode output voltage of the differential amplifier must be smaller than the logic threshold voltage of the inverter. With NMOS-input transistors, the input common-mode range of the differential pair is from 1 to 5 V. The output voltage varies from 3.71 to 3.65 V when the input common-mode voltage is varied from 1 to 5 V. The logic threshold of INV1 is designed to be 4.06 V. Thus, the common-mode output of the differential pair is 0.35–0.41 V lower than the logic threshold of the inverter INV1, which ensures that both output transistors are off when $V_{\rm OUT} = V_{\rm IN}$.

The voltage gain of the differential pair is 34. Thus, when $V_{\rm IN} - V_{\rm OUT} \geq 10$ mV, the voltage on node P (Fig. 1) will be a logical low voltage, i.e., the output PMOS will be turned on. Similarly, when $V_{\rm IN} - V_{\rm OUT} \leq -10$ mV, the output NMOS will be turned on. Thus, when $V_{\rm OUT}$ has been charged or discharged to within 10 mV of $V_{\rm IN}$, i.e., $\mid V_{\rm IN} - V_{\rm OUT} \mid \leq 10$ mV, both output transistors are off and the maximum tacking error is 10 mV. In this way, when input voltage changes, only one of the two output transistors will be turned on to make the output follow the input. Once the output voltage is within the maximum tacking error, both output transistors are off. Thus, the dynamic power can approach the theoretical lower limit of 0.5 $fC_LV_SV_{\rm DD}$. Since the threshold mismatch in a CMOS process could be as large as 10 mV, the influence of the comparator's offset voltage must be considered. With the sign of the offset voltages defined in Fig. 1, the operation of the output buffer becomes:

1) when $V_{\rm IN} - V_{\rm OUT} - V_{OS1} \geq 10$ mV, the output PMOS will be turned on;
2) when $V_{\rm IN} + V_{OS2} - V_{\rm OUT} < -10$ mV, the output NMOS will be turned on;
3) when -10 mV $- V_{OS2} < V_{\rm IN} - V_{\rm OUT} < 10$ mV $+ V_{OS1}$, both output transistors are off.

Thus, if $V_{OS1} = -5$ mV and $V_{OS2} = -5$ mV, then both output transistors are off when -5 mV $< V_{\rm IN} - V_{\rm OUT} < 5$ mV. If $V_{OS1} = -5$ mV and $V_{OS2} = 5$ mV, then both output transistors are off when -5 mV $< V_{\rm IN} - V_{\rm OUT} < 15$ mV. It can be seen that a positive comparator offset increases the safety margin for short-circuit current but also increases voltage error. A negative offset reduces the margin for short-circuit current, but voltage error is also reduced. In this design, when negative offset is more than 10 mV, the margin is reduced to zero, i.e., short-circuit current occurs when $V_{\rm IN} = V_{\rm OUT}$. Note that a class-B amplifier has crossover distortion. In this design, the crossover distortion is the tracking error. When the tracking error is reduced to zero, the circuit becomes a class-A amplifier. The designed nominal tracking error is a tradeoff between output accuracy and immunity to comparator offset.

Since the thin-film-transistor LCD can display up to 256 gray levels in each color, each gray level is 16 mV at 4.096 V full scale. Thus, the output buffer must have a voltage error less than ± 8 mV. Without comparator offset, the designed input resolution of the output buffer is ± 10 mV, i.e., about 0.6 least significant bit (LSB). When process varies, the output common-mode voltage of the differential pair and the inverter's logic threshold voltage both vary in the same direction so that the difference between these two voltages remains at about 35 mV. The voltage gain of the differential pair varies between 32 and 36 over process variations and 0–100°C temperature range. Thus, the input resolution of the output buffer remains at about ± 10 mV.

The ac analysis of this output buffer was done with $V_{\rm IN} = 3.011$ V and the negative input node, $V_{\rm IN-} = 3$ V, so that Cmp1 and Mp are operating in linear region. The output loading is 600 pF. The dc gain is 88 dB at room temperature and with typical process. There are three poles: the dominant pole, which occurs at 90 Hz, is caused by the output node; the second pole, at 2 MHz, is caused by the differential pair's output node; and the third pole, at 100 MHz, is caused by the INV1 inverter's output node. The unity-gain bandwidth is 1.3 MHz; the phase margin is 50°. Since the output node is the dominant pole, reducing output load capacitance increases the bandwidth but reduces phase margin. Increasing the bias current of the differential stage or reducing the input capacitance of the INV1 inverter can move the second pole outward, which increases the phase margin.

III. Experimental Results

The proposed output buffer amplifier was fabricated using a 0.8-μm CMOS technology and a 5-μm CMOS 24-V technology. The latter is for field emission devices applications, which require a higher voltage rating. Both chips functioned. Since the design principles are the same, only the results from the 0.8-μm CMOS chip are reported. The die photograph of the output buffer is shown in Fig. 3. The active area of an output buffer is 230 $\times$ 140 μm^2 excluding input and output pads. Fig. 4 shows the measured result of the output buffer with 10 KHz triangular input and 600 pF load capacitance; the input voltage range is 1–5 V. The lower trace is the input and the upper trace is the output. The output basically

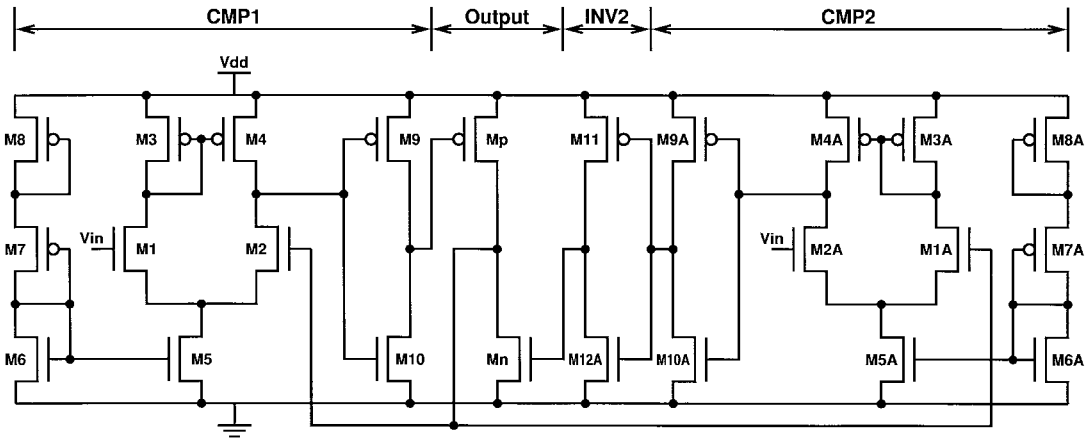

Fig. 2. Circuit diagram of class-B output buffer.

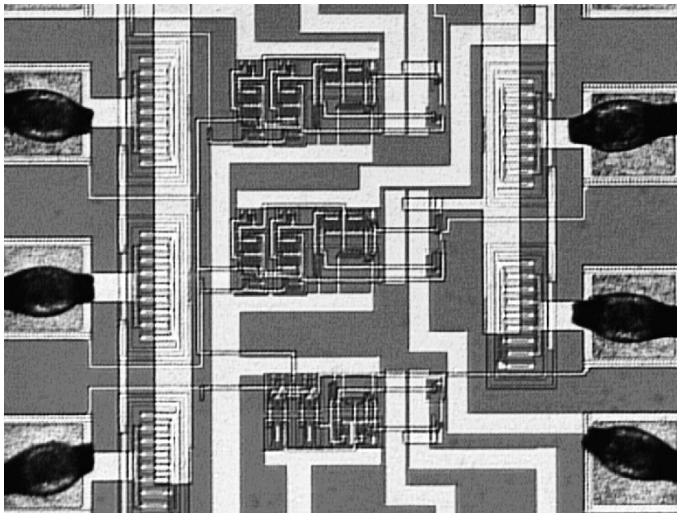

Fig. 3. The microphotograph of the die.

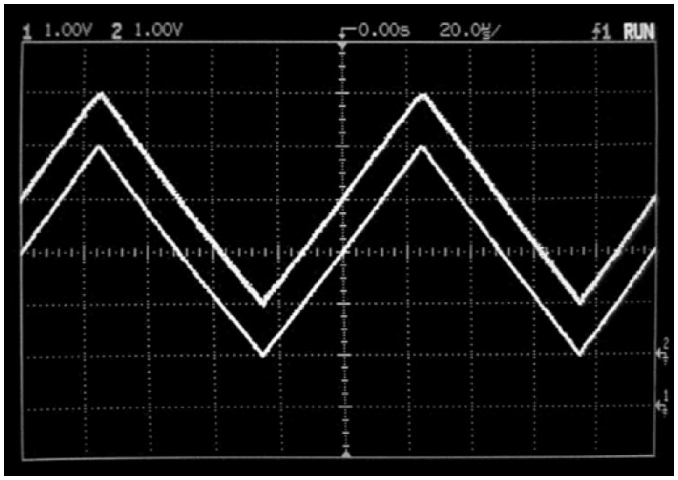

Fig. 4. The output voltage of the output buffer with 10 KHz triangle wave input. The lower trace is input.

follows the input. The step response with 50 KHz square wave input and 600 pF load capacitance (not including parasitic capacitance of the test circuit) is shown in Fig. 5. The lower trace is the input whose voltage changes between 1 and 5 V. The upper trace is the output, and the time for the output to settle within 0.2% (0.5 LSB) of the final voltage is 8 and 3 μs for the rising and falling edges, respectively. The supply current for the output stage is 131 μA, and the supply current for the rest of the circuit (static bias current) is 24 μA. When input frequency is varied from 1 to 50 KHz, the static bias current remained unchanged and the output-stage current varied linearly with the frequency. The theoretical output-stage current at 50 KHz is 120 μA, i.e., the measured current corresponds to a 650 pF loading.

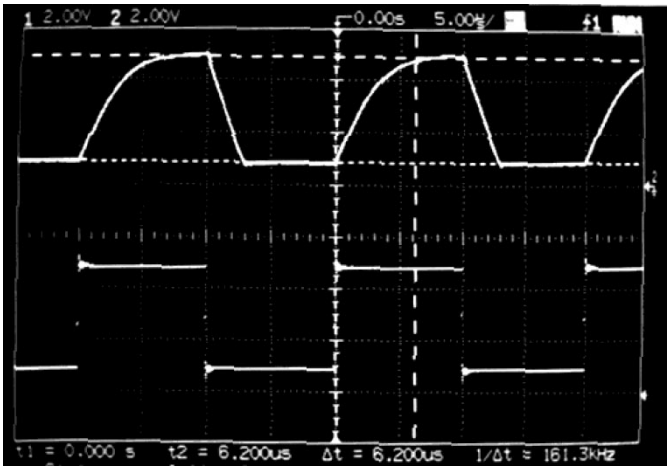

Fig. 5. The step response of class-B output buffer for 600 pF load capacitance.

An example of the steady-state error of the output buffer is shown in Fig. 6. To show the small error voltage, the signals are ac coupled. The input is a 100 mV swing square wave. The output swing is 108 mV. Thus, the average tracking error is $\pm$4 mV. The tracking errors of the output buffer for input voltages ranging from 1 to 5 V are shown in Fig. 7. The input voltage is changed in 0.1 V steps quasi-statically. The errors are all within $\pm$7 mV. For inputs between 1.2 and 5 V, the errors are smaller (within $\pm$4 mV). The steady-state output-stage current is always zero, and the static bias current increases from 21 to 30 μA when input increases from 1 to 5 V. Note that the tracking error depends on the input's slope and step size. Thus, the results shown in Fig. 7 do not cover all possible cases.

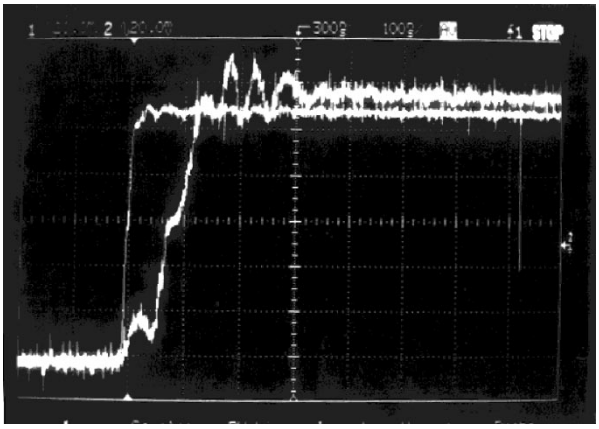

Fig. 6. Step response for small input signal.

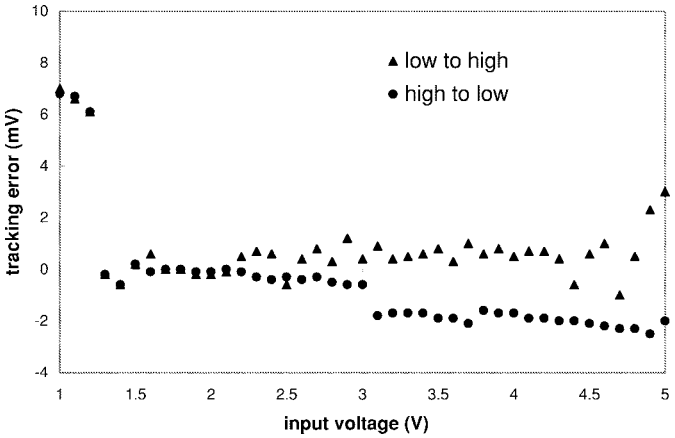

Fig. 7. Tracking error versus input voltage for output buffer.

IV. Conclusion

A compact, low static power class-B output buffer amplifier for driving a large capacitance load in flat-panel display is presented. The minimum voltage resolution of this buffer is decided by the comparator. Namely, it is the difference between the common-mode output voltage of the differential pair and the logic threshold voltage of the inverter INV1 divided by the voltage gain of the differential stage. The slew rate of the output buffer is decided by the transistor sizes of the output stage, supply voltage, and load capacitance. Because when the output transistor is turned on, it is fully turned on, the output transistor sizes are much smaller than those of class A and AB buffers. With these two parameters fixed, the bandwidth and bias current of the differential pair can be decided accordingly to obtain stable operation. An experimental prototype output buffer was implemented in a 0.8 μm CMOS technology. With 5 V supply voltage and 600 pF load capacitance, the measured static current is 24 μA; the maximum tracking error voltage is $\pm$7 mV; the output voltage swing is from 1 to 5 V. The settling time for 4 V swing to 0.2% is 8 μs, which is more than adequate for driving a 1280 $\times$ 1024 pixels LCD panel with an 86 Hz frame rate, which requires a settling time of less than 10 μs.

References

[1] Y. Takahashi *et al.*, "Multimedia projector using 720 $\times$ 480 pixel a-Si TFT-LCD's and a high-speed analogue driver LSI," *Displays: Technology & Application*, vol. 13, no. 1, pp. 5–30, Jan. 1992.

[2] C.-C. Wang, J.-C. Wu, and C.-M. Huang, "Data line driver design for a 10$''$ 480 $\times$ 640 $\times$ 3 color FED," in *Proc. 9th Int. Vacuum Microelectronics Conf.*, St. Petersburg, FL, July 1996, pp. 557–561.

[3] Hitachi Corp., *Hitachi LCD Controller/Driver LSI*, 1993.

[4] B. W. Lee and B. J. Sheu, "A high-speed CMOS amplifier with dynamic frequency compensation," in *Proc. IEEE CICC 1990*, New York, May 1990, pp. 8.4.1–8.4.4.

[5] R. C. Geiger, P. E. Allen, and N. R. Strader, *VLSI Design Techniques for Analog and Digital Circuits.* New York: McGraw-Hill, 1990.

[6] H. Khorramabadi, "A CMOS line driver with 80 dB linearity for ISDN applications," in *1991 Symp. VLSI Circuits Dig. Tech. Papers*, June 1991, pp. 75–76.

[7] F. C. Su, Unipac Optoelectronics Corp., private communication.