A New True-Single-Phase-Clocking BiCMOS Dynamic Pipelined Logic Family for High-Speed, Low-Voltage Pipelined System Applications

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***Abstract*— New true-single-phase-clocking (TSPC) BiCMOS/BiNMOS/BiPMOS dynamic logic circuits and BiCMOS/BiNMOS dynamic latch logic circuits for high-speed dynamic pipelined system applications are proposed and analyzed. In the proposed circuits, the bootstrapping technique is utilized to achieve fast near-full-swing operation. The circuit performance of the proposed new dynamic logic circuits and dynamic latch logic circuits in both domino and pipelined applications are simulated by using HSPICE with 1-μm BiCMOS technology. Simulation results have shown that the new dynamic logic circuits and dynamic latch logic circuits in both domino and pipelined applications have better speed performance than that of CMOS and other BiCMOS dynamic logic circuits as the supply voltage is scaled down to 2 V. The operating frequency and power dissipation/MHz of the pipelined system, which is constructed by the new clock-high-evaluate-BiCMOS dynamic latch logic circuit and clock-low-evaluate-BiCMOS (BiNMOS) dynamic latch logic circuit, and the logic units with two stacked MOS transistors, are about 2.36 (2.2) times and 1.15 (1.1) times those of the CMOS TSPC dynamic logic under 1.5-pF output loading at 2 V, respectively. Moreover, the chip area of these two BiCMOS pipelined systems is about 1.9 times and 1.7 times as compared with that of the CMOS TSPC pipelined system. A two-input dynamic AND gate fabricated with 1-μm BiCMOS technology verifies the speed advantage of the new BiNMOS dynamic logic circuit. Due to the excellent circuit performance in high-speed, low-voltage operation, the proposed new dynamic logic circuits and dynamic latch logic circuits are feasible for high-speed, low-voltage dynamic pipelined system applications.**

***Index Terms*—BiCMOS pipelined system, low-voltage BiCMOS dynamic logic circuits, true single-phase clocking (TSPC).**

I. Introduction

BiCMOS technology has been widely applied to the design of memories and high-performance very-large-scale integrated circuit (VLSI) logic due to its advantageous features of high speed, high driving capability, and low power dissipation [1]. In the design of conventional BiCMOS static logic circuits, extra PMOS devices should be used with NMOS devices to realize logic functions. As a consequence, the chip area is large, especially in complex logic. Also, both power dissipation and speed performance are degraded. This problem can be solved by using dynamic circuit techniques. The resulting BiCMOS dynamic logic circuits can retain the high-performance features of BiCMOS and have smaller chip area than the static circuits. Using the dynamic BiCMOS logic, high-speed BiCMOS pipelined circuits can be realized for various applications. They can also be used with CMOS pipelined logic to form an optimal pipelined logic system.

Recently, many BiCMOS dynamic logic circuits have been proposed [2]–[5]. In the BiCMOS dynamic logic circuits proposed in [2]–[4], the N-P domino circuit structure with alternatively connected N-cell and P-cell [6], [7] is adopted. But the high-speed pipelined operation is not considered. Moreover, these BiCMOS dynamic circuits require a true-two-phase clock signal, which increases clock design complexity and chip area. As the supply voltage is scaled down, the speed of some BiCMOS dynamic logic circuits [2], [3] is degraded significantly due to the $V_{\rm be}$ loss in the output voltage swing [8]. In the BiCMOS domino circuit proposed in [5], only a precharge high P-cell is used to form the domino circuit for 1.5-V operation. However, if the logic function is complex, especially for dynamic OR gate implementation, the speed performance of the proposed logic is degraded due to the use of the PMOS logic unit. Moreover, the pipelined system operation is not considered in [5].

In this work, new true-single-phase BiCMOS/BiNMOS/BiPMOS dynamic logic circuits [9] and BiCMOS/BiNMOS dynamic latch logic circuits for the design of BiCMOS pipelined logic circuits are proposed and analyzed. In the proposed new logic circuits, the true-single-phase clocking (TSPC) scheme is used so that the clock driving and distribution are simple and less chip area is occupied by clock lines [10]–[19]. Furthermore, the bootstrapping technique [4], [9], [20], [21] is used to obtain fast operation and near-full-swing output. It is shown that under 2-V operation, the new BiCMOS dynamic logic circuits and latch logic circuits, as well as the formed new pipelined logic circuits, have better speed performance than both conventional BiCMOS and CMOS design.

In Section II, the circuit structure and operational principle of the new BiCMOS/BiNMOS/BiPMOS dynamic logic circuits are described. The circuit structure of the new BiCMOS/BiNMOS dynamic latch logic circuits and design considerations of pipelined structure on the new circuits are also presented in Section III. In Section IV, the HSPICE simulation results are presented to verify the performance of

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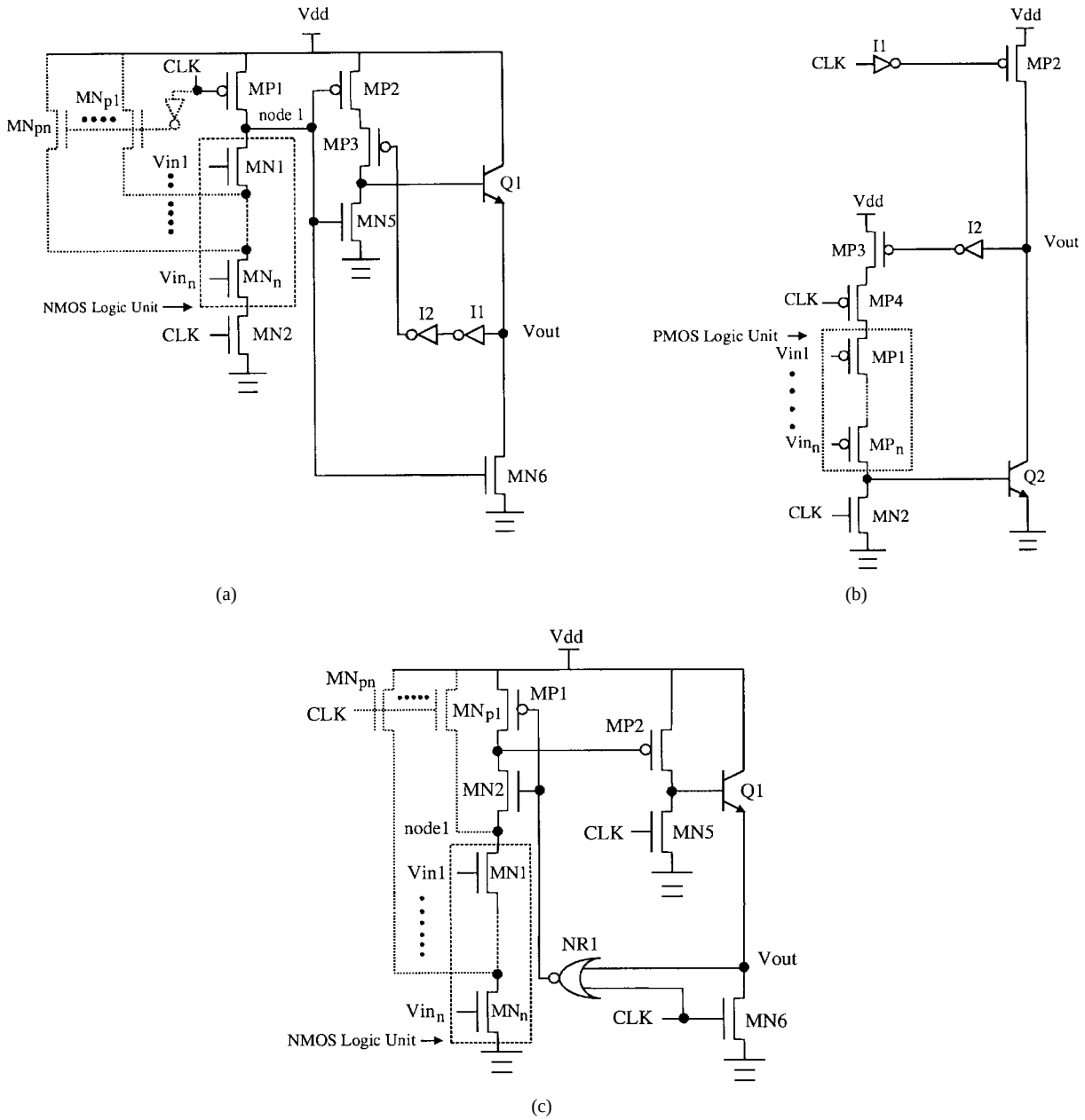


Fig. 1. The circuit structure of (a) the CHE-BiNMOS dynamic logic circuit, (b) the CLE-BiPMOS dynamic logic circuit, and (c) the CLE-BiNMOS dynamic logic circuit.

new BiCMOS dynamic logic circuits and BiCMOS/BiNMOS dynamic latch logic circuits. Comparisons to other BiCMOS and CMOS dynamic circuits are also made. Experimental results are demonstrated in Section V to further verify the performance of some proposed logic circuits. Conclusions are given in Section VI.

II. New TSPC BiCMOS Dynamic Logic

According to the circuit structure of the load driver, the proposed dynamic logic circuits in BiCMOS technology can be divided into two types, namely, BiNMOS/BiPMOS logic and BiCMOS logic. In BiNMOS/BiPMOS dynamic logic, the precharge-low (high) operation is performed by NMOS (PMOS) devices. In Fig. 1(a) and (b), the precharge-low (high) device is NMOSFET (PMOSFET), whereas the logic circuit is evaluated when the clock is high (low). Thus, it is called the clock-high (low)-evaluate-BiNMOS (BiPMOS) [CHE(CLE)-BiNMOS (BiPMOS)] dynamic logic. In Fig. 1(c), the precharge-low device is NMOSFET, whereas the logic circuit is evaluated when the clock is low and precharged low when the clock is high. Thus, it is called the clock-low-evaluate-BiNMOS (CLE-BiNMOS) dynamic logic. These circuits can be used to form the domino circuit where the precharge time is not critical. The CHE-BiNMOS and CLE-BiPMOS dynamic logic circuits can also be used in the pipelined structure where the output load of the pipelined logic gate is medium.

The operation of the CHE-BiNMOS dynamic logic circuit in Fig. 1(a) can be divided into two phases, namely, the precharge phase and the evaluation phase. During the precharge phase,

the clock is pulled low and node 1 is pulled high. Thus, MN6 is turned on, and the output is pulled down to the ground level. At the same time, the PMOS MP2 is turned off, whereas the NMOS MN5 is turned on. Thus, the excess minority charges in the base of Q1 are discharged and Q1 is turned off.

During the precharge phase, the internal-node precharge transistors MN_{p1} to MN_{pn} can be turned on to charge the internal nodes of the NMOS logic unit to V_{dd}–V_{tn}, where V_{tn} is the threshold voltage of NMOS transistors with the body effect. This nonfull-swing internal-node precharging technique [5], [9] is different from the conventional multiple precharging internal-node technique [22], which precharges the internal nodes to V_{dd} by PMOS transistors. Precharging to V_{dd}–V_{tn} can enhance the evaluation speed while avoiding the charge-sharing problem during the evaluation period.

In the evaluation phase with CLK high, MP1 is turned off, MN2 is turned on, and MP3 is still kept on by the precharge-low output signal through the two inverters I1 and I2. If all inputs to the NMOS logic unit are high, node 1 is pulled low to turn off MN5 and turn on MP2. Thus, Q1 is turned on to pull up the output voltage. This high output voltage makes the output of I2 high to turn off MP3. As a result, the base of Q1 is isolated from the circuit to confine the excess minority charge in the base. Due to the capacitive coupling between gate and drain of MP3 and between output node and base of Q1, the base voltage of Q1 can be bootstrapped up beyond V_{dd}, and thus, the output can be pulled up nearly to V_{dd} [4], [9]. Thus, the fast near-full-swing operation can be performed at a considerably higher speed than by using the feedback technique [3]. This bootstrapping technique [4], [9] has an operation voltage limit at 2 V [4]. As the supply voltage is reduced below 2 V, the CHE-BiNMOS dynamic logic circuit cannot achieve fast near-full-swing operation.

The operational principle of the CLE-BiPMOS dynamic logic circuit shown in Fig. 1(b) is described as follows. During the precharge phase, the clock is pulled high and MP2 is turned on by the inverter I1 to pull up the output to V_{dd}. At the same time, MP4 is turned off, whereas MN2 is turned on. Thus, the excess minority charge in the base of Q2 is discharged and Q2 is turned off. Note that the inverter I1 and MN2 should be optimized to make Q2 turned off before MP2 is turned on. Thus, the short-circuit current through MP2 and Q2 during the clock pull-high transition can be avoided.

In the precharge phase, MP4 is turned off by the clock signal to eliminate the dc power dissipation problem when all the inputs of the CLE-BiPMOS dynamic logic circuit are driven by logic-low signals during the precharge period in the pipelined system. If the CLE-BiPMOS dynamic logic circuit is adopted in the domino circuit structure as an internal gate, all the inputs of the CLE-BiPMOS dynamic logic circuit are precharged high by the previous stage. Thus, the PMOS MP4 can be removed to enhance the evaluation speed. As a result, this circuit is similar to that proposed in [5]. Moreover, the charge-sharing problem can be avoided by adding an NMOS predischarge transistor in the pulldown section where the drain node and the gate node of this NMOS transistor are connected to the base node of Q2 and the gate node of MP1, respectively, as discussed in [5].

In the evaluation phase with CLK low, MP2 and MN2 are turned off, whereas MP4 is turned on. The PMOS MP3 is still kept on by the precharged high output signal through the inverter I2. If all inputs to the PMOS logic unit are low, Q2 is turned on by the PMOS logic unit to pull down the output voltage. Since Q2 is driven from forward active region to saturation region, the output voltage can be driven to the ground level. Hence, the full-swing operation can be achieved. At the end of the output pulldown transition, MP3 is turned off by the inverter I2. Thus, the extra power dissipation after the pulldown transition can be avoided.

The CLE-BiNMOS dynamic logic circuit shown in Fig. 1(c) is suitable for domino circuit structure. The operational principle is described as follows. During the precharge phase, the clock is pulled high and the output voltage V_{out} is pulled down to the ground level. At this time, the output of the static CMOS NOR gate is low to turn on MP1, and thus, MP2 is turned off. In addition, MN5 is turned on, which discharges the base of Q1. Thus, Q1 is turned off. In addition, the internal-node precharge transistors MN_{p1} to MN_{pn} are turned on to charge node 1 and internal nodes of the NMOS logic unit to V_{dd}–V_{tn}. This can avoid the charge-sharing problem during the evaluation period.

In the evaluation phase with CLK low, MN6, MN5, and MN_{p1} to MN_{pn} are turned off, whereas MN2 is turned on by the NOR gate NR1 with two inputs low. If all inputs to the NMOS logic unit are high, MP2 is turned on and Q1 pulls up the output voltage. When the output voltage is high enough, the output of the feedback NOR gate NR1 is pulled low to turn on MP1 and turn off MN2. Thus, MP2 is turned off immediately. As a result, the base of Q1 is isolated from the circuit to confine the excess minority charges in the base. Similar to the operation of the CHE-BiNMOS dynamic logic circuit, the output voltage of the CLE-BiNMOS dynamic logic circuit can be pulled up close to V_{dd}.

The other type of proposed dynamic logic is called the BiCMOS dynamic logic circuit. Fig. 2(a) and (b) shows the clock-high-evaluate-BiCMOS (CHE-BiCMOS) [clock-low-evaluate-precharge-high-BiCMOS (CLEPH-BiCMOS)] dynamic logic circuit, which is evaluated during the clock high (low) period. When the CHE-BiCMOS logic in Fig. 2(a) is in the precharge phase, the clock is pulled low and MP5 is turned on. If the previous state of the output is high, MP4 is in the "on" state and MN3 is off because of the low feedback signal at the output of the inverter I1. Thus, Q2 is turned on to pull down output voltage. Since MP4 and MP5 provide a direct path from V_{dd} to the base node of Q2, the turn-on time of Q2 is short and the output voltage can be discharged rapidly. When output voltage is pulled low enough, MP4 is turned off and MN3 is turned on by the feedback inverter I1, and the base node of Q2 is discharged. Therefore, Q2 saturates transiently, and full-swing pulldown operation can be achieved. Other operations of the CHE-BiCMOS dynamic logic are the same as those of the CHE-BiNMOS dynamic logic circuit.

When the CLEPH-BiCMOS dynamic circuit of Fig. 2(b) is in the precharge phase, the clock is pulled high. At this time, MP5 is turned on, whereas MN3 is turned off by the inverter I1. If the previous state of the output is low, MP2 is in the "on" state. Thus, Q1 is turned on to pull up the output voltage.

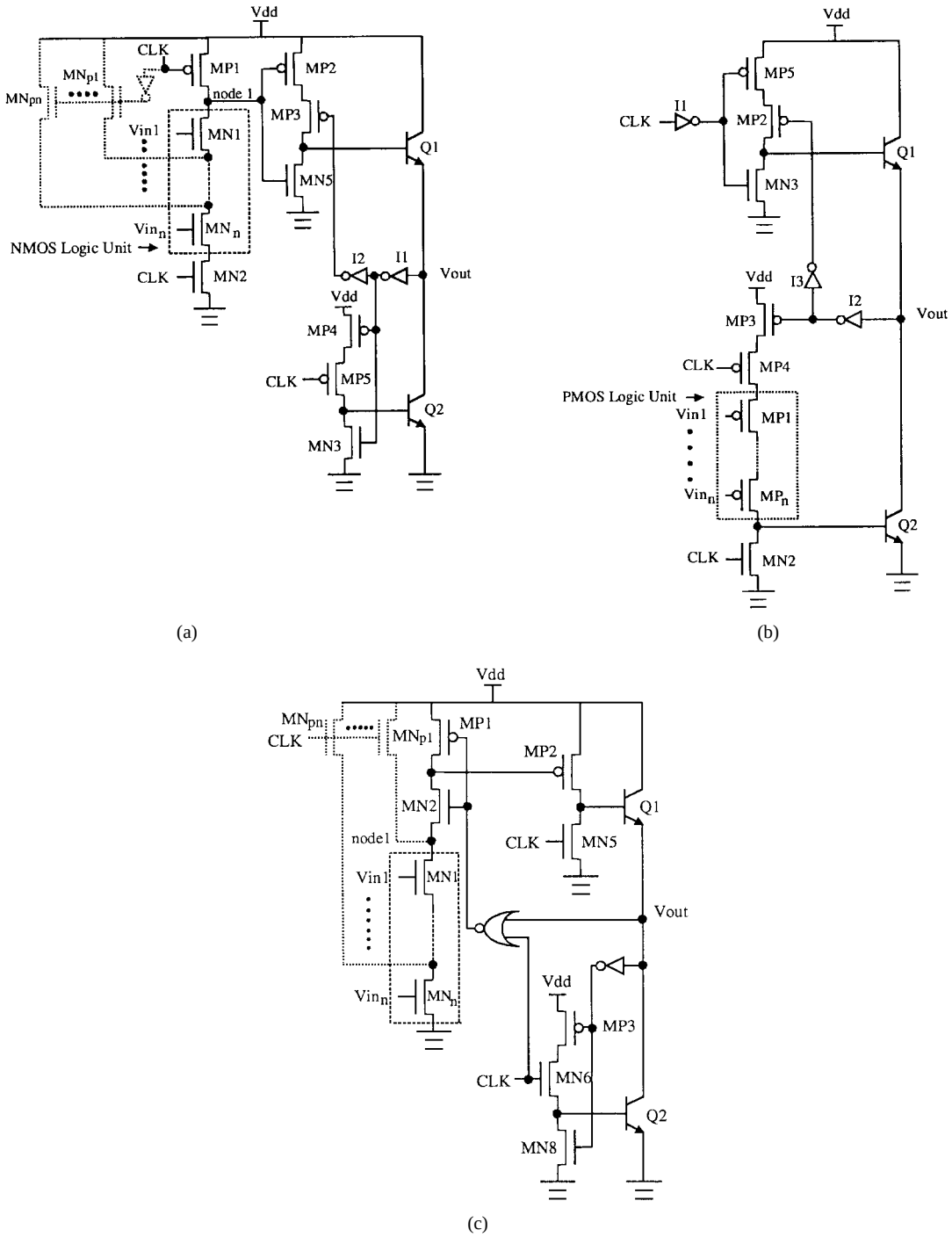


Fig. 2. The circuit structure of (a) the CHE-BiCMOS dynamic logic circuit, (b) the CLEPH-BiCMOS dynamic logic circuit, and (c) the CLE-BiCMOS dynamic logic circuit.

When the output voltage is high enough, MP2 is turned off by I3. As a result, the base node of Q1 is isolated from the circuit to confine the excess minority charge in the base. Similar to the operational principle of the CHE-BiCMOS/BiNMOS dynamic logic, the output voltage can be pulled up to nearly V_{dd}. In the evaluation phase of the CLEPH-BiCMOS logic, the operation is identical to the CLE-BiPMOS because they have identical pulldown circuits.

In the CLE-BiCMOS dynamic logic circuit of Fig. 2(c), the precharge-low operation when the clock is high is similar to that in the CHE-BiCMOS dynamic logic. In the evaluation phase of the CLE-BiCMOS dynamic logic, the operation is identical to the CLE-BiNMOS dynamic logic because they have identical pullup circuits.

Since the outputs of the proposed CHE-BiCMOS/BiNMOS and CLE-BiCMOS/BiNMOS (CLE-BiPMOS and CLEPH-BiCMOS) dynamic logic circuits are precharged to low (high) and they all use NMOS (PMOS) logic units, the CHE-BiCMOS/BiNMOS and CLE-BiCMOS/BiNMOS (CLE-BiPMOS and CLEPH-BiCMOS) dynamic logic circuits can

be cascaded directly to form the BiCMOS domino circuit systems.

III. New TSPC BiCMOS/BiNMOS Pipelined Logic

To develop a complete BiCMOS dynamic logic family for pipelined systems, three new BiCMOS/BiNMOS dynamic latch logic circuits that use an N-logic unit or a P-logic unit are proposed. The circuit diagram of the new BiCMOS dynamic latch logic with the N-logic unit is shown in Fig. 3(a), where the output data are evaluated when the clock is high. Thus, it is called the clock-high-evaluate-BiCMOS dynamic latch logic. In the precharge-and-hold phase, the clock is pulled low and MP1 is turned on to precharge the node 1 to $V_{\rm dd}$. Thus, MP2 is turned off and MN1 is turned on. Meanwhile, the output of the feedback NAND gate NA1 is high to turn off MP3 and turn on MN2. Thus, the bipolar transistor Q1 is turned off by MN1, whereas Q2 is turned off by MN2. Because both Q1 and Q2 are turned off, the output node holds the previous state. In the precharge-and-hold phase, the output voltage is held by the small-size CMOS static latch composed of the feedback inverters I2 and I3 to avoid charge leakage problems and increase noise immunity.

In the evaluation phase, the clock is pulled high. If the previous output state is high, the output of NA1 is pulled low to turn on MP3 and turn off MN2. Meanwhile, if at least one of the logic inputs is low, node 1 remains high and MN3 is still in the "on" state. In this case, Q2 is turned on to pull down $V_{\rm out}$ immediately. Since Q2 is driven from forward active region to saturation region, the output voltage can be driven to the ground level. Hence, the full-swing operation can be achieved. At the end of the output falling transition, node 2 is pulled up by NA1 and MP3 is turned off. This can eliminate the extra current from power supply through MN3, MP3, and Q2 to ground. Thus, the extra power dissipation after the pulldown transition can be avoided. In addition, MN2 is turned on to discharge the excess minority charges in the base of Q2, and thus, Q2 is turned off. On the other hand, if all logic inputs are high in the evaluation phase, node 1 is pulled down to the ground level to turn on MP2 and turn off MN3. Thus, Q2 remains in the "off" state and output voltage $V_{\rm out}$ still holds the previous high state.

In the evaluation phase, if the previous state is low, the output of NA1 is high and MP4 is turned on by the inverter I1 in the previous phase. If all logic inputs to the NMOS logic unit are high, node 1 is pulled down to the ground level to turn on MP2 and turn off MN1. Thus, Q1 is turned on to pull up the output voltage. When the output voltage is high enough, node 2 is pulled down by NA1 and MP4 is turned off by I1. As a result, the base node of Q1 is isolated from the circuit to confine the excess minority charge in the base. Similar to the operational principle of the CHE-BiCMOS/BiNMOS dynamic logic, the output voltage can be pulled up nearly to $V_{\rm dd}$. If at least one of the logic inputs is low, node 1 remains high. It can be analyzed similarly that both Q1 and Q2 are in the "off" state and the previous low output state is held.

The new BiCMOS dynamic latch logic with the P-logic unit is called the clock-low-evaluate-BiCMOS dynamic latch logic, as shown in Fig. 3(b), where I1 and I3 are small-size CMOS static latches. In the precharge-and-hold phase, the clock is pulled high. Thus, MP4 is turned off and MN3 is turned on. This turns off the bipolar transistor Q2. At the same time, MN1 is turned on to discharge node 1 to ground and turn off MN2. Also, MP2 is turned off by the clock signal. This makes the base node of Q1 in the floating state retain the "off" state of Q1 in the previous evaluation phase. Because both Q1 and Q2 are in the "off" state, the output node holds the previous state.

In the evaluation phase, the clock is pulled low. If the previous state is high, MP5 is on and MP3 is off. If all inputs to the PMOS logic unit are low, node 1 is pulled high to turn off MP1 and turn on MN2. Thus, the base node of Q1 is discharged and Q1 is turned off. At the same time, Q2 is turned on by the PMOS logic unit and the output voltage is pulled down to ground. Note that MN2 and both PMOS logic units in the pullup and pulldown sections should be optimized to make Q1 turned off before Q2 is turned on. Thus, the short-circuit current through Q1 and Q2 during the output pulldown transition can be avoided. At the end of the output pulldown transition, MP5 is turned off by the inverter I1. Thus, the extra power dissipation after the pulldown transition can be avoided. If at least one of the logic inputs is high, the precharge state is retained and the output holds the previous high state.

If the previous state is low in the evaluation period, MP3 is turned on by the inverter I2. If at least one of the logic inputs is high, node 1 remains low and the output is pulled up to nearly $V_{\rm dd}$ in a similar way as that in the CHE-BiCMOS dynamic latch logic circuit. On the other hand, if all inputs to the PMOS logic unit are low, node 1 is pulled up to turn off MP1. In addition, MN2 is turned on to keep Q1 in the previous off state. Thus, the output node holds the previous low state.

The pulldown part of the CLE-BiCMOS dynamic latch logic in Fig. 3(b) can be replaced by a simple NMOS device controlled by the node 1 voltage, as shown in Fig. 3(c). The circuit of Fig. 3(c) can implement a similar latched logic function as the CLE-BiCMOS dynamic latch logic and is called the CLE-BiNMOS dynamic latch logic.

There are two kinds of race problems in CMOS pipelined systems, namely, precharge race and clock-skew race [6]. The precharge operation of the conventional CMOS dynamic logic circuits under the slow-transition clock operation could lead to the precharge race, which results in the failure operation [24]. Fig. 4 shows HSPICE-simulated output voltages of both a CMOS TSPC dynamic logic circuit [23] and a new BiCMOS dynamic latch logic circuit under 45-ns clock slope. It is seen that the CMOS TSPC dynamic logic circuit cannot hold the output level due to the precharge race, whereas the new BiCMOS dynamic latch logic circuit can. Thus, the precharge-race immunity of the new circuit is improved.

Although the NAND gate NA1 in the CHE-BiCMOS dynamic latch logic circuit of Fig. 3(a) is driven by the clock signal and the output signal to control the node 2 voltage to achieve hold and pulldown operations, the clock-skew immunity is not degraded because the clock signal drives the evaluation device directly. Since the new BiCMOS dynamic latch logic uses the true-single-phase clock, the clock-skew

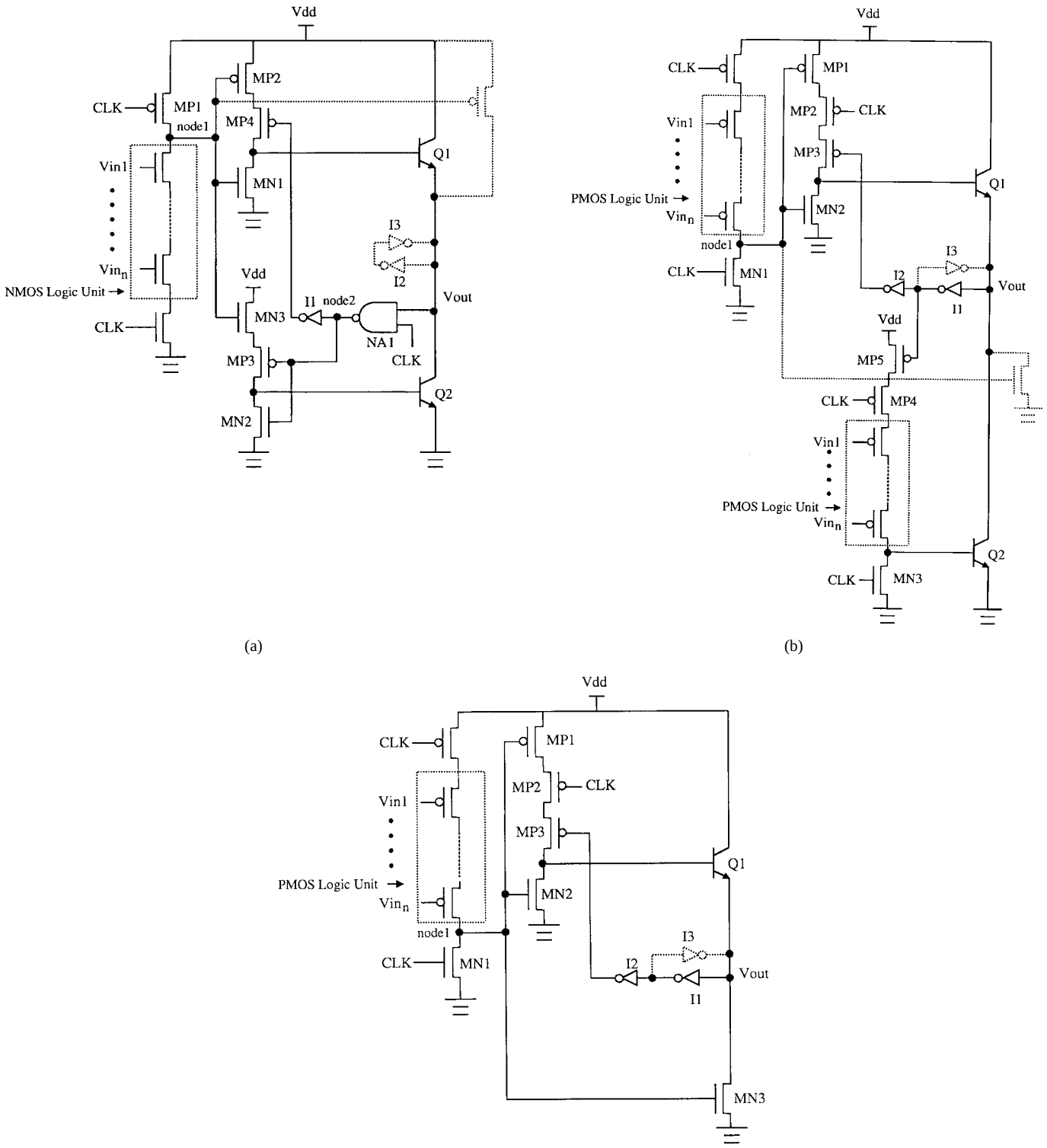


Fig. 3. The circuit structure of (a) the CHE-BiCMOS dynamic latch logic circuit, (b) the CLE-BiCMOS dynamic latch logic circuit, and (c) the CLE-BiNMOS dynamic latch logic circuit.

race can be avoided by using the same techniques as in the CMOS TSPC pipelined systems [23].

Generally, the BiCMOS TSPC pipelined system with the precharged dynamic circuit technique consists of two different types of pipelined sections, namely, CLK-HIGH section and CLK-LOW section. The two sections must be connected alternatively in the pipelined structure. In the CLK-HIGH section, the basic block is the CHE-BiCMOS dynamic latch logic circuit. Since the proposed BiCMOS dynamic logic is fully compatible with the CMOS dynamic logic, the basic block in the CLK-HIGH section can be the CMOS TSPC N-block [23] if the output load is not heavy. If more logic

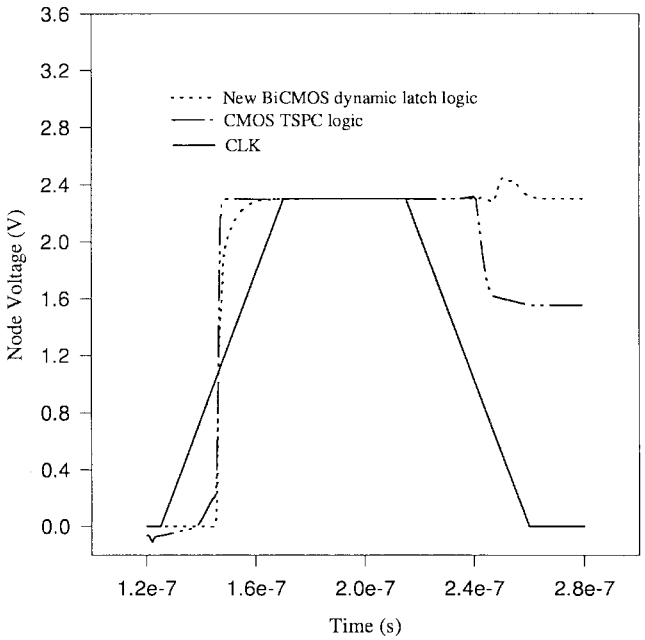


Fig. 4. HSPICE-simulated output waveforms of CMOS TSPC logic and new BiCMOS dynamic latch logic under 45-ns clock slope.

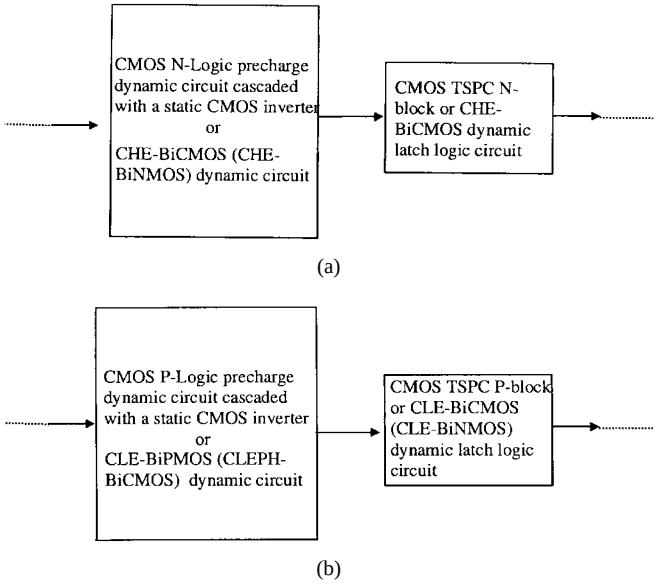


Fig. 5. The logic diagram of (a) CLK-HIGH section and (b) CLK-LOW section.

functions or more stages are to be implemented in the same section, CHE-BiCMOS or CHE-BiNMOS dynamic circuits as well as CMOS N-logic precharge dynamic circuits with output static inverter can be connected to the basic block, as shown in Fig. 5(a). When driven by CHE-BiCMOS, CHE-BiNMOS, or CMOS N-logic precharge dynamic circuits with output static inverter, the charge-sharing problem may occur in the CHE-BiCMOS dynamic latch logic, as in the case of CMOS TSPC dynamic circuits. This problem can be avoided by using the same techniques described in the previous section. Directly cascadable with CMOS dynamic circuits makes the BiCMOS pipelined system more flexible in delay with different capacitive load and achieving the optimal performance.

Similarly, the CLK-LOW section consists of CLE-BiCMOS (CLE-BiNMOS) dynamic latch logic circuit and CMOS TSPC P-block [23] as the basic block, which may be driven by CLE-BiPMOS (CLEPH-BiCMOS) dynamic circuit or CMOS P-logic precharge dynamic circuit cascaded with an output static CMOS inverter, as shown in Fig. 5(b). The charge-sharing problem of the CLE-BiCMOS (CLE-BiNMOS) dynamic latch logic circuit driven by other dynamic circuits can be avoided by using the same techniques as in the CLE-BiPMOS dynamic logic circuit.

The output dip phenomenon is a common problem for precharge circuits [23]. Such dips at the output nodes of the latches result in more power dissipation under heavy loading conditions. Thus, the dip problem of CHE-BiCMOS (CLE-BiCMOS) dynamic latch logic should be considered. During the precharge phase of CHE-BiCMOS dynamic latch logic, as shown in Fig. 3(a), node 1 is precharged high and MP3 is turned off by the NAND gate NA1. When the clock signal makes a low-to-high transition and the previous output state is high, MP3 is turned on by NA1 in the evaluation phase. If the pulldown delay at node 1 is shorter than that of NA1, Q2 remains in the "off" state and the output holds the previous high state. Thus, the dip phenomenon does not occur. It is found that if only one CHE-BiCMOS (CLE-BiCMOS) dynamic latch logic circuit is adopted in the CLK-HIGH (CLK-LOW) section, the dip phenomenon and, thus, its extra power dissipation can be avoided when the number of stacked MOS devices in the logic unit is smaller than three.

If more logic functions or more stages are to be implemented in the CLK-HIGH section, the pulldown delay at node 1 is equal to the total evaluation delay of the previous stages plus the pulldown delay of the logic unit in the CHE-BiCMOS dynamic latch logic. If the pulldown delay at node 1 is large enough, Q2 is turned on by MN3 and MP3 to pull down the output voltage below the logic threshold of NA1. Thus, MP4 can be turned on by the inverter I1, and the output voltage can be recovered by Q1 when the voltage at node 1 is pulled low.

If the pulldown delay is not large enough and the output voltage cannot be pulled down below the logic threshold of NA1 by Q2, MP4 is still in the "off" state. The output voltage level cannot be recovered. This will result in a failure operation. In this case, an extra PMOS transistor should be shunted with Q1 of the CHE-BiCMOS dynamic latch logic, as shown in Fig. 3(a), to solve this problem. The gate node of the PMOS device is connected to node 1. With the PMOS device, the output voltage can be recovered, and the resultant waveform of the dip phenomenon is shown in Fig. 6, where the unrecoverable output voltage of the latch logic without the PMOS device is also shown for comparison. Similarly, an extra NMOS transistor should be added to the CLE-BiCMOS dynamic latch logic, as shown in Fig. 3(b), to solve this problem.

To provide a design guideline in choosing new BiCMOS/BiNMOS/BiPMOS dynamic logic circuits or CMOS precharge dynamic circuits to form a BiCMOS pipelined system with optimal performance, the evaluation time of these dynamic circuits is minimized through optimal device

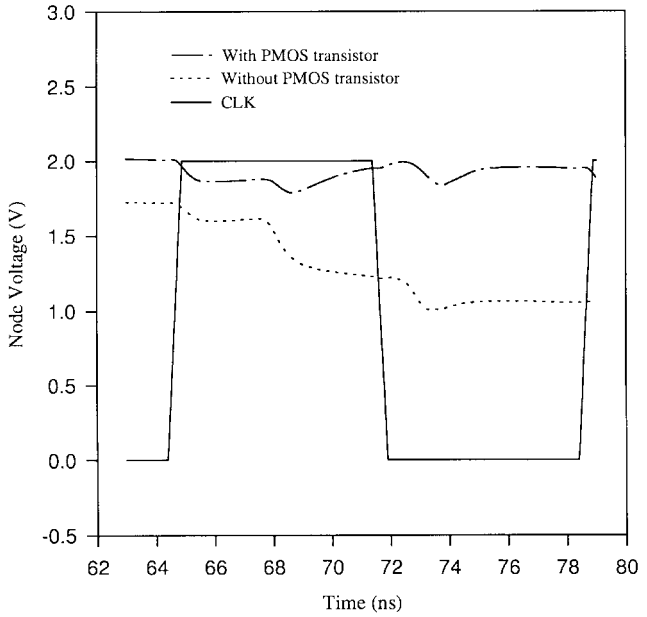
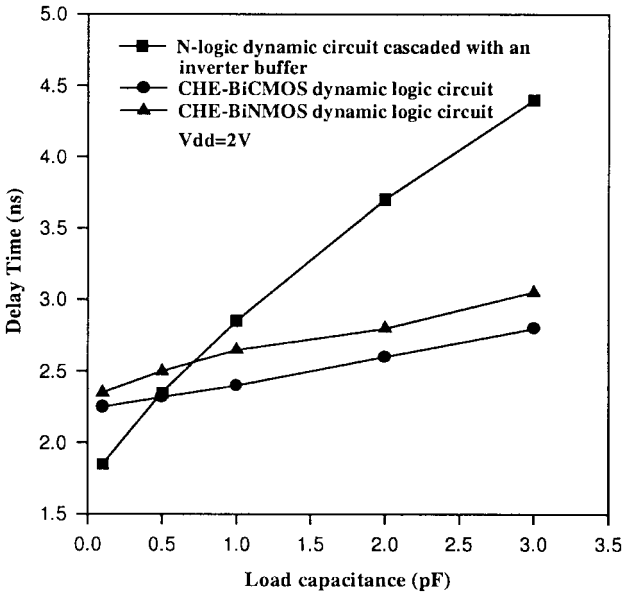


Fig. 6. HSPICE-simulated output waveforms of CHE-BiCMOS dynamic latch logic with and without PMOS transistor.

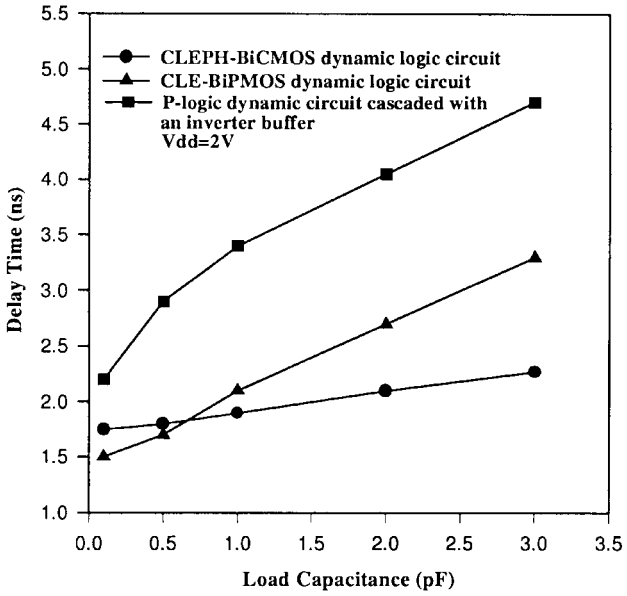
dimension design, and the precharge time is designed to be the same as the evaluation time. Then the delay times of the BiCMOS/BiNMOS/BiPMOS or CMOS dynamic circuits are compared. Fig. 7(a) shows the HSPICE-simulated delay times versus load capacitance for a CMOS N-logic precharge dynamic circuit with an output static CMOS inverter buffer, CHE-BiCMOS, and CHE-BiNMOS dynamic logic circuits, all with two stacked MOS devices in the logic unit. As may be seen from Fig. 7(a), if the load capacitance is smaller than 0.5 pF, the CMOS N-logic precharge dynamic circuit with an inverter buffer should be used to obtain a higher speed. It can also be seen that the average speed performance difference between CHE-BiCMOS dynamic logic and CHE-BiNMOS dynamic logic as the load capacitance increases from 0.5 to 3 pF is about 9%. Thus, if the delay time is critical, the CHE-BiNMOS dynamic logic circuit can be replaced by the CHE-BiCMOS dynamic logic circuit to achieve higher speed performance. Fig. 7(b) shows the HSPICE simulated delay times versus load capacitance for CMOS P-logic precharge dynamic circuit with an output static CMOS inverter buffer, CLEPH-BiCMOS, and CLE-BiPMOS logic circuits, all with two stacked MOS devices in the logic unit. The figure indicates that the CLEPH-BiCMOS and CLE-BiPMOS are faster than the CMOS P-logic precharge dynamic circuit under various output loadings. It can also be seen that if the load capacitance is smaller than 0.5 pF, the CLE-BiPMOS logic circuit should be used to obtain a higher speed.

IV. Performance Evaluation

The circuit performance of the proposed new BiCMOS dynamic logic circuits and the new BiCMOS pipelined circuits are simulated by using HSPICE with the Berkeley Short-Channel IGFET Model (BSIM) [25] for MOS transistors. Moreover, the performance of the proposed BiCMOS dynamic logic circuits and BiCMOS pipelined circuits are



(a)



(b)

Fig. 7. HSPICE-simulated gate-delay times versus load capacitance at $V_{dd} = 2$ V.

compared with CMOS TSPC dynamic circuits and other BiCMOS domino logic gates proposed in [3]–[5].

In the simulation of the BiCMOS domino logic in [3] and [4], the average evaluation delay times and the average power dissipation are extracted from the gate chain formed by alternately connecting the N-cell and the P-cell. The evaluation delay time versus load capacitance of the CLE-BiNMOS dynamic logic with three stacked MOS transistors in the logic unit are shown in Fig. 8, where the data of other BiCMOS domino gates are also presented. It can be seen that the speed performance of the CLE-BiNMOS and CLE-BiCMOS domino logic gates are higher than that of the other domino logic circuits as the output loading is beyond 0.5 pF at 2 V. It can also be seen that the evaluation speed of the CLE-BiCMOS

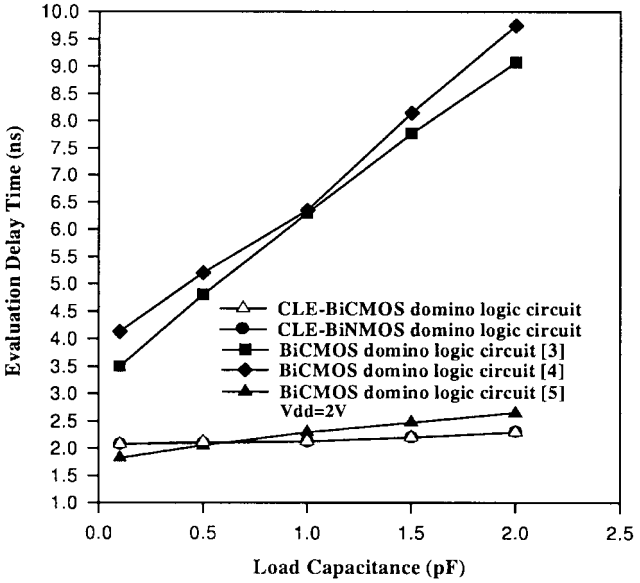


Fig. 8. HSPICE-simulated gate-evaluation delay times versus load capacitance for various domino circuits at $V_{dd} = 2$ V.

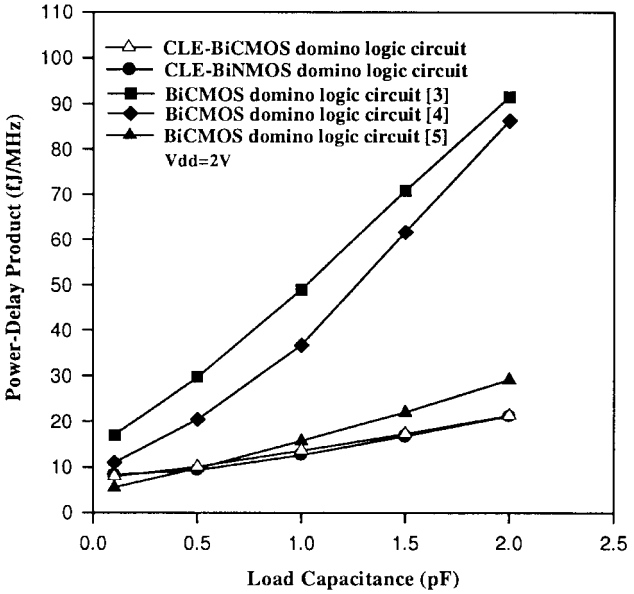


Fig. 10. HSPICE-simulated power-delay product versus load capacitance for various domino circuits at $V_{dd} = 2$ V.

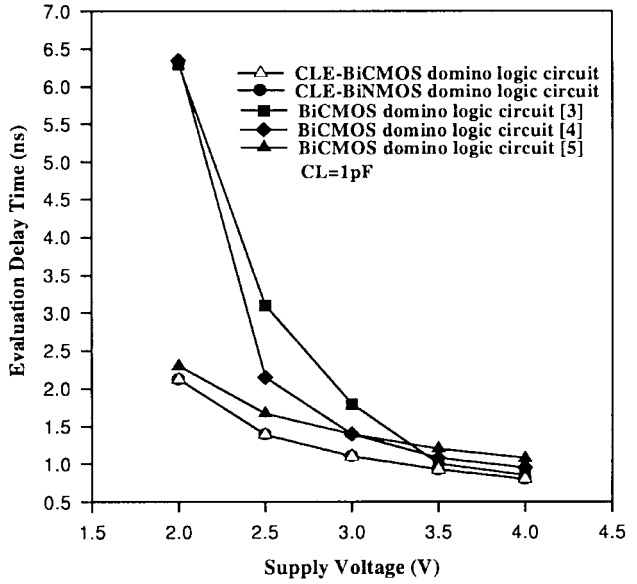


Fig. 9. HSPICE simulated gate-evaluation delay times versus supply voltage for various domino circuits under 1-pF load capacitance.

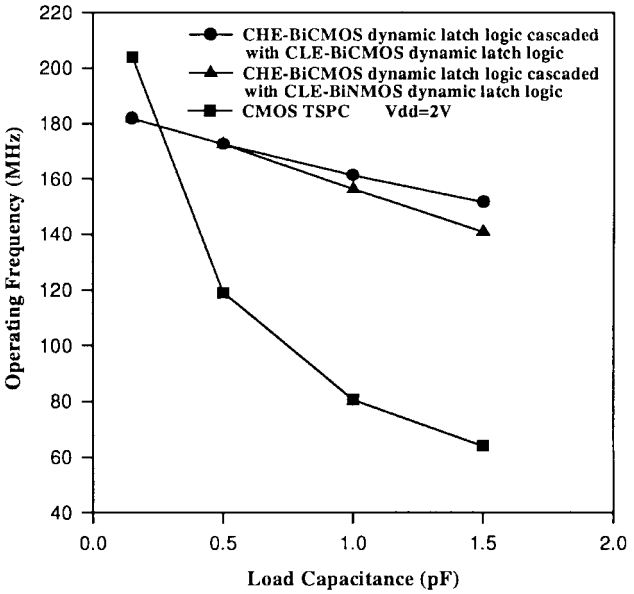


Fig. 11. HSPICE-simulated operating frequency versus load capacitance at $V_{dd} = 2$ V.

domino logic is nearly equal to that of the CLE-BiNMOS domino logic because they have the same evaluation circuit structures. Fig. 9 shows the evaluation delay times versus supply voltage. It can be seen that the CLE-BiNMOS and CLE-BiCMOS domino logic circuits have a smaller delay than other BiCMOS domino logic circuits as the supply voltage is scaled down from 4 to 2 V.

Fig. 10 shows the power-delay product versus load capacitance. As seen from Fig. 10, the power-delay product of the CLE-BiNMOS dynamic logic gates is smaller than that of other BiCMOS domino gates when the output loading is beyond 0.5 pF.

The operating frequency versus load capacitance of the BiCMOS dynamic pipelined system, which is constructed by the new BiCMOS dynamic latch logic circuits with two stacked MOS transistors in the logic unit, is shown in Fig. 11, where the data of a CMOS TSPC dynamic circuit are also presented. The rise/fall time of the clock signal is 0.5 ns. It can be seen from Fig. 11 that the operating frequency of the pipelined system, which is constructed by CHE-BiCMOS dynamic latch logic and CLE-BiCMOS (BiNMOS) dynamic latch logic, is smaller than that of the CMOS TSPC under 0.15-pF load capacitance. However, under 0.5- and 1.5-pF load capacitances, the operating frequencies of the BiCMOS dynamic pipelined system with CLE-BiCMOS (BiNMOS) dynamic latch logic at 2-V supply voltage are 172.4 (172.4) and 151.5 (140.8) MHz, while the power dissipations per megahertz are 9.99 (9.49) and 16.88 (16.22) μW/MHz, respec-

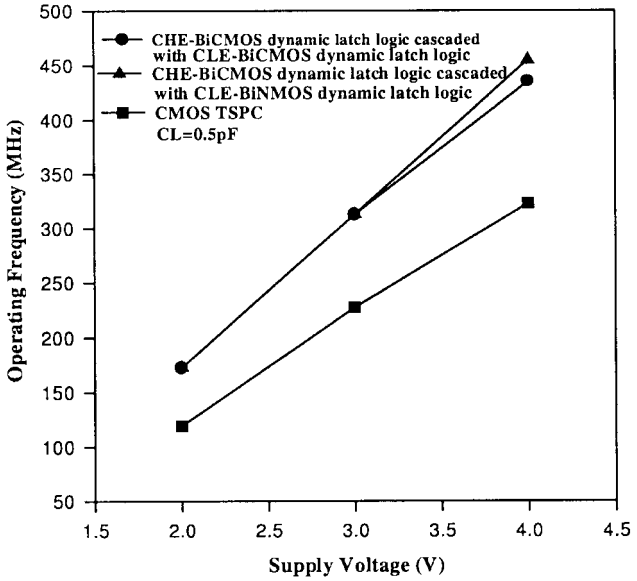


Fig. 12. HSPICE-simulated operating frequency versus supply voltage under 0.5-pF load capacitance.

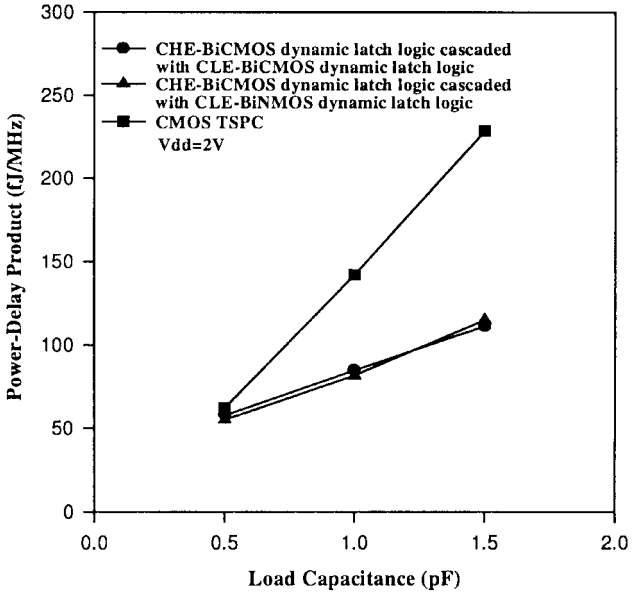


Fig. 13. HSPICE-simulated power-delay product versus load capacitance at $V_{dd} = 2$ V.

tively. They are about 1.45 (1.45) times and 2.36 (2.2) times the operating frequency, as well as 1.34 (1.28) times and 1.15 (1.1) times the power dissipation in the CMOS TSPC dynamic pipelined system, respectively, where the CMOS parameters are extracted from 1-μm BiCMOS technology.

It can be seen from Fig. 11 that when the output loading is larger than 0.5 pF, the operating frequency of the pipelined system that is constructed by CHE-BiCMOS dynamic latch logic and CLE-BiCMOS dynamic latch logic is higher than that of the pipelined system, which is constructed by CHE-BiCMOS dynamic latch logic and CLE-BiNMOS dynamic latch logic. This is because the pulldown driving capability of the NMOS device in the CLE-BiNMOS dynamic latch logic is smaller than that of the bipolar device in CLE-BiCMOS dynamic latch logic under heavy loading conditions. Thus, the new CLE-BiCMOS dynamic latch logic is suitable for heavy loading pipelined operation. As the device technology is scaled down to the deep submicrometer range, it is expected from the above analyses that the speed advantages of new BiCMOS pipelined systems can be maintained if the bipolar device is suitably scaled.

Fig. 12 shows the operating frequency versus supply voltage. The figure indicates that the operating frequency of the BiCMOS dynamic pipelined system is faster than that of CMOS TSPC under various supply voltages. Moreover, as the supply voltage is scaled down from 4 to 2 V, the operating frequency of the BiCMOS dynamic pipelined system is about 1.4–1.45 times the operating frequency in the CMOS TSPC pipelined system under 0.5-pF output loading.

The power-delay product versus load capacitance of the new BiCMOS dynamic latch logic circuits and CMOS TSPC dynamic circuits is shown in Fig. 13, where the delay time is defined as 1/(clock frequency). As seen from Fig. 13, the power-delay product of BiCMOS dynamic pipelined systems constructed by CHE-BiCMOS dynamic latch logic cascaded with CLE-BiCMOS (BiNMOS) dynamic latch logic is smaller than that of the CMOS TSPC pipelined system as the load capacitance increases from 0.5 to 1.5 pF.

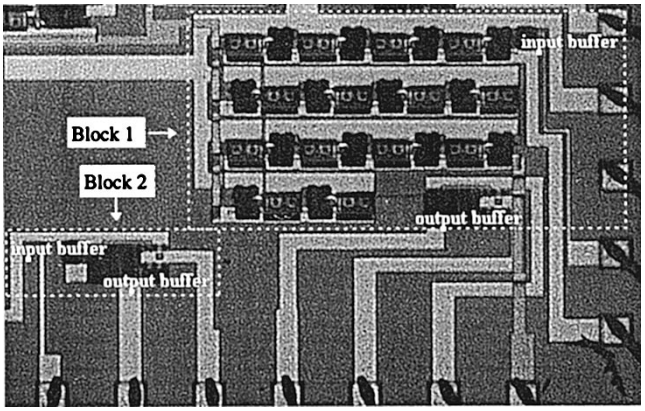


Fig. 14. Microphotograph of the experimental chip.

The chip area of the new BiCMOS pipelined system is also compared with the CMOS TSPC pipelined system. Under 1.5-pF load capacitance, the area of the pipelined system constructed by CHE-BiCMOS dynamic latch logic circuit cascaded with CLE-BiCMOS (BiNMOS) dynamic latch logic circuit, and the logic units with two stacked MOS transistors, is about 1.9 (1.7) times that constructed by the CMOS TSPC dynamic logic.

V. Experimental Results

To experimentally evaluate the performance of the new BiCMOS/BiNMOS dynamic logic gates, an experimental chip is designed by using a 1-μm double-poly, double-metal BiCMOS process. The minimum gate length of NMOS and PMOS devices are 1 and 1.2 μm, respectively. The threshold voltages of NMOS and PMOS devices are 0.7 and -0.8 V, respectively. Fig. 14 shows the microphotograph of the experimental chip, which consists of two blocks. In Block 1, a logic gate chain

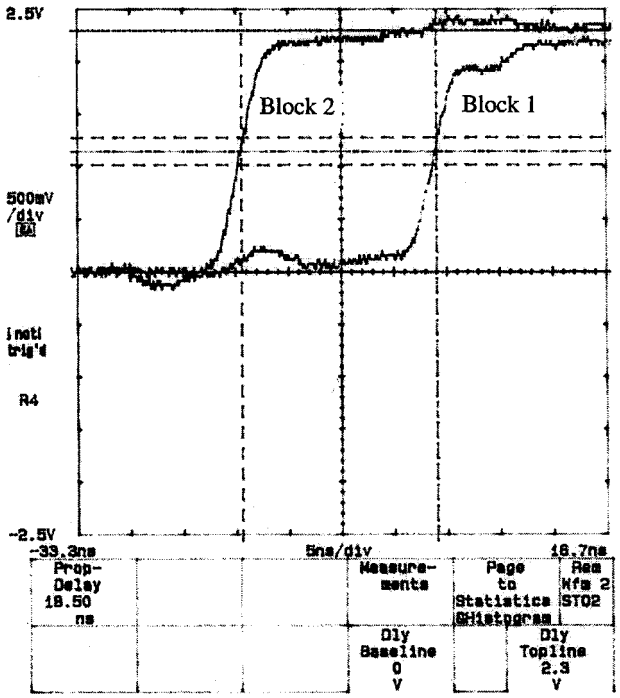


Fig. 15. The two measured output waveforms of Block 1 and Block 2 driven by the same input voltage waveform at 2.3 V.

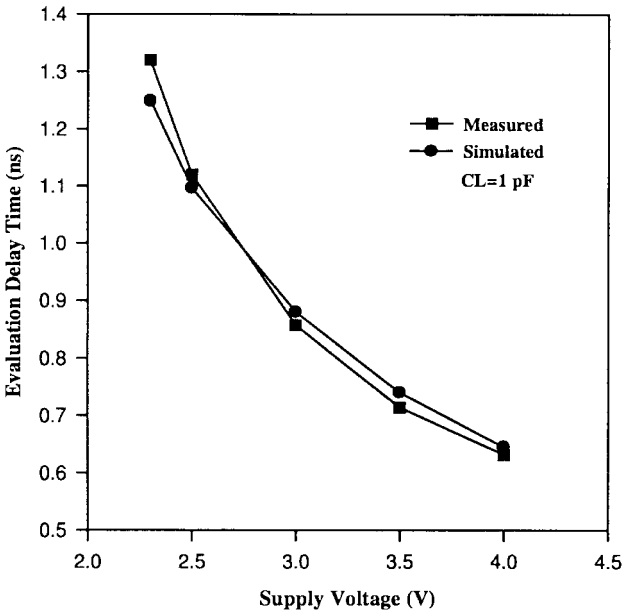


Fig. 16. The measured evaluation delay time of the CLE-BiNMOS dynamic two-input AND gate versus supply voltage under 1-pF load capacitance.

constructed by 14 stages of the CLE-BiNMOS dynamic two-input AND gates with 1-pF output load capacitance in each stage. The input of the logic gate chain is connected to the input buffer, whereas the output is connected to the output buffer. Block 2 is formed by cascading the input buffer to the output buffer directly. Fig. 15 shows the two measured output waveforms of Block 1 and Block 2 driven by the same input voltage waveform. The delay time between these two waveforms is equal to the evaluation delay time of the fabricated 14 stages of CLE-BiNMOS dynamic logic. It can be seen from Fig. 15 that the evaluation delay time of the CLE-BiNMOS is 1.32 ns at 2.3 V. The power dissipation of a gate at 2.3 V is 9.26 μW/MHz. Fig. 16 shows the measured and simulated evaluation delay time versus supply voltage of the fabricated CLE-BiNMOS dynamic two-input AND gate with 1-pF load capacitance. The figure indicates that the experimental results coincide with the simulation results. This verifies the low-voltage performance of the CLE-BiNMOS dynamic logic circuits.

VI. Conclusion

In this paper, new BiCMOS/BiNMOS/BiPMOS dynamic logic and new BiCMOS/BiNMOS dynamic latch logic for pipelined system applications have been proposed and analyzed. The proposed circuits are race free and use a true-single-phase clocking scheme. Some common problems related to the pipelined logic circuits under low-voltage operation such as full-swing output, charge redistribution, clock slew rate, and clock skew have been overcome or improved upon in the proposed BiCMOS dynamic pipelined logic circuits. The speed performance of the new BiNMOS dynamic logic circuit under low-voltage operation has been verified by both simulation results and experimental results. In the future, more applications on the proposed BiCMOS dynamic pipelined logic circuits will be explored.

Acknowledgment

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