Novel Contact Hole Fabrication Using Selective Liquid-Phase Deposition Instead of Reactive Ion Etching

Ching-Fa Yeh, Chien-Hung Liu, and Jwinn-Lein Su

***Abstract*— This work forms a contact hole utilizing the selectively liquid-phase deposited (S-LPD) silicon-oxide technique instead of the conventional reactive ion etching (RIE). The n^+/p junction diode with contact hole formed by S-LPD exhibits one order less reverse current, larger forward current, smaller ideality factor, and better thermal stability than that formed by RIE. The Schottky junction with S-LPD contact hole also possesses several excellent characteristics, including ideality factor, reverse current and barrier height, even without sintering treatment. These characteristics confirm the effectiveness of S-LPD technique in replacing conventional RIE to form contact holes, particularly for the ultra-shallow junction in future.**

***Index Terms*— Liquid-phase deposition.**

I. Introduction

REACTIVE ION ETCHING (RIE) is widely employed to form contact holes owing to its anisotropic etching ability. However, RIE easily causes surface damage [1], [2] and contamination [3], [4]. RIE also causes radiation damage, resulting in the generation of fixed charge and SiO_2/Si interface trap [5]–[7]. In addition, RIE selectivity issue has become increasingly critical in ultra-shallow junction, because overetch is less allowed. To avert these problems, an alternative method without etching is urgently required to replace conventional RIE method. According to our previous investigations, the liquid-phase deposition (LPD) method can selectively deposit silicon oxide against photoresist in half-micron process if the condition of hydro-fluorosilicic acid solution is adequately controlled [8], [9]. This technique has also been applied to form the interlayer dielectric (ILD) in multilevel interconnect [10] and asymmetry LDD spacer structures [11]. These studies reveal the possibility of applying S-LPD to the deep submicron process. In this work, we apply S-LPD to form contact holes in n^+/p and Schottky diodes. The superiority of applying S-LPD over conventional RIE is demonstrated by comparing the current–voltage (I–V) characteristics of prepared junction diodes.

II. Experimental

The S-LPD process and its mechanism have been described in our previous literature [8], [12]. Fig. 1 shows the S-LPD process window, which is the function of silicic acid $Si(OH)_4$ concentration and solution temperature. In this work, we mainly performed S-LPD in the solution of $Si(OH)_4$ concentration of 7.3×10^{-3} mol/L at 23 °C. The SEM photograph in Fig. 1 inset shows the oxide is selectively deposited against photoresist. This also indicates the feasibility of applying S-LPD to half-micron meter contact holes and the capability to form the holes of high aspect-ratio.

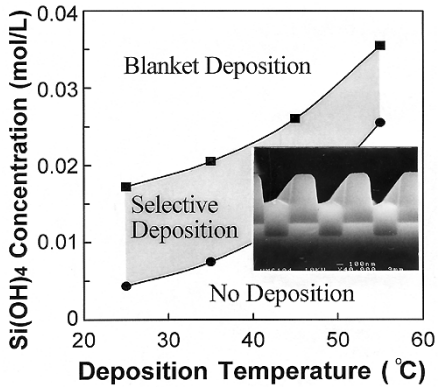

Fig. 1. Process window and SEM photograph for S-LPD.

The P-type (100) wafers with 15–25 Ω-cm resistivity are adopted herein. Following formation of the channel stopper and field oxide, phosphorus with dose of 5×10^{15} cm^{-2}, and energy of 40 keV is implanted to make n^+/p junction. As the left side of Fig. 2 indicates, for S-LPD samples, the photoresist on the site of contact hole region is first patterned and, then, the LPD oxide is selectively grown on the region without photoresist. After S-LPD, the photoresist is removed by using H_2SO_4/H_2O_2 mixed solution, and the contact holes are automatically formed. For RIE samples, as shown in the right side of Fig. 2, LPD oxide is globally deposited all over the wafers and, then, the contact holes are formed by using RIE through lithography photoresist patterns. Herein, a partial RIE method is adopted to buffer the damage generation attributed to RIE. Such an application suggests that the 85% oxide is etched by RIE (CF_4 gas: 5 sccm; 50 mtorr; rf power: 100 W) and, then, the remaining 15% oxide is etched by wet-etching in BHF solution. After standard RCA cleaning [13] for contact holes, metallization is performed, and then sintering is performed for some samples at 400 °C, 30 min in N_2. For Schottky junction diodes, the N-type (100) wafers with 1–5 Ω-cm resistivity are adopted. Their fabrication procedures

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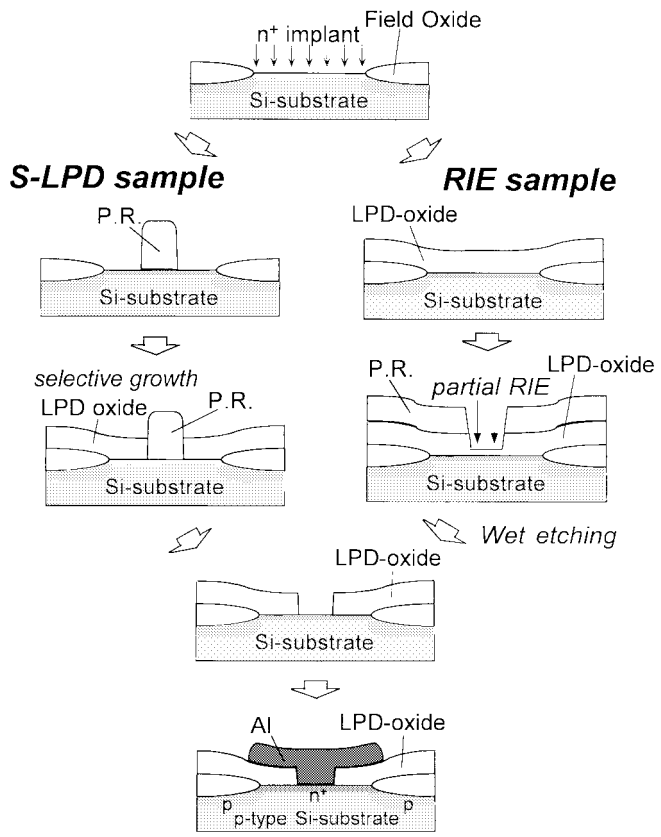

Fig. 2. Process-flow diagram of n^+/p junction diode with contact hole fabricated by S-LPD (left) or conventional RIE (right).

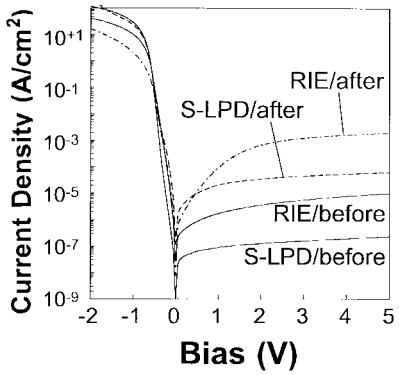

Fig. 3. Comparison of I–V characteristics between n^+/p diodes with S-LPD and RIE contact holes (junction area: 100 μm × 100 μm contact area: 60 μm × 60 μm), before and after sintering for 30 min at 400 °C in N_2.

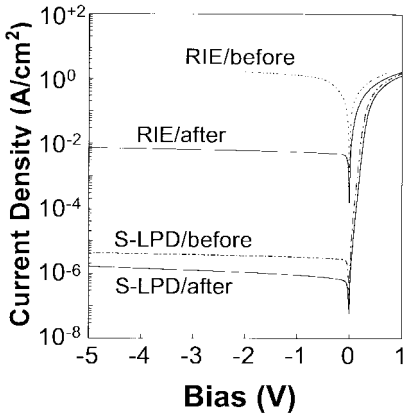

Fig. 4. Comparison of I–V characteristics between Schottky diodes with S-LPD and RIE contact holes (contact area: 500 μm × 500 μm), before and after sintering for 30 min at 400 °C in N_2.

closely resemble those of n^+/p junction diodes except for no ion-implantation process. For both n^+/p and Schottky junction diodes with contact holes prepared by S-LPD or RIE method, the I–V characteristics are investigated and compared.

III. Results and Discussion

Fig. 3 compares typical I–V characteristics before/after sintering between n^+/p diodes with contact holes fabricated by S-LPD and RIE, respectively. Before sintering, for S-LPD sample the reverse current at 5 V reverse bias is one order smaller than that for RIE sample. The ideality factor η of S-LPD and RIE sample in the forward bias $-0.4 \sim -0.5$ V is 1.11 and 1.64, respectively. Above results imply that extremely few G-R centers exist in S-LPD sample, but many exist in RIE sample. Otherwise, the S-LPD samples also exhibit larger forward current at forward bias >1.0 V, especially after sintering. This finding indicates that a smaller series resistance arises in the neutral region and a smaller contact resistance R_c exists in contact region for S-LPD diodes. We have found that the R_c, measured with Kelvin resistor, of S-LPD sample is about one-half to one-tenth of RIE sample for different contact sizes [14]. According to a previous investigation, on the Si surface RIE easily induces bonding defects, subsequently inducing donor-like charge states [15]. These states serve as G-R centers and increase reverse current if they locate near the band-gap center. As Fig. 3 depicts, after sintering, the reverse current of RIE sample further increases, i.e., significantly more than that of S-LPD sample. This attributes to that a lot of RIE related impurities and defects have diffused from Si surface into depletion region. Relatively the S-LPD samples exhibit a good thermal stability. Another investigation reported that the fluorine-contained ion bombardment and permeation, i.e., inevitable in RIE process, enlarge the reverse current and cause the soft breakdown [16]. Even if the partial RIE is adopted, some energetic ions or radicals can still penetrate the 15% remaining oxide into Si substrate. Particularly at contact periphery, the microtrenching effect [17] due to ion reflection from the photoresist sidewall can enhance more serious penetration. However, these problems never occur in the S-LPD diodes and, therefore, more ideal I–V characteristics are observed.

We further investigate the Si near-surface region by using Schottky diodes to show the superiority of utilizing S-LPD because this region can be simulated as the ultra-shallow junction. Fig. 4 compares typical I–V characteristics between Al/n–Si Schottky diodes with contact holes prepared by partial RIE and S-LPD, respectively. Before sintering, RIE sample nearly loses the rectifying characteristics of Schottky diode under reverse bias, but S-LPD sample exhibits satisfactory Schottky characteristics. However, after sintering, the S-LPD sample still exhibits about four order smaller than the RIE

sample in reverse current; meanwhile the ideality factor 1.03 of the former is also lower than 2.03 of the latter. This finding reveals that the sintering is necessary for the RIE sample to release a part of residues and defects from the Si surface, but unnecessary for the S-LPD sample. For RIE Schottky diode, the worse ideality can be attributed to the large surface recombination velocity [18]. According to the curve slope of $\ln\{I/[1-\exp(-qV/kT)]\}$ versus forward-bias voltage, the potential barriers is 0.83 and 0.6 eV for S-LPD and RIE Schottky diode, respectively. As mentioned earlier, the donor-like bonding defects and the polymer residues make the depletion region thinner [19] and the potential barrier lowering. The barrier lowering effect seriously degrades both reverse and forward I–V characteristics. Above results imply that RIE will be increasingly critical and requires more severe after-RIE-treatment [20] in ultra-shallow junction. However, utilizing S-LPD can avert these problems, and is expected to be a highly promising candidate as novel contact hole technology.

IV. Conclusion

This work successfully employs a novel selective-LPD method to prepare contact holes for the n^+/p diodes and the Schottky diodes. Compared to the RIE samples, the S-LPD samples exhibits much smaller reverse current, larger forward current, better ideality factor and better thermal stability. In contrast, the conventional RIE technology cannot be utilized in damageless contact-hole formation. The S-LPD technique is highly promising to replace conventional RIE for contact hole formation. In general, S-LPD method doesn't damage and contaminate the device surface; thus, no additional treatment is required. Therefore, the novel S-LPD technology can be applied to ultra-shallow junction and deep submicron process in the near future.

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