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Thin-Film Properties and Barrier Effectiveness of Chemically Vapor Deposited Amorphous WSi_x Film

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ABSTRACT

Thin-Film properties and barrier effectiveness against copper (Cu) diffusion of a thin amorphous WSi_x layer were investigated. The amorphous WSi_x layer was deposited by the chemical vapor deposition (CVD) method using the SiH_4/WF_6 chemistry with the activation energy determined to be 3.0 kcal/mol. The CVD-WSi_x film has a low film stress, low electrical resistivity, and excellent step coverage. The resistivity of the amorphous CVD-WSi_x layer increases with the deposition temperature, but the residual stress of the layer decreases with the deposition temperature. The WSi_x/Si structure is thermally stable up to at least 600°C, while the copper-contacted Cu/WSi_x/Si structure with a 50 nm thick WSi_x barrier is stable only up to 550°C. Moreover, the Cu/WSi_x/p^+-n junction diodes can sustain a 30 min thermal annealing up to 500°C without causing degradation in electrical characteristics. Barrier failure of the WSi_x layer in the Cu/WSi_x/Si structure at temperatures above 550°C is attributed to Cu atoms diffusion via fast paths in the WSi_x layer. These fast paths were presumably developed from grain growth of the WSi_x layer and/or thermal-stress-induced weak points in the WSi_x layer.

Introduction

As the interconnect linewidth shrinks continuously to deep-submicron dimensions, Al metallurgy becomes inadequate owing to its poor electromigration resistance; in addition, the resistivity of Al alloys is higher than desired for fast integrated circuits (ICs). Therefore, other metals with lower resistivity and superior electromigration resistance have been extensively studied.[1-3] Copper (Cu) has a lower resistivity than aluminum (Al) and it has an excellent electromigration resistance. Moreover, Cu can be deposited by chemical vapor deposition (CVD).[4-6] However, Cu diffuses fast in Si substrate and forms Cu-Si compounds at low temperatures (about 200°C),[7,8] causing deep-level traps in Si.[7] Moreover, Cu adheres poorly to dielectric layers and drifts through oxide under field acceleration.[9,10] Therefore, a diffusion barrier between Cu and its surrounding layers is considered a prerequisite for Cu to be useful in silicon based IC applications.

Although many studies have shown that the sputter-deposited amorphous materials are very effective barriers for Cu metallization due to the absence of grain boundaries,[11-13] it is difficult to deposit metal barriers with acceptable conformity in submicron contact holes using the sputter deposition method. In contrast, CVD generally offers a much better conformal deposition than the physical vapor deposition (PVD) method; therefore, there is increasing interest in depositing amorphous barriers by CVD. Chemically vapor deposited silicon-rich (Si/W atomic ratio larger than 2.0) WSi_x layers used in polycide application has been extensively investigated using either SiH_4/WF_6[14-21] or SiH_2Cl_2/WF_6 chemistry.[22-25] However, no study has been made on metal-rich (Si/W atomic ratio less than 2.0) WSi_x layers with respect to their barrier effectiveness against Cu diffusion.

In this study, film properties and barrier effectiveness of thin, amorphous, metal-rich WSi_x layers were investigated using electrical measurement as well as material analysis. The amorphous WSi_x layers were deposited by low-pressure chemical vapor deposition (LPCVD) using SiH_4 reduction of WF_6. We evaluated the barrier capability of the amorphous WSi_x layers for Cu metallization using a structure of Cu/WSi_x/p^+-n junction diodes. Stability of the unpatterned samples of Cu/Si, WSi_x/Si, and Cu/WSi_x/Si structures was also investigated. The electrical measurement is believed to be a much more sensitive technique for barrier-failure detection than the material analyses, while the material analyses can provide microscopic information of material change, which is helpful to the understanding of failure mechanisms of the barrier layers. The results of this study may be useful for the integration of the amorphous WSi_x in Cu metallization applications.

Experimental

The thermal stability of barrier layers was evaluated by measuring leakage current of thermally annealed Cu/bar-

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rier/p^+-n junction diodes. The starting materials for the diodes fabrication were 4 in., (100)-oriented, n-type silicon wafers with 4-7 Ω cm nominal resistivity. After RCA standard cleaning, the wafers were thermally oxidized to grow a 500 nm oxide layer. Diffusion areas with sizes of 500 × 500 and 1000 × 1000 μm were defined on the oxide-covered wafers using the conventional photolithographic technique. The p^+-n junctions with junction depth of 0.3 μm were formed by BF_2^+ implantation at 40 keV to a dose of 3×10^{15} cm^{-2}, followed by furnace annealing at 900°C for 30 min in N_2 ambient.

After the junctions were formed, the wafers were divided into three groups for the preparation of the following devices: Cu/p^+-n, WSi_x/p^+-n, and Cu/WSi_x/p^+-n junction diodes. The WSi_x layer was deposited by CVD method to a thickness of about 50 nm using SiH_4 reduction of WF_6. Prior to the CVD-WSi_x deposition, the wafers were dipped in dilute HF (50:1) for 30 s, followed by a rinse in DI water for 5 min and spin dry. The wafers were then loaded into a load-locked coldwall W-CVD system (ULVAC ERA-1000S) within 5 min and transferred to the deposition chamber without exposure to the atmosphere. The ERA-1000S is a fully automatic single-wafer CVD system equipped with a cluster of multichambers, including a load/unload, buffer, and two deposition chambers. The system employs a robot unit in the buffer chamber for wafer transfer in vacuum. The aluminum-alloy reactor was water-cooled and was kept at a high vacuum base pressure of 1×10^{-6} Torr by a turbopump. In this study, the CVD-WSi_x was deposited using the following conditions: substrate temperature 150–450°C, total gas pressure 12 mTorr, WF_6 flow rate 2 sccm, and SiH_4 flow rate 6 sccm. We designated these deposition conditions with substrate temperature at 250°C as the standard deposition condition hereafter.

After the WSi_x deposition, Cu metallization was applied for the fabrication of Cu/p^+-n and Cu/WSi_x/p^+-n junction diodes. Cu films 200 nm thick were sputter-deposited using a pure Cu target (99.99%) in Ar ambient at a pressure of 7.6 mTorr. The base pressure before sputtering was below 2×10^{-6} Torr. Finally, the Cu layer was patterned and then etched using 5 vol % HNO_3 dilute solution, and the WSi_x layer was etched using SF_6/N_2 plasma etching. For comparison, WSi_x/p^+-n junction diodes without the Cu overlayer were also fabricated. The completed structures for the Cu/p^+-n, WSi_x/p^+-n, and Cu/WSi_x/p^+-n junction diodes are illustrated in Fig. 1.

To investigate thermal stability of the diodes, samples were thermally annealed in N_2 flowing furnace for 30 min at various temperatures from 200 to 800°C. Reverse bias leakage current measurement on the thermally annealed Cu/WSi_x/p^+-n junction diodes was used to evaluate the barrier capability of WSi_x. An HP-4145B semiconductor parameters analyzer was used for the measurement, and at least 30 diodes were measured in each case. Unpatterned samples with structures of Cu/Si, WSi_x(250 nm)/Si, and Cu/WSi_x(50 nm)/Si were also prepared for material analysis. A four-point probe was used for sheet resistance measurement. Film stress of the as-deposited WSi_x layers was measured using a commercially available Tencor FLX-2320 system. Auger electron spectroscopy (AES) was used to determine the composition of WSi_x films. X-ray diffraction (XRD) analysis using a 30 keV copper Kα radiation was used for phase identification, and scanning electron microscopy (SEM) was used to observe surface morphology.

Results and Discussion

Thin-film properties of CVD-WSi_x.—To investigate the effects of deposition temperature on the film properties of the CVD-WSi_x, the deposition of WSi_x films was conducted at temperatures ranging from 150 to 450°C and with a total gas pressure of 12 mTorr, WF_6 flow rate of 2 sccm, and SiH_4 flow rate of 6 sccm. Figure 2 shows the deposition rate of WSi_x vs. deposition temperature. At temperatures below 300°C, the surface reaction was the rate-limiting process, and the activation energy of CVD-WSi_x was determined to be 3.0 kcal/mol. At temperatures above

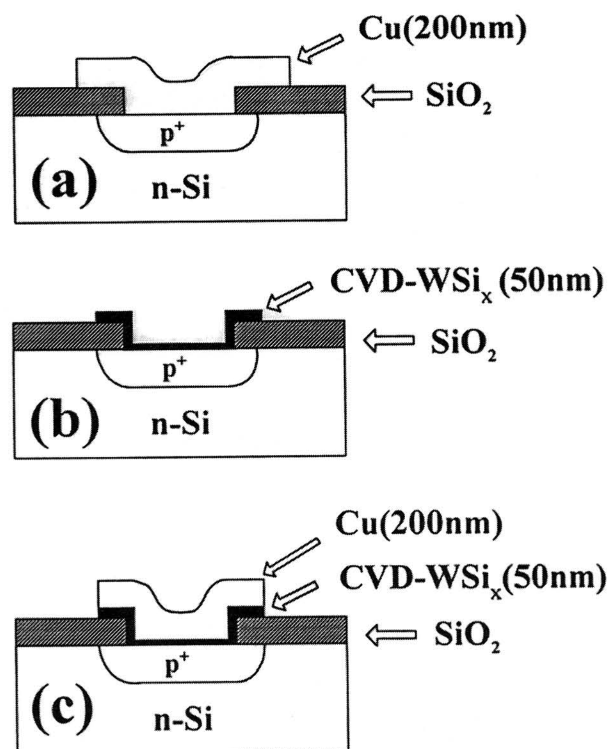

Fig. 1. Completed structures of (a) Cu/p^+-n, (b) WSi_x/p^+-n, and (c) Cu/WSi_x/p^+-n junction diodes.

300°C, the deposition rate was independent of temperature and the process was mass-transfer-limited. The as-deposited WSi_x layer was amorphous and remained in amorphous phase at temperatures up to 600°C (to be discussed later). Figure 3 shows the resistivity and film stress of the amorphous WSi_x layer vs. temperature of film deposition. The film resistivity increased with increasing temperature of film deposition. Since the decomposition of SiH_4 is a thermally activated process, the amount of Si incorporated into the WSi_x film increases with increasing deposition temperature. It was reported that the resistivity of the chemically vapor deposited amorphous WSi_x increased with increasing Si content in the as-deposited film.[15,26] The reported observation is consistent with the results of this work that the increase of deposition temperature resulted in increase of resistivity for the as-deposited WSi_x film. The film stress of the WSi_x layer decreased with increasing deposition temperature. A similar result was reported for silicon-rich WSi_x films. The stress of WSi_x decreased with the deposition temperature.[27] Fig-

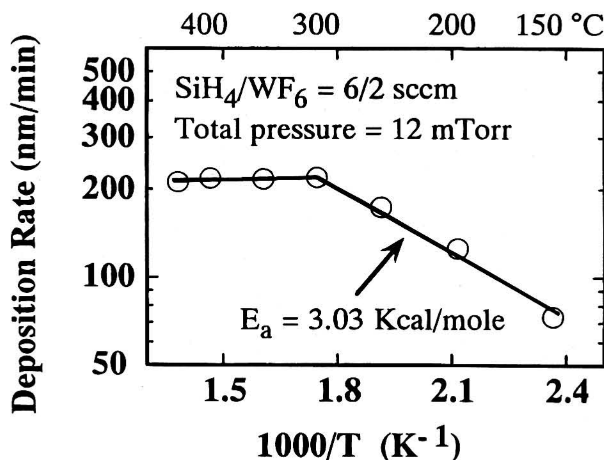

Fig. 2. Deposition rate of WSi_x vs. deposition temperature.

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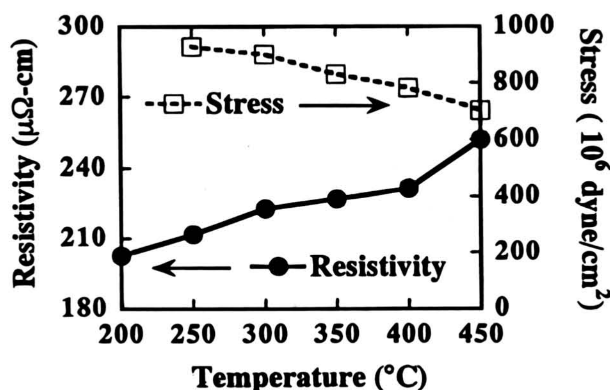
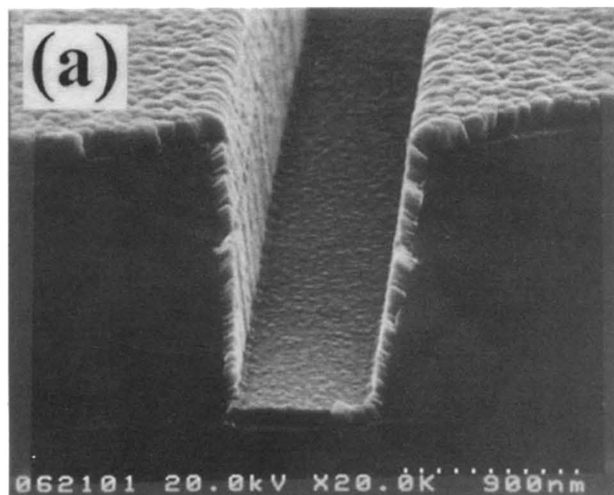


Fig. 3. Film resistivity and stress of WSi_x vs. deposition temperature.

ure 4 shows the WSi_x films deposited on submicron trenches with aspect ratios of 2 and 5 using the "standard deposition condition." A highly conformal deposition of CVD-WSi_x was obtained.

Electrical measurement.—The Cu/p^+-n, Cu/WSi_x/p^+-n, and WSi_x/p^+-n junction diodes were thermally annealed in an N_2 flowing furnace for 30 min at various temperatures. Figure 5 shows the statistical distributions of reverse bias leakage current density measured at −5 V for the Cu/p^+-n, Cu/WSi_x/p^+-n, and WSi_x/p^+-n junction diodes in which the WSi_x barrier layers were deposited using our standard deposition conditions. The Cu/p^+-n diodes without any barrier layer between Cu and Si substrate failed after annealing at 200°C (Fig. 5a). With a barrier layer of 50 nm CVD-WSi_x between Cu and Si substrate, the Cu/WSi_x/p^+-n junction diodes were able to retain the devices integrity up to 500°C. After annealing at 550°C, however, the diodes completely failed (Fig. 5b). For comparison, WSi_x/p^+-n junction diodes without a Cu overlayer were also investigated. The WSi_x/p^+-n junction diodes retained their integrity up to 700°C and revealed only slight degradation after annealing at 750°C (Fig. 5c), presumably due to WSi_2 formation (which consumed the substrate Si) and its grain growth as well as increase of film stress for the thermally annealed WSi_x layer. Clearly, the WSi_x layer itself did not degrade the electrical characteristics of the WSi_x/p^+-n junction diodes up to 700°C, and the complete failure of the Cu/WSi_x/p^+-n junction diodes at 550°C (Fig. 5b) is attributed to the presence of Cu overlayer on the WSi_x surface.



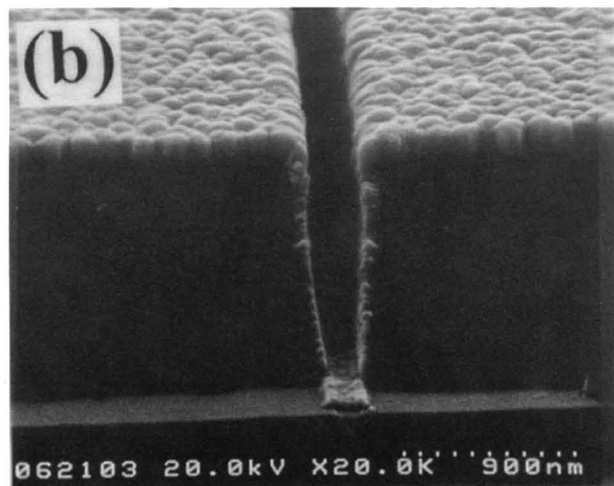


Fig. 4. Step coverage of WSi_x films deposited on submicron trenches with aspect ratio of (a) 2.0 and (b) 5.0. The WSi_x films were deposited at a total gas pressure of 12 mTorr, WF_6 flow rate of 2 sccm, SiH_4 flow rate of 6 sccm, and substrate temperature of 250°C.

Material analyses.—XRD analysis.—Figure 6 shows XRD spectra for the Cu/Si and WSi_x(250 nm)/Si samples after annealing at various temperatures. For the sample of Cu/Si annealed at 150°C, the XRD spectrum remained unchanged as compared with the as-deposited sample (not shown). However, a strong Cu_3Si peak appeared for the sample annealed at 200°C, indicating formation of copper silicide. After annealing at 250°C, the (200) peak of Cu disappeared, indicating that the Cu overlayer might have translated into Cu_3Si completely (Fig. 6a). For the sample of WSi_x(250 nm)/Si, the amorphous state of the as-deposited WSi_x remained unchanged even after annealing at 600°C. With annealing temperature raised to 650°C, a number of peaks belonging to WSi_2 phase appeared, indicating silicidation of the WSi_x layer (Fig. 6b).

The XRD spectra for the Cu/WSi_x(50 nm)/Si multilayer structure are illustrated in Fig. 7. Presumably because the WSi_x layer was too thin and was covered with a 200 nm thick Cu film, the amorphous band belonging to the WSi_x layer was too weak to be observed. The crystallization temperature of the WSi_x layer in the Cu/WSi_x/Si structure

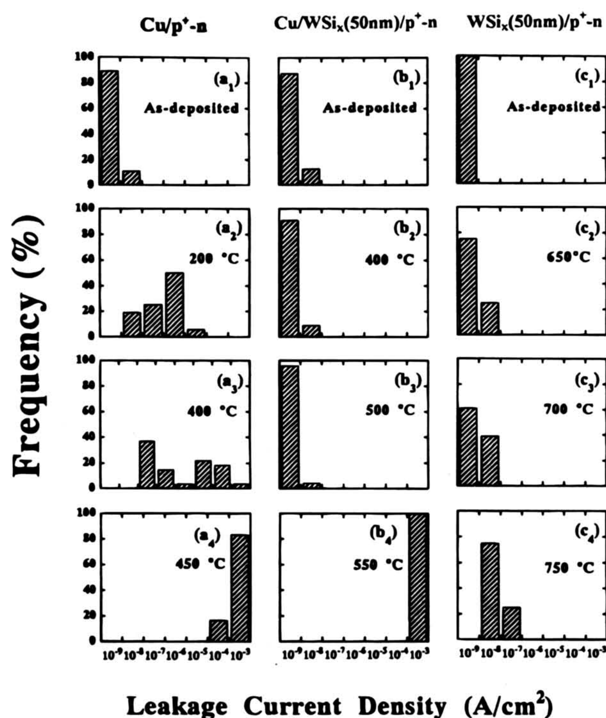


Fig. 5. Histograms showing distributions of reverse bias leakage current density for (a) Cu/p^+-n, (b) Cu/WSi_x/p^+-n, and (c) WSi_x/p^+-n junction diodes annealed at various temperatures.

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was found to be around 600°C. By comparing XRD spectra of the Cu/WSi_x/Si sample with that of the WSi_x/Si sample shown in Fig. 6b, we found that the crystallization temperature of WSi_x layer in the Cu/WSi_x/Si structure is about 50°C lower than that in the WSi_x/Si sample. This discrepancy is presumably due to the presence of Cu overlayer for the Cu/WSi_x/Si sample. It was reported that the crystallization temperature of amorphous $Ta_{36}Si_{14}N_{50}$ deposited on sapphire dropped from 1100 to 900°C when the $Ta_{36}Si_{14}N_{50}$ film was in contact with a polycrystalline copper layer.[28] In this study we found that the WSi_x/Si structure remained stable up to 600°C with no silicide phase formation (Fig. 6b); however, silicide phase appeared for the Cu/WSi_x/Si sample annealed at 600°C due to the presence of Cu layer in contact with WSi_x (Fig. 7).

The fact that the presence of Cu overlayer in the Cu/WSi_x/Si sample reduced the crystallization temperature of WSi_x may presumably be explained as follows.

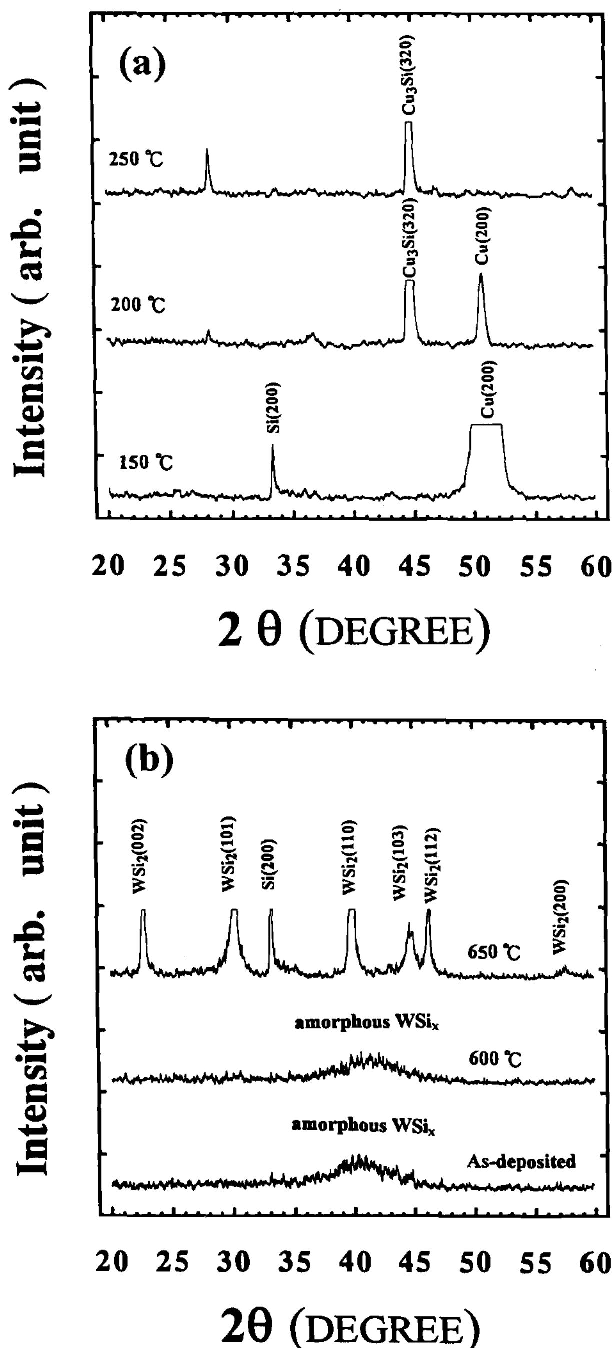

Fig. 6. XRD spectra for (a) Cu/Si and (b) WSi_x/Si samples annealed at various temperatures.

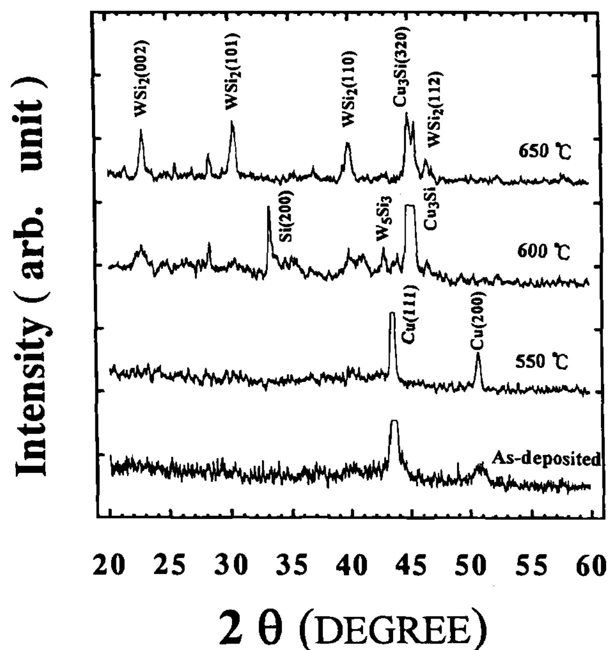

Fig. 7. XRD spectra for Cu/WSi_x/Si samples annealed at various temperatures.

First, a small amount of Cu atom penetrated the WSi_x layer to form Cu_3Si phase at the WSi_x/Si interface during thermal annealing at 600°C. This penetration probably occurred via localized defects, such as vacancy-accumulated voids, thermal-stress-induced microcracks of the WSi_x layer, and/or grain boundaries which developed from grain growth of the WSi_x layer. Second, the Cu_3Si formation at the WSi_x/Si interface generated point defects, e.g., Si self-interstitial or vacancy in the Si lattice,[29,30] promoting silicidation of WSi_x at the WSi_x/Si interface. Another possible mechanism for the accelerated silicidation of the WSi_x can be the introduction of nucleation sites by the penetrated Cu atoms. The formation of copper silicide and tungsten silicide at the WSi_x/Si interface resulted in a net volume change and produced more fast paths for Cu diffusion, thus further degrading the WSi_x barrier capability. Table I summarizes the formation of silicides on thermally annealed Cu and/or WSi_x contacted structures.

Sheet resistance measurement.—The sheet resistance change of annealed samples, normalized to the as-deposited sheet resistance value, is denoted as $\Delta Rs/Rs$ % and defined as follows

$$\frac{\Delta Rs}{Rs} \% = \frac{Rs_{\text{after anneal}} - Rs_{\text{as-deposited}}}{Rs_{\text{as-deposited}}} \times 100\%$$

Figure 8 shows the percentage change of sheet resistance vs. annealing temperature for the Cu/Si and WSi_x/Si samples. The sheet resistance of Cu/Si remained constant following anneal at temperatures up to 175°C but increased drastically after annealing at 200°C. The drastic increase in sheet resistance is attributed to the formation of high-

Table I. Silicide formation on various Cu and WSi_x contacted structures.

Annealing temperature (°C)	Contact structure		
	Cu/Si	WSi_x/Si	Cu/WSi_x/Si
200	Cu_3Si	×	×
500	Cu_3Si	×	×
600		×	W_5Si_3, WSi_2, Cu_3Si
650		WSi_2	WSi_2, Cu_3Si

Note: "×" indicates no observation of silicide phase.

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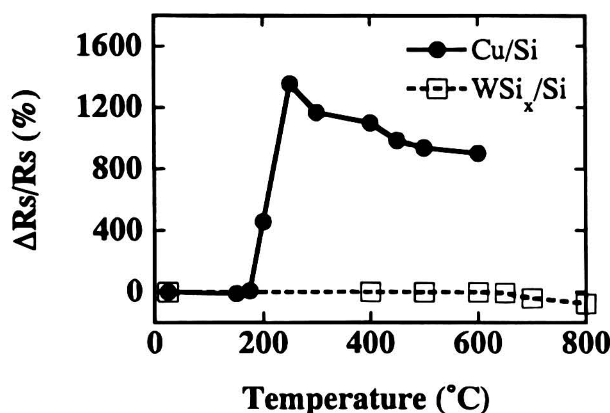


Fig. 8. Percentage change of sheet resistance vs. annealing temperature for the samples of Cu/Si and WSi_x/Si.

resistivity η''-Cu_3Si precipitate, as confirmed by XRD analysis shown in Fig. 6a. For the WSi_x/Si sample, the sheet resistance remained stable up to 600°C. With the sample annealed at temperatures above 650°C, the sheet resistance decreased slightly with increasing annealing temperature. This is attributed to the formation of low-resistivity WSi_2 phase at temperatures above 650°C, as shown in Fig. 6b.

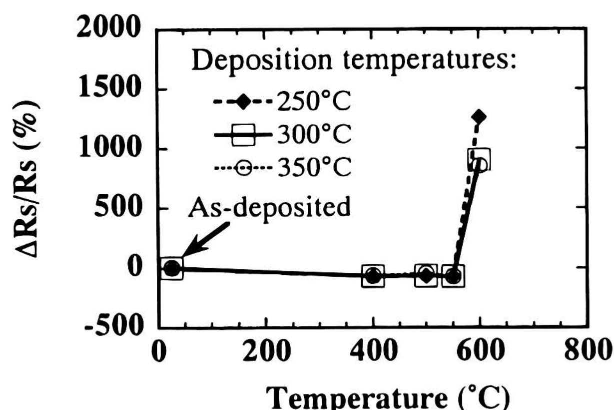


Fig. 9. Percentage change of sheet resistance vs. annealing temperature for the Cu/WSi_x/Si samples with the WSi_x films deposited at different substrate temperatures.

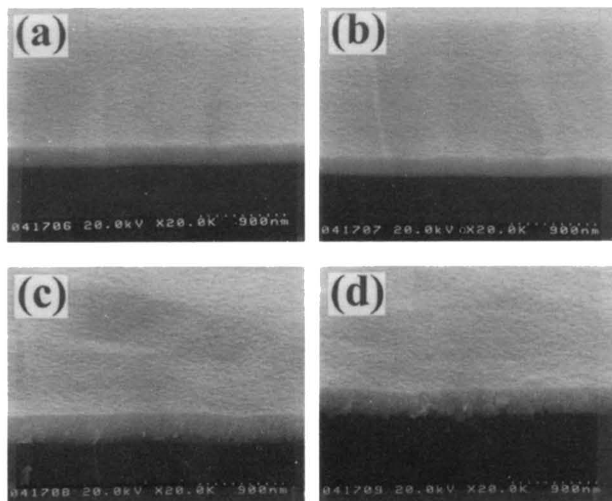
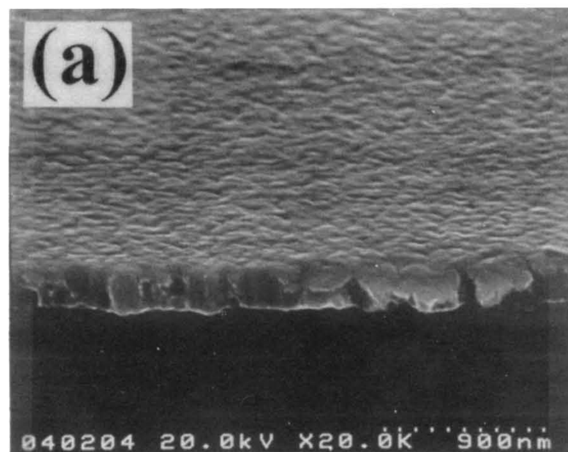
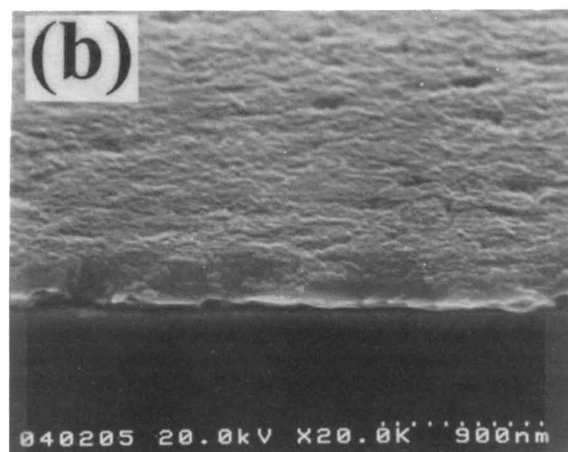


Fig. 10. Oblique view SEM micrographs for the WSi_x/Si samples (a) as-deposited and thermally annealed at (b) 600, (c) 650, and (d) 800°C.

Figure 9 shows the percentage change of sheet resistance vs. annealing temperature for the Cu/WSi_x/Si samples in which the WSi_x layers were deposited at different temperatures. It can be seen that the change of sheet resistance is not sensitive to the deposition temperature of the WSi_x layer. The sheet resistance of the Cu/WSi_x/Si samples decreased slightly after annealing at 400°C, presumably due to out-diffusion of impurities, grain growth of the Cu layer, and the annealing out of sputter-induced damage in the Cu film. Thermal stability of the Cu/WSi_x/Si multilayer structure reached 550°C. After annealing at 600°C, drastic increase in sheet resistance was found for all samples, implying failure of the Cu/WSi_x/Si structure. This is consistent with the results of XRD analysis shown in Fig. 7.





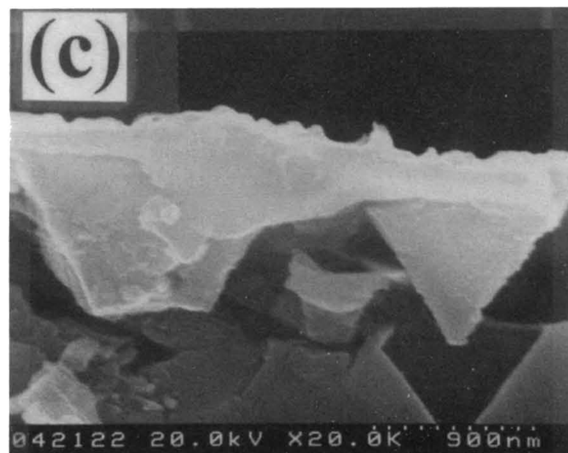


Fig. 11. SEM micrographs for the Cu/WSi_x/p^+-n junction diodes (a) as-deposited and thermally annealed at (b) 500 and (c) 550°C.

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Table II. Comparative results of barrier effectiveness for WSi_x determined by different techniques of measurement and/or analysis.

Measurement/analysis methods					
Leakage current measurement		Materials analysis			
Diode structure	Thermal stability temperature (°C)	Layered structure	Sheet resistance measurement (°C)	XRD (°C)	SEM (°C)
Cu/p^+-n	150	Cu/Si	175	150	175
$Cu/WSi_x/p^+$-n	500	$Cu/WSi_x/Si$	550	550	500
WSi_x/p^+-n	700	WSi_x/Si	650	600	600

SEM observation.—Figure 10 shows the SEM micrographs for the WSi_x(250 nm)/Si samples before and after thermal annealing. No grain-like structure was observed for both the as-deposited as well as the 600°C-annealed samples (Fig. 10a and b). Grain-like structure was observed for the WSi_x film annealed at 650°C, and it became more obvious at 800°C (Fig. 10c and d). This is consistent with the results of XRD analysis (Fig. 6b) and sheet resistance measurement (Fig. 8). Figure 11 shows the SEM micrographs for the Cu/WSi_x(50 nm)/p^+-n junction diodes before and after thermal anneal. The integrity of the Cu/barrier/Si structure basically remained unchanged after annealing at 500°C (Fig. 11b); however, large Cu_3Si precipitates were found after annealing at 550°C. With cross-sectional SEM analysis, it has been determined that a fully developed Cu_3Si precipitate is inverted pyramid-shaped and bounded by Si{111} planes (Fig. 11c).[29] Comparative results of barrier effectiveness for the WSi_x layers determined by different techniques of measurement and/or analysis are summarized in Table II.

Conclusions

Thin-film properties of amorphous WSi_x layers and thermal stability of $Cu/WSi_x/p^+$-n junction diodes were investigated. The amorphous WSi_x layer was deposited by (CVD) method using the SiH_4/WF_6 chemistry with the activation energy determined to be 3.0 kcal/mol. The WSi_x film has a low film stress, low electrical resistivity, and excellent step coverage. The WSi_x/Si structure is thermally stable up to at least 600°C, while the copper-contacted $Cu/WSi_x/Si$ structure with a 50 nm thick WSi_x barrier is stable only up to 550°C. Moreover, the $Cu/WSi_x/p^+$-n junction diodes are able to sustain a 30 min thermal annealing at temperatures up to 500°C without causing degradation to the devices electrical characteristics. Barrier failure of the WSi_x layer at temperatures above 550°C is attributed to Cu diffusion via fast paths, which are presumably developed from grain growth of the WSi_x layer and/or thermal stress-induced weak points in the WSi_x layer.

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