Sputtered Cr and Reactively Sputtered CrN_x Serving as Barrier Layers Against Copper Diffusion

Jui-Chang Chuang,* Shuo-Lun Tu, and Mao-Chieh Chen**

Department of Electronics Engineering and the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan

ABSTRACT

The barrier capability of sputter deposited Cr and reactively sputter deposited CrN_x films against Cu diffusion in a structure of Cu/barrier/p^+n junction diodes was investigated by means of thermal annealing at elevated temperatures in conjunction with electrical measurements and material analysis. For a 500 Å thick barrier layer, the barrier capability of a pure Cr layer was limited to temperatures up to 500°C, while CrN_x films sputter deposited in a gas mixture of Ar and N_2 showed improved barrier capabilities. With Ar/N_2 flow rates of 24/6 to 24/12 standard cubic centimeters per minute, the deposited CrN_x films possessed a much improved barrier capability. In particular, the Cu/CrN_x (24/9)/p^+n junction diodes were capable of sustaining 30 min of thermal anneal at temperatures up to 700°C without degradation of the diodes' electrical characteristics. The failure of Cu/Cr/p^+n and Cu/CrN_x/p^+n junction diodes under extreme thermal treatment was presumed to arise from two mechanisms: grain boundary diffusion for lightly nitrogen doped CrN_x and pure Cr barriers, and localized defect (microcrack) diffusion for excessively nitrogen doped CrN_x barriers.

Introduction

With the continuing progress of integrated circuit technology, the requirement to increase device density necessitates the improvement of multilevel metallizations.[1,2] As the linewidth of aluminum (Al) interconnects is scaled down to deep submicrometer dimensions, the electrical resistivities of Al and its alloys are no longer low enough to reduce the interconnect propagation delay.[3] The Al interconnection line also suffers from earlier electromigration failure under high current density.[4-6] Furthermore, hillocks form on Al films at processing temperatures as low as 300°C, and cause interlevel (as well as intralevel) shorting by penetrating through the dielectric layers that separate neighboring interconnect lines.[7]

Copper (Cu) has been extensively studied as a potential substitute for Al and Al alloys in multilevel metallization of semiconductor devices and integrated circuits.[1,2] Copper metallization for multilevel interconnects has many advantages, such as high melting point,[8,9] high electromigration resistance,[10] low electrical resistivity,[1,8] and thus low interconnect RC time delay, low reaction tendency with commonly used diffusion barrier materials,[1,8-10] and, probably, overall back-end process simplicity. However, there are a number of difficulties associated with the application of Cu in silicon-based integrated circuits, for example, poor adhesion to dielectric layers,[1] difficulty in dry etching,[3,11] easy diffusion in silicon and SiO_2, deep level trap in silicon, and formation of Cu silicides at low temperatures. All of these drawbacks have detrimental effects on the device reliability.[12-17] Therefore, the use of barrier layers between Cu and Si as well as Cu and SiO_2 becomes essential to the successful use of Cu in integrated circuit applications.

A large number of barrier layers have been studied.[17] Among them, refractory metals (Cr, Nb, Ti, Mo, W, and Ta) and their nitrides have been investigated as diffusion barriers because of their high melting points, high thermal stability, good adhesion to dielectrics, and good electrical conductivity.[17-21] Chromium (Cr) and its nitride (CrN_x) films are widely used as scratch and corrosion passivation layers in field application.[22,23] Nonetheless, little work has been reported regarding the properties of Cr-related thin films that serve as diffusion barriers in Cu metallization systems. In this work, Cu/Cu/*n*-Si and Cu/CrN_x/*n*-Si structures were investigated with respect to the barrier capability of the sputtered Cr and reactively sputtered CrN_x films against Cu diffusion.

* Electrochemical Society Student Member.
** Electrochemical Society Active Member.

Experimental

For this study, Cu/Cr/p^+n and Cu/CrN_x/p^+n junction diodes were fabricated from n-type, (100) oriented, 4 in. diam Si wafers with a nominal resistivity of 1-7 Ω cm. After a standard RCA cleaning,[24] 5000 Å SiO_2 was thermally grown in a pyrogenic steam atmosphere at 1050°C. Square active regions with areas ranging from 100 × 100 to 1000 × 1000 μm were defined by the conventional photolithographic method. Then a 250 Å screen oxide was thermally grown in dry oxygen atmosphere at 900°C. The p^+n junctions were formed by BF_2^+ implantation at an energy of 40 keV to a dose of 3×10^{15} cm^{-2} followed by thermal annealing in a N_2 atmosphere at 900°C for 30 min. The screen oxide was then removed using a dilute HF solution. The junction made by this process was estimated to be 0.25-0.30 μm. The wafers were loaded into a sputtering system immediately following the screening oxide removal. A 500 Å, Cr or CrN_x barrier layer was sputter deposited, followed by another deposition of 2000 Å Cu overlayer without breaking the vacuum. The Cr film was sputter deposited using a pure Cr target (99.9999% purity) in Ar atmosphere, while the CrN_x layers were deposited by reactive sputtering using the same Cr target in a gas mixture of Ar and N_2 with various flow rates. The base pressure of the sputtering chamber was 2×10^{-6} Torr, and films were sputtered at a pressure of 7.6 mTorr. For the purpose of easy identification, the CrN_x films deposited with various flow rates of Ar and N_2 are designated as CrN_x (a/b) hereafter, where a and b stand for Ar and N_2 flow rates in standard cubic centimeters per minute (sccm), respectively, in the sputtering gas mixture. After the deposition of the Cu overlayer, the Cu/Cr as well as the Cu/CrN_x dual layers were patterned using the lift-off method.

The Cu/barrier/p^+n samples were thermally annealed in a furnace for 30 min at temperatures ranging from 400 to 800°C in a N_2 atmosphere. At the end of the thermal treatment, samples were retained in the furnace with N_2 flushing until the temperature was below 200°C; then samples were removed from the furnace. Reverse bias leakage currents were measured at a reverse bias of 5 V for the samples with various junction areas. Typically, for each case, eighteen randomly chosen diodes were measured using an HP4145B semiconductor parameter analyzer.

Unpatterned samples of Cr/Si, CrN_x/Si, Cu/Cr/Si, and Cu/CrN_x/Si structures processed in the same process run were also prepared for material analysis. Sheet resistance was measured using a four-point probe on the unpatterned samples. The phase composition was identified by X-ray diffraction (XRD) analysis. Scanning electron microscopy

(SEM) was used to investigate the surface morphology and the cross section of the samples. The nitrogen content (atomic concentration, designated as N atom %) in the as-deposited CrN_x film was obtained by Auger electron spectroscopy (AES) analysis.

Results and Discussion

Thermal stability of Cu/barrier/p⁺n junction diodes.— Figure 1 shows the statistical distributions of reverse bias (5 V) leakage current densities for the Cu/Cr (500 Å)/p⁺n junction diodes as well as for the Cu/CrN_x(500 Å)/p⁺n junction diodes annealed at various temperatures. In this study, we defined a leakage current density larger than 1×10^{-7} A/cm² as a failure. The Cu/Cr/p⁺n junction diodes (Fig. 1a) were able to sustain a 30 min thermal treatment up to 500°C without causing degradation; however, annealing at 550°C resulted in severe degradation. For the Cu/CrN_x(24/4)/p⁺n junction diodes (Fig. 1b), diode degradation after annealing at temperatures above 600°C was observed, showing an at least 50°C improvement of the thermal stability over the Cu/Cr/p⁺n diodes. Further improvement was observed for the Cu/CrN_x(24/6)/p⁺n and Cu/CrN_x(24/12)/p⁺n junction diodes (Fig. 1c and e), which were able to sustain the thermal treatment up to 600°C. The best result was observed for the Cu/CrN_x(24/9)/p⁺n junction diodes (Fig. 1d), which remained stable at temperatures up to 700°C. This is an improvement of 200°C as compared to the Cu/Cr/p⁺n junction diodes. However, the thermal stability of Cu/CrN_x(24/16)/p⁺n diodes (Fig. 1f) showed only slight improvement over that of Cu/Cr/p⁺n diodes.

Average values of leakage current density vs. annealing temperature for all the Cu/CrN_x/p⁺n junction diodes are summarized in Fig. 2. The results indicate that the thermal stability of Cu/Cr/p⁺n junction diodes can be substantially improved by using reactively sputtered CrN_x films with appropriate nitrogen contents in a sputtering gas mixture of Ar and N_2 instead of a pure Cr barrier layer.

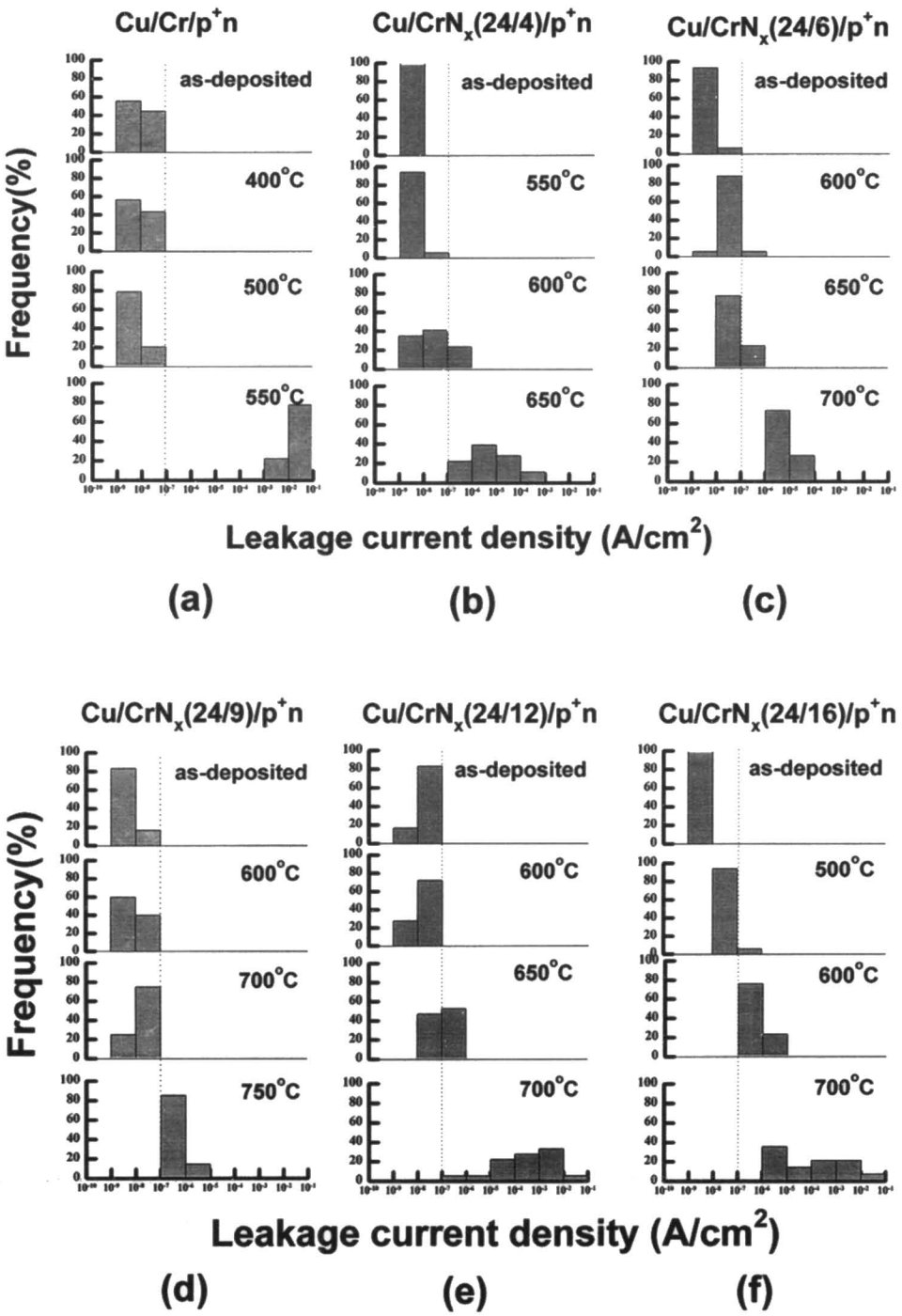

Fig. 1. Statistical distributions of reverse bias (5 V) leakage current density for the Cu/barrier/p⁺n junction diodes having 500 Å thick barrier layers annealed at various temperatures for 30 min: (a) Cu/Cr/p⁺n, (b) Cu/CrN_x(24/4)/p⁺n, (c) Cu/CrN_x(24/6)/p⁺n, (d) Cu/CrN_x(24/9)/p⁺n, (e) Cu/CrN_x(24/12)/p⁺n, and (f) Cu/CrN_x(24/16)/p⁺n.

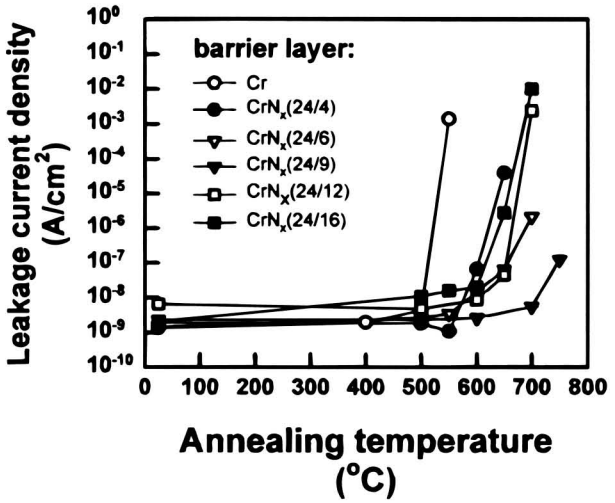

Fig. 2. Average reverse bias leakage current density vs. annealing temperature for various Cu/barrier/p⁺n junction diodes.

Physical properties of Cr and CrN_x films deposited on an Si substrate.—Figure 3 shows the nitrogen content (N atom %) of various as-deposited CrN_x films. It reveals the increasing trend of N atom % in the CrN_x films with the increase of nitrogen volume fractions (N_2/Ar + N_2) in the sputtering gas mixture. Nonetheless, N atom % eventually reached a saturated value of about 40 atom %. Figure 4 shows the surface morphology of the 2000 Å thick as-deposited Cr and various CrN_x films on Si substrates. The Cr film (Fig. 4a) revealed a slightly granular surface, while the CrN_x films revealed granular surfaces with various grain sizes and roughness (Fig. 4b-d). Also, microcracks were clearly observable on the surface of the CrN_x(24/16) film (Fig. 4d), which was sputtered in a gas mixture with a high content of nitrogen (flow rate 16 sccm). Figure 5 shows XRD spectra for the as-deposited and thermally annealed Cr and various CrN_x films deposited on Si substrates. For the as-deposited samples (Fig. 5a), the Cr/Si sample exhibited a strong Cr(110) preferred orientation as well as a weak diffraction peak corresponding to the Cr oxide, presumably due to air exposure of the samples before taking the XRD analysis, because Cr is inherently an oxygen absorber.[8,9] For the CrN_x/Si samples, the Cr nitride (CrN) phase appeared, and the intensity of the diffraction peak became stronger with increasing nitrogen content in the sputtering gas mixture. The CrN_x(24/4)/Si (not shown) and CrN_x(24/6)/Si samples revealed similar XRD spectra, i.e., neither Cr nor CrN diffraction peaks were observed. The CrN_x(24/9)/Si sample revealed a polycrystalline CrN phase of (111) and (200) orientations. The CrN_x(24/12) and CrN_x(24/16) (not shown) samples showed similar spectra, in which only CrN(111) X-ray reflections were found. For the thermally annealed samples (Fig. 5b), the XRD spectra showed basically the same nitride phase detected in the corresponding as-deposited samples. However, a silicide ($CrSi_2$) phase appeared on the Cr/Si sample annealed at

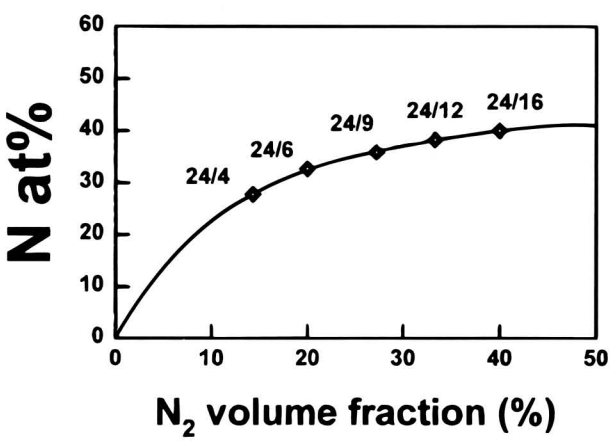

Fig. 3. N atom % of as-deposited CrN_x films vs. N_2 volume fraction in the sputtering gas mixture as determined by AES.

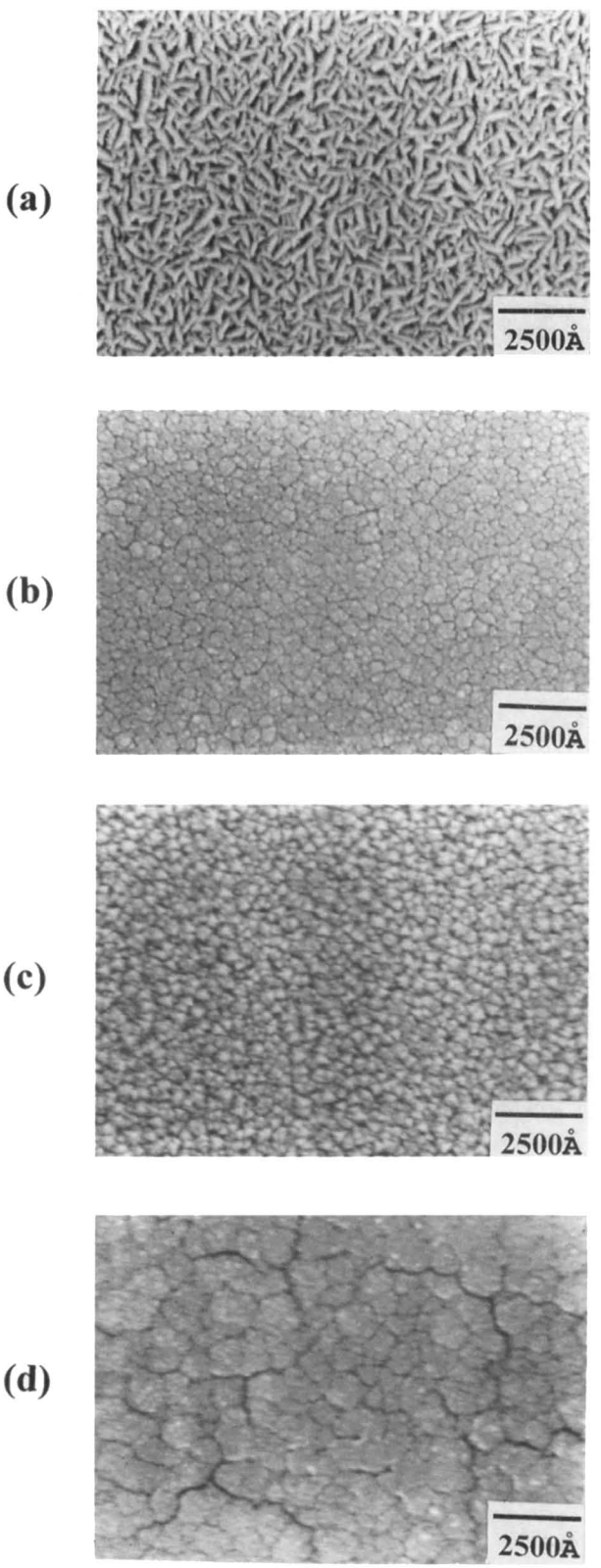

Fig. 4. SEM micrographs showing the surface morphology of as-deposited Cr and CrN_x films: (a) Cr, (b) CrN_x(24/6), (c) CrN_x(24/9), and (d) CrN_x(24/16).

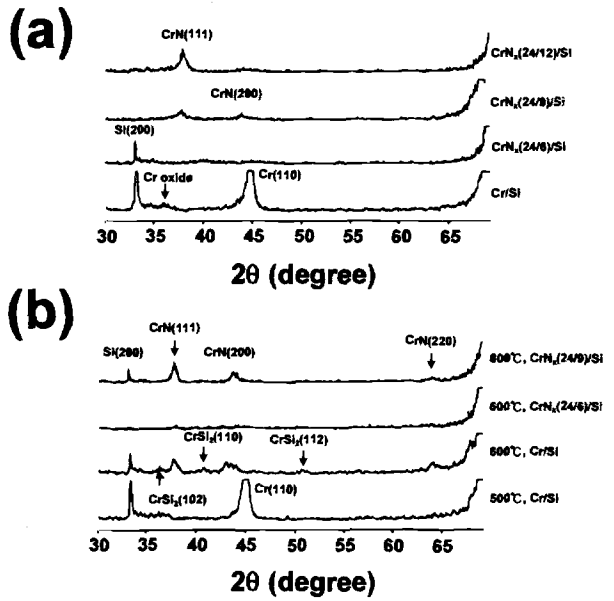

Fig. 5. XRD spectra for (a) as-deposited and (b) thermally annealed Cr/Si and various CrN_x/Si samples.

temperatures of 600°C and above. Figure 6 shows the resistivity of CrN_x films vs. nitrogen volume fraction in the sputtering gas mixture, showing an N-shaped variation. Figure 7 shows the deposition rate of CrN_x films for various sputtering powers vs. nitrogen volume fraction in the sputtering gas mixture. As was expected, higher sputtering powers resulted in higher deposition rates. Furthermore, higher volume fractions of nitrogen in the sputtering gas mixture resulted in lower deposition rates.

Thermal annealing of Cu/Cr/Si and Cu/CrN$_x$/Si structures.—XRD spectra of as-deposited and thermally annealed Cu/Cr/Si and Cu/CrN_x/Si samples having 500 Å thick barrier films are illustrated in Fig. 8. For the as-deposited samples, the phase composition of the Cr and CrN_x films remained unchanged as compared with the corresponding samples without a Cu overlayer. In addition, there were no obvious differences between the spectra of as-deposited and the corresponding low temperature annealed samples. Figure 9 shows sheet resistance vs. annealing temperature for various Cu/CrN_x/Si samples. After annealing at a temperature of 400°C, all samples revealed a slight decrease of sheet resistance, presumably due to the healing of sputter induced defects and the crystallization of the Cr and CrN_x films.[1,17,25] For the Cu/Cr/Si sample, sheet resistance revealed a drastic increase after

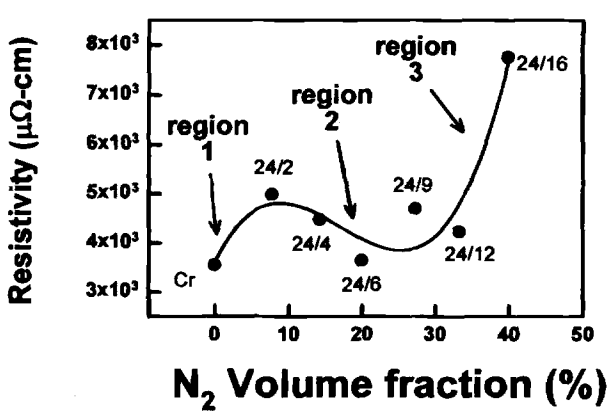

Fig. 6. Resistivity of as-deposited CrN_x films vs. N_2 volume fraction in the sputtering gas mixture.

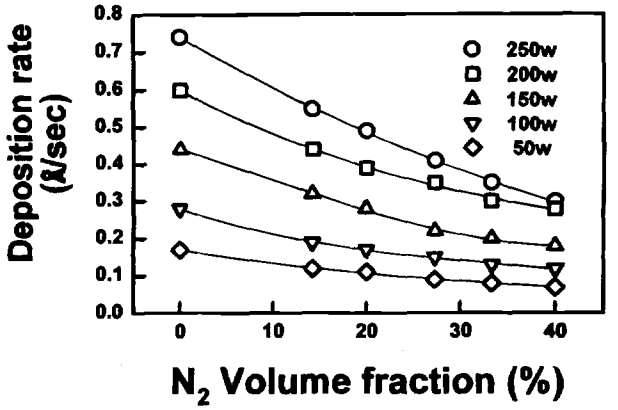

Fig. 7. Deposition rate of CrN_x films vs. N_2 volume fraction in the sputtering gas mixture for various sputtering powers.

annealing at 500°C, and the XRD analysis showed the appearance of Cu_3Si phase after annealing at temperatures as low as 550°C, but showed no appearance of Cr silicide phase (Fig. 8a). For the Cu/CrN_x(24/4)/Si sample, Cu_3Si and $CrSi_2$ were observed after annealing at 650°C (Fig. 8b) and the sheet resistance also showed a drastic increase (Fig. 9a). For the samples with Cr or CrN_x(24/4) as a barrier layer, the results of the electrical measurements (Fig. 1 and 9) and the XRD analysis (Fig. 8) consistently show that the formation of high resistive Cu silicide[20] stand for the failure of the diffusion barrier. For the sam-

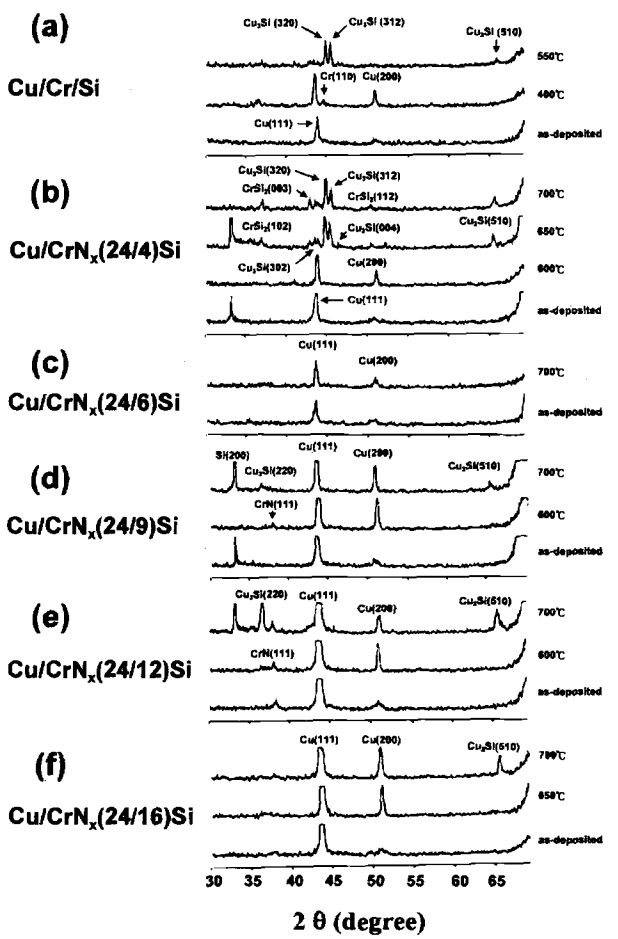

Fig. 8. XRD spectra for the as-deposited as well as the thermally annealed Cu/barrier/Si samples: (a) Cu/Cr/Si, (b) Cu/CrN_x(24/4)/Si, (c) Cu/CrN_x(24/6)/Si, (d) Cu/CrN_x(24/9)/Si, (e) Cu/CrN_x(24/12)/Si, and (f) Cu/CrN_x(24/16)/Si.

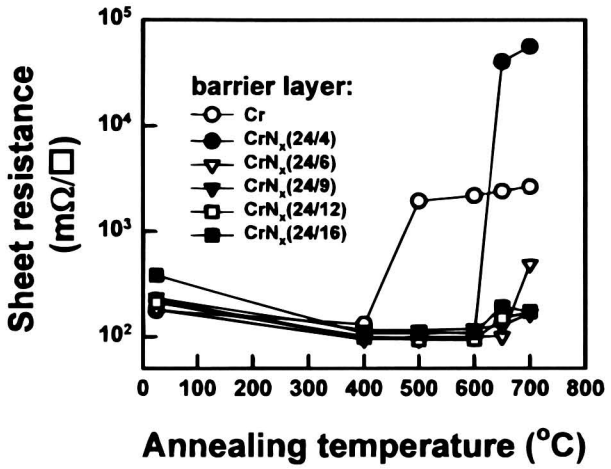

Fig. 9. Sheet resistance vs. annealing temperature for various Cu/barrier/Si samples.

ples with a barrier layer of CrN_x films deposited with a higher nitrogen content in the sputtering gas mixture (Ar/N_2 flow ratio less than 24/6), Cu silicide was also detected by XRD analysis at and above the temperatures of the observation of electrical failure (Fig. 1, 8, and 9d-f); however, no Cr silicide phase was observed. The samples with CrN_x(24/9), CrN_x(24/12), and CrN_x(24/16) barrier layers showed only a moderate increase of the sheet resistance after annealing at temperatures above 600°C; this indicated that the interaction between Cu and Si substrates was not sensitively detectable by sheet resistance measurement and XRD analysis, but was serious enough to detrimentally increase the junction leakage current. Figure 10 shows SEM micrographs for the Cu/Cr/Si and $Cu/CrN_x/Si$ samples annealed at elevated temperatures; formation of Cu silicide can be clearly observed. After annealing at high temperatures, tetragonal[9,26-28] Cu_3Si was observed. Deformed and ruptured films due to the stress induced by the volume change of silicide formation were easily observed for the Cu/Cr/Si sample annealed at 600°C (Fig. 10a and b) and the Cu/CrN_x(24/4)/Si sample annealed at 650°C (Fig. 10c); they were also observed for the Cu/CrN_x(24/6)/Si sample annealed at 800°C (Fig. 10d) and the Cu/CrN_x(24/9)/Si sample annealed at 750°C (Fig. 10e), though they were found in fewer numbers. For the Cu/CrN_x(24//16)/Si sample that revealed microcracks in the as-deposited CrN_x film (Fig. 4d), thermal annealing resulted in porosity of the Cu overlayer (Fig. 10f), presumably resulting from the fast inward diffusion of Cu through the microcracks.[29]

Discussion.—In Fig. 5, it was observed that the sputtered Cr film revealed a Cr(110) preferred orientation, which remained stable after annealing at temperatures up to 500°C. For the reactively sputtered CrN_x films, diffraction peaks of CrN phase appeared and the intensity of the peaks increased with the nitrogen content in the sputtering gas

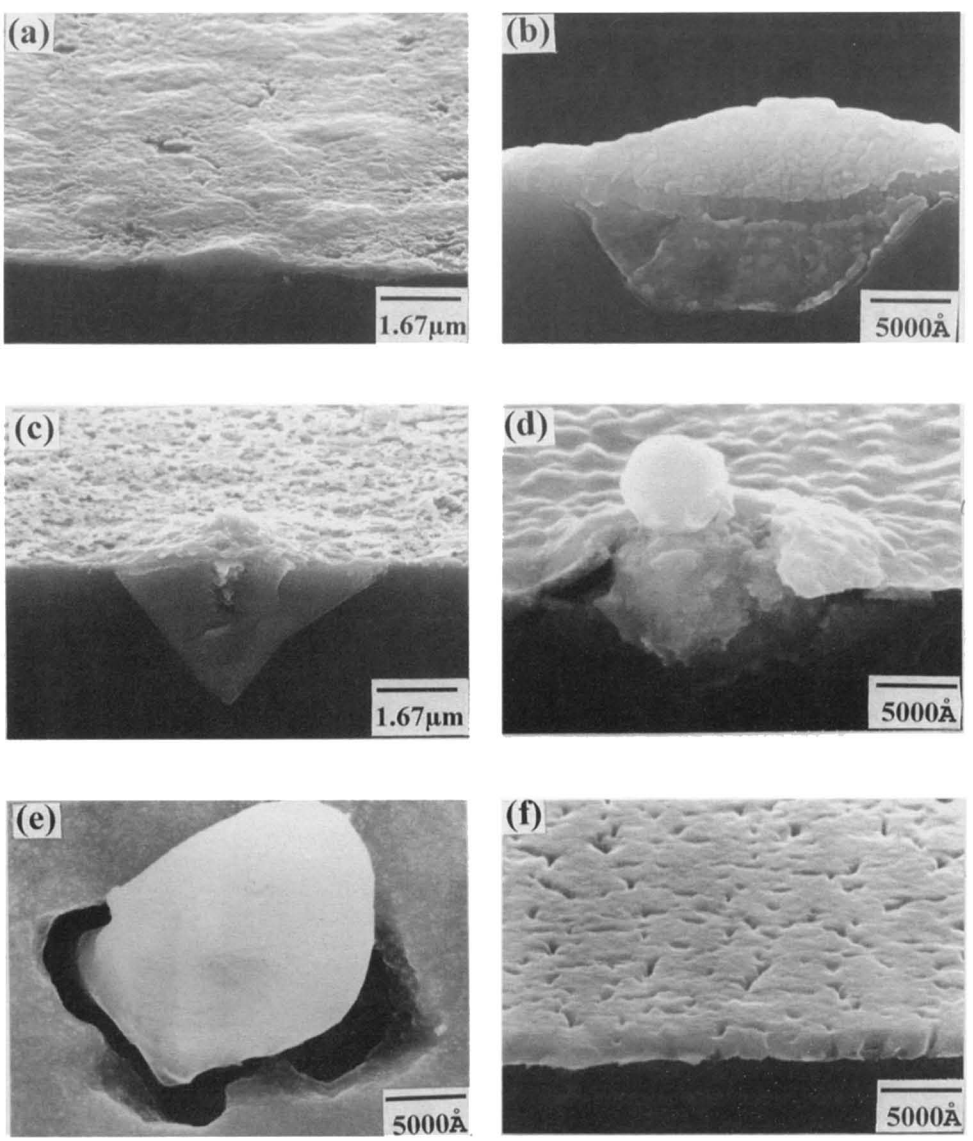

Fig. 10. SEM micrographs showing the surface morphology and cross-sectional view for the thermally annealed Cu/barrier/Si samples: (a) and (b) Cu/Cr/Si at 600°C, (c) Cu/CrN_x(24/4)/Si at 650°C, (d) Cu/CrN_x(24/6)/Si at 800°C, (e) Cu/CrN_x(24/9)/Si at 750°C, and (f) Cu/CrN_x(24/16)/Si at 650°C.

mixture. In addition, the CrN phase with the (111) preferred orientation was detected for the samples of CrN_x(24/12) and CrN_x(24/16). Because all the CrN_x films were reactively sputtered using the same conditions except the Ar/N_2 flow rates, we assume that the nitrogen content in the sputtering gas mixture should be responsible for the orientation preference.

For the CrN_x films deposited with low nitrogen flow rates, the incorporated nitrogen did not react with the sputtered Cr; instead, the nitrogen tended to collect in the grain boundaries of the deposited Cr films. As a consequence of lattice deformation, the resistivity of the Cr films increased with the increase of nitrogen content. This is designated as region 1 for the N-shaped curve shown in Fig. 6. Eventually, the crystalline structure of the Cr film was destroyed and the XRD data showed a nearly amorphous spectrum, which revealed no distinguishable diffraction peak after annealing at temperatures up to 600°C. As the nitrogen content in the sputtering gas mixture was increased, the chemical reaction of Cr and nitrogen increased, resulting in the formation of Cr nitride, and thus decreasing resistivity (region 2 of Fig. 6). The XRD data were similar to that shown in Fig. 5 for the sample of CrN_x(24/6)/Si, which revealed very weak but still distinguishable diffraction peaks of CrN after annealing at 600°C. As the nitrogen content in the sputtering gas mixture was further increased, a portion of the incorporated nitrogen turned to decorate grain boundaries of the polycrystalline Cr nitride in addition to increase the N atom % in the deposited films; thus, resistivity of the film increased again. However, we assume that there is a competing sputter deposition/etching process in the sputtering chamber. The nitrogen in the reactive sputtering process served as a reactant for the formation of Cr nitride and also supported the N_2 plasma, which would sputter etch the deposited Cr nitride film. When the nitrogen flow rate in the sputtering gas mixture was increased to a notable amount, the rates of sputter etching and sputter deposition became comparable.[25,30] Thus, we observed the ceasing of the increasing trend of N atom % (Fig. 3), the decrease of deposition rates irrespective of the deposition power (Fig. 7), and the increase of surface damages of the films. Eventually, as the nitrogen flow rate was increased to an excessive amount (e.g., an N_2 flow rate of 16 sccm), microcracks (Fig. 4d) were created in the films that resulted in a drastic increase of resistivity, as shown in region 3 of Fig. 6.

Thermodynamic data[31] suggest that Cr nitrides are more stable than Cr silicides at room temperature but silicides are more stable at elevated temperatures., The results shown in Fig. 5b indicate that interaction between Cr and the nitrogen in N_2 atmosphere as well as between Cr and the silicon in Si substrate occurred at 600°C of the Cr/Si samples, while there was no interaction between CrN_x and the Si substrate at temperatures up to 800°C for the CrN_x/Si samples. For the reactively sputter deposited CrN_x films on Si substrate, Cr nitride was formed during the sputter deposition process, and the formation of Cr silicide was deterred by the presence of Cr nitride.

There are two possible types of Cu diffusion paths in the Cr-based barrier layers. First, for the Cr and CrN_x films deposited with low nitrogen content in the sputtering gas mixture (N_2 flow rates below 6 sccm), Cu diffuses to the Si substrate through the barrier layers along the grain boundaries which are deficient in nitrogen decoration. Second, for the CrN_x films deposited with high nitrogen content in the sputtering gas mixture (N_2 flow rates above 12 sccm), localized defects, such as microcracks, provide fast diffusion paths for Cu diffusion. Cu can diffuse to the Si substrate by way of these diffusion paths and deteriorate the electrical characteristics of the p^+n junction diodes,[12-17] and form localized Cu_3Si grains as shown in Fig. 10. As the grains of Cu_3Si grew, the volume difference between Cu and its silicide resulted in the deformation of the Cu overlayer and the protrusion of Cu_3Si through the Cu overlayer as well as the intrusion of Cu_3Si grains into the underlying Si substrate.

Presumably, the roles of the nitrogen are to collect at the grain boundaries of the as-deposited barrier layers and to form Cr nitrides. For the CrN_x films deposited with low nitrogen content in the sputtering gas mixture, there was not enough nitrogen incorporation and a Cr nitride phase was not detected. For the CrN_x films deposited with high nitrogen content in the sputtering gas mixture, the nitrogen content in the CrN_x films was increased and CrN was detected. The abundant supply of nitrogen not only formed Cr nitride but also blocked the grain boundaries of the Cr nitride; thus, it should possess a superior barrier capability. However, CrN_x films deposited with very high nitrogen content in the sputtering gas mixture (e.g., N_2 flow rate of 16 sccm) possessed sputter-induced defects such as miro-cracks. Therefore, the defect-related failure took dominance and the electrical characteristics of the p^+n junction diodes tended to deteriorate with increasing annealing temperature. For the CrN_x films deposited with medium nitrogen content in the sputtering gas mixture (N_2 flow rates from 6 to 12 sccm), failure would occur due to both mechanisms. Moreover, the barrier capability of CrN_x films deposited with nitrogen flow rate of 9 sccm (i.e., the CrN_x(24/9) film) was the best among all the Cr nitride films investigated.

Conclusion

This work investigated the barrier capability of sputter deposited Cr and reactively sputter deposited CrN_x films against Cu diffusion in a structure of Cu/barrier/p^+n junction diodes. The CrN_x films deposited in a sputtering gas mixture of Ar and N_2 with Ar/N_2 flow ratios from 24/6 to 24/12 were found to possess efficient barrier capability. For a 500 Å thick layer, we found that the Cu/CrN_x(24/9)/p^+n junction diodes were capable of sustaining 30 min of thermal annealing at temperatures up to 700°C without degradation to the diodes' electrical characteristics. The corresponding thermal stability of junction diodes using a pure Cr barrier layer was found to be 500°C. The failure of Cu/CrN_x/p^+n junction diodes under extreme thermal treatment was presumed to be arising from two mechanisms: grain boundary diffusion for the lightly nitrogen doped CrN_x including the Cr barriers, and localized defect (microcrack) diffusion for the excessively nitrogen doped CrN_x barriers.

Acknowledgment

The authors wish to thank the Semiconductor Research Center of National Chiao-Tung University for providing excellent processing environment. This work was supported by the National Science Council, ROC, under contract no. NSC-86-2215-E-009-040.

Manuscript submitted March 10, 1998; revised manuscript received August 10, 1998.

National Chiao-Tung University assisted in meeting the publication costs of this article.

REFERENCES

1. See, for example, *MRS Bull.*, **18** (1993); **19** (1994); devoted to the topic of copper metallization for microelectronics.
2. K. P. Rodell, E. G. Colgan, and C. K. Hu, in *Mater. Res. Soc. Symp. Proc.*, **337,** P. Murarka, A. Katz, K. N. Tu, and K. Maex, Editors, p. 59, MRS, Pittsburgh, PA (1994).
3. C. K. Hu, B. Luther, F. B. Kaufman, J. Hummel, C. Uzoh, and D. J. Pearson, *Thin Solid Films*, **262,** 84 (1995).
4. K. N. Tu, *J. Vac. Sci. Technol., A*, **2,** 216 (1984).
5. J. K. Howard, J. F. White, and P. S. Ho, *J. Appl. Phys.*, **49,** 4083 (1978).
6. C. K. Hu, *Thin Solid Films*, **260,** 124 (1995).
7. S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era*, Vol. 1, Editor, p. 269, Lattice Press, Sunset Beach, CA (1986).
8. *CRC Handbook of Chemistry and Physics*, 73rd ed., D. R. Lide, Editor, Section 12, CRC Press, Inc., Boca Raton, FL (1992).
9. *Binary Alloy Phase Diagrams*, 2nd ed., T. B. Massalski, Editor, pp. 1266, 1293, 1304, 1333, 1446, ASM International, Materials Park, OH (1990).
10. S. Shingubara, K. Fujiki, A. Sano, H. Sakaue, and Y. Horiike, in *Mater. Res. Soc. Symp. Proc.*, P. Borgesen,

J. C. Coburn, J. E. Sanchez, Jr., K. P. Rodbell, and W. F. Filter, Editors, p. 441, MRS, Pittsburgh, PA (1994).
11. Y. Igarashi, T. Yamanobe, and T. Ito, *Thin Solid Films,* **262,** 124 (1995).
12. J. D. McBrayer, R. M. Swanson, and T. W. Sigmon, *J. Electrochem. Soc.,* **133,** 1242 (1986).
13. Y. Shacham-Diamand, A. Dedhia, D. Hoffstetter, and W. G. Oldham, *J. Electrochem. Soc.,* **140,** 2427 (1993).
14. D. Gupta in *Mater. Res. Soc. Symp. Proc.,* S. P. Murarka, A. Katz, K. N. Tu, and K. Maex, Editors, p. 209, MRS, Pittsburgh, PA (1994).
15. G. Raghavan, C. Chiang, P. B. Anders, S. M. Tzeng, R. Villasol, G. Bai, M. Bohr, and D. B. Fraser, *Thin Solid Films,* **262,** 168 (1995).
16. *VLSI Technology,* 2nd ed., S. M. Sze, Editor, p. 309, McGraw-Hill, Singapore (1988).
17. S. Q. Wang, S. Suther, C. Hoeflich, and B. J. Burrow, *J. Appl. Phys.,* **73,** 2301 (1993).
18. C. A. Chang, *J. Appl. Phys.,* **67,** 6184 (1990).
19. D. Y. Shih, C. A. Chang, J. Paraszczak, S. Nunes, and J. Cataldo, *J. Appl. Phys.,* **70,** 3052 (1991).
20. H. Ono, T. Nakano, and T. Ohta, *Appl. Phys. Lett.,* **64,** 1511 (1994).
21. L. C. Lane, T. C. Nason, G. R. Yang, T. M. Lu, and H. Bakhru, *J. Appl. Phys.,* **69,** 6719 (1991).
22. F. Cosset, G. Contoux, A. Celerier, and J. Machet, *Surf. Coat. Technol.,* **79,** 25 (1996).
23. C. Friedrich, G. Berg, E. Broszeit, and K. H. Kloos, *Surf. Coat. Technol.,* **74-75,** 279 (1995).
24. W. Kern and D. A. Puotinen, *RCA Rev.,* **31,** 187 (1970).
25. J. C. Chuang and M. C. Chen, *Thin Solid Films,* **322,** 213 (1998).
26. C. S. Liu and L. J. Chen, *J. Appl. Phys.,* **74,** 3611 (1993).
27. C. S. Liu and L. J. Chen, *Thin Solid Films,* **262,** 187 (1995).
28. C. S. Liu and L. J. Chen, *J. Appl. Phys.,* **75,** 2370 (1994).
29. R. E. Reed-Hill, *Physical Metallurgy Principles,* 2nd ed., p. 386, Van Nostrand, New York (1972).
30. J. C. Chuang and M. C. Chen, *J. Electrochem. Soc.,* **145,** 3170 (1998).
31. E. A. Brandes, in *Smithells Metals Reference Book,* 6th ed., p. 8, Robert Hartnoll Ltd., Bodmin, Cornwall, England (1983).

Application of a Semi-insulating Amorphous Hydrogenated Silicon Nitride Film as a Resistive Field Shield and Its Reliability

K. Matsuzaki,*[a] T. Horasawa,[b] G. Tada,[c] and M. Saga[d]

[a]*Fuji Electric Corporate Research and Development, Limited, Advanced Device Technology Laboratory, Matsumoto City, Japan 390*
[b]*Fuji Electric Company, Limited, Matsumoto Factory, IC Fabrication Department, Matsumoto City, Japan 390*
[c]*Fuji Electric Company, Limited, Matsumoto Factory, Semiconductor Device Research and Development Center, Matsumoto City, Japan 390*
[d]*Fuji Electric Corporate Research and Development, Limited, Yokosuka City, Japan 240*

ABSTRACT

In order to develop reliable high voltage integrated circuits (HVICs), the characteristics of semi-insulating plasma-deposited amorphous silicon nitride (a-SiN:H) films as resistive field shields, are examined, the reliability of their application to HVICs are studied. The surfaces of these semi-insulating films were unstable, and it was concluded that these films must be covered with a final passivation film such as an insulating plasma-deposited a-SiN:H film. The transverse electrical conduction mechanism of these films is briefly discussed.

Introduction

In general, high voltage integrated circuits (HVICs) using planar technology employ shallow junctions and alternative means to control the electric field near the surface of a semiconductor. The depletion layer can be controlled and the breakdown voltage can be improved by using a field plate, a resistive field shield, an equipotential ring, etc.[1,2] The use of semi-insulating polycrystalline silicon (SIPOS) as a resistive field shield has been developed,[3-5] but its use has been limited.[6-8] Because a resistive field shield was needed and the problems encountered with SIPOS must be avoided, Osenbach et al. developed Si-rich plasma-deposited amorphous silicon nitride hydrogen alloys (a-SiN:H) as resistive field shields.[7] In this paper, we study the reliability of HVICs using such semi-insulating a-SiN:H films.

Experimental

Chemical vapor deposition of a-SiN:H films.—A VDS-5000 plasma chemical vapor deposition (CVD) system (JPEL Co.) was used for the deposition of a-SiN:H films. This system was operated at 50 kHz, 1 kW radio frequency (rf) power, and 320°C. The pressure of deposition and the flow of Ar carrier gas were kept at 53 Pa and 1.5 standard liters per minute (slm), respectively. The gas flow ratio $R = SiH_4/(SiH_4 + NH_3)$ was variable. Insulating and semi-insulating a-SiN:H films were deposited at $R = 0.15$ and $R = 0.70$–0.77, respectively. The substrates were 4 in. diam, (100)-polished silicon wafers.

HVIC device structure using semi-insulating a-SiN:H films.—The schematic structure of the device is shown in Fig. 1. The substrates were 4 in. diam, (100)-polished, p-type ($\rho = 100$–$150\ \Omega$ cm) silicon wafers. N-well ($\rho \sim 10\ \Omega$ cm, $X_j \sim 6\ \mu$m), P-base ($\rho \sim 0.5\ \Omega$ cm, $X_j \sim 2\ \mu$m), P-offset ($\rho \sim 10\ \Omega$ cm, $X_j \sim 1.5\ \mu$m), gate oxide ($t_{ox} = 25$ nm), poly-Si gate electrodes, and source-drain regions were successively formed in the substrates. The field region lying between source and drain region was covered with localized oxidation of silicon (LOCOS) ($t_{ox} = 0.7\ \mu$m), phosphosilicate glass (PSG) SiO_2 ($t_{PSG} = 1\ \mu$m), and finally a semi-insulating α-SiN:H film ($t_{SiN} = 1\ \mu$m, $R = 0.76$ typically) as a resistive field shield. The length of the field region was ~70 μm. The breakdown voltage of this HVIC was designed to be over 700 V.

Measurements.—The thickness of the film was determined by a laser-based ellipsometer. The density of the film was calculated using the mass determined by measuring the sample weight before and after deposition, and the volume of the film. The transmission infrared spectrum of the film was taken with Fourier transform infrared (FTIR)

* Electrochemical Society Active Member.