Effect of bottom electrodes on dielectric relaxation and defect analysis of $(Ba_{0.47}Sr_{0.53})TiO_3$ thin film capacitors

M.S. Tsai, T.Y. Tseng[*]

Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 30050, Taiwan

Abstract

The dielectric relaxation and defect analysis of $(Ba_{0.47}Sr_{0.53})TiO_3$ (BST) thin films deposited on various bottom electrodes, such as Pt, Ir, IrO_2/Ir, Ru, RuO_2/Ru before and after annealing in O_2 ambient was investigated. Through the measurement of dielectric dispersion as a function of frequency (100 Hz $\leq f \leq$ 10 MHz) and temperature (27°C $\leq T \leq$ 150°C), we studied the trapping dielectric relaxation and defect quantity of the films, and proposed an equivalent circuit on the basis of the capacitance, admittance and impedance spectra. A shallow trap level located at 0.005–0.01 eV below the conduction band was observed from the admittance spectral studies in the temperature range of 27–150°C. The origin of dielectric relaxation and defect concentration was attributed to the existence of the grain boundary defect, interface defect and shallow trap level in the films. An equivalent circuit was established which can well explain the AC response and identify the contribution of defects on electrical properties of BST thin film. From the viewpoint of trapping phenomena and dielectric relaxation analyses, we propose Ir as the optimum material for bottom electrode to withstand the post-annealing treatment. © 1998 Elsevier Science S.A. All rights reserved.

1. Introduction

Barium strontium titanate $(Ba_{0.47}Sr_{0.53})TiO_3$ (BST) thin films are one of the most promising materials for practical use in the capacitor of giga-bit dynamic random access memories (DRAMs) because of its high dielectric constant, low leakage current density, high dielectric breakdown strength, paraelectric perovskite phase do not exhibit fatigue, aging and the ease of composition control [1–9].

There are at least four possible defects, namely, the interface-defect at metal/BST Schottky junction [10], the grain boundary defect, oxygen vacancies and conduction electron existing in the metal/BST/metal capacitors, which may lead to dielectric relaxation as a function of frequency. The complex plane analysis is a valuable tool for the characterization of dielectric relaxation in ceramic capacitors. A semicircular fit of the AC data (Cole–Cole plot) in any plane suggests an appropriate equivalent R–C circuit that represents the observed spectra. Several works were recently carried out using this technique in thin film capacitors such as RuO_2/BST [11], RuO_2/PZT [12] and Pt/BST [13] to explain the nature of dielectric relaxation.

The bottom electrode materials greatly affect the electrical characteristic of the BST thin capacitor [14,15]. However, systematic studies of the effect of AC electrical response of BST thin films on various bottom electrodes are still lacking. In this work, we have investigated the effects of bottom electrodes (Pt, Ir, IrO_2/Ir, Ru, RuO_2/Ru) during deposition on the AC electrical response and the realistic equivalent circuit by three complex planes (capacitance, impedance and admittance) analyses in BST thin films without and with post-annealing, and propose them as optimum electrode materials. This paper also reports the observed shallow trap level and the total defect quantity of interface defect and grain boundary defect using admittance spectroscopy, which helps in better understanding of the effect of dielectric relaxation on electrical properties of BST films.

2. Defect traps in BST

The defect often leads to dielectric relaxation as a function of frequency, in which the dielectric constant decreases and loss tangent increases with increasing frequency. The defect traps of perovskite titanates may include three major

*Corresponding author. E-mail: tseng@cc.nctu.edu.tw

categories: grain boundary defect [16,17], interface defect at BST/metal interface [16,17] and shallow trap level [18,19]. In the case of grain boundary defect, it is considered that the grain boundary in dielectric ceramics represents a resistor R and the grain is a thin insulating layer C. There are many such RC series equivalent circuits in parallel throughout the ceramic. Based on the equivalent circuit analysis it indicates that the grain boundary plays a prominent role in the relaxation of ceramics. The grain boundary defect exists within the non-stoichiometry grain boundary and the dominant defect is the oxygen vacancy. In the case of interface defect, it exists within the forbidden gap due to the interruption of the periodic lattice structure. The positively charged oxygen vacancies with relatively high mobility, electromigrate toward the cathode under DC electric field. The oxygen vacancies then pile up at the front of the cathode and are compensated by the electron injected from the cathode. On the other hand, at the anode, an electrode reaction leads to generation of oxygen gas and electrons, leaving oxygen vacancies behind, and may cause an oxidation of electrode material. The reduction reaction leads to a growth of an *n*-conducting cathodic region toward the anode, and to an increase of electronic conductivity. The net result is that the space charge accumulation at grain boundaries and interface of BST/metal reduces the barrier height at grain boundaries and interface barrier height, and increases the leakage current and forms the dielectric relaxation. The details are given in reference [17].

The current induced by grain boundary defects is attributed to Poole–Frenkel conduction [10], and the current induced by interface defects is attributed to the Schottky emission [10,17]. The grain boundary defects and interface defects can be also determined by DC measurement and stress [10,17]. The energy of grain boundary defects and interface defects is about 0.25–0.35 eV [10] which is one order larger than the thermal energy (kT) 0.026–0.032 eV at 27–100°C, where k is the Boltzmann constant. Hence, the emission rate (grain boundary defect and interface defect) may be affected slightly by the temperature and approach nearly independent of temperature.

The shallow trap level can be determined under small-signal AC stress applied at various temperatures [19]. A level is referred to as an electron trapping state, when the predominant charge exchange is between the conduction band and the trap level. Under small-signal AC stress applied at the Schottky junction, the depletion layer width varies about its equilibrium position due to trapping and detrapping of electrons from the oxygen vacancies or shallow trap level, denoted by E_t [20]. The shallow trap level is near the conduction band, and hence its emission rate will be affected by temperature.

The band-diagram before contact for the Pt–BST–Pt system is shown in Fig. 1(a) where the BST film has smaller grain size [14] and the work function of Pt is 5.6 eV. Fig. 1(b) indicates the diagram for the Ru (bottom electrode)–BST–Pt (top electrode) system in which the BST
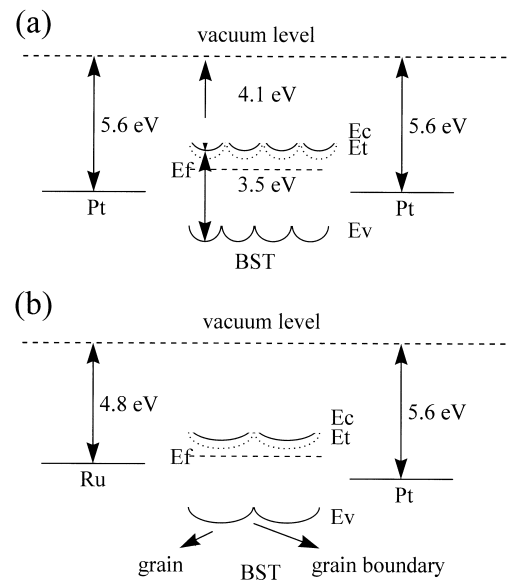

Fig. 1. The energy band situation in (a) Pt–BST–Pt, (b) Ru (bottom electrode)–BST–Pt (top electrode) system before contact.
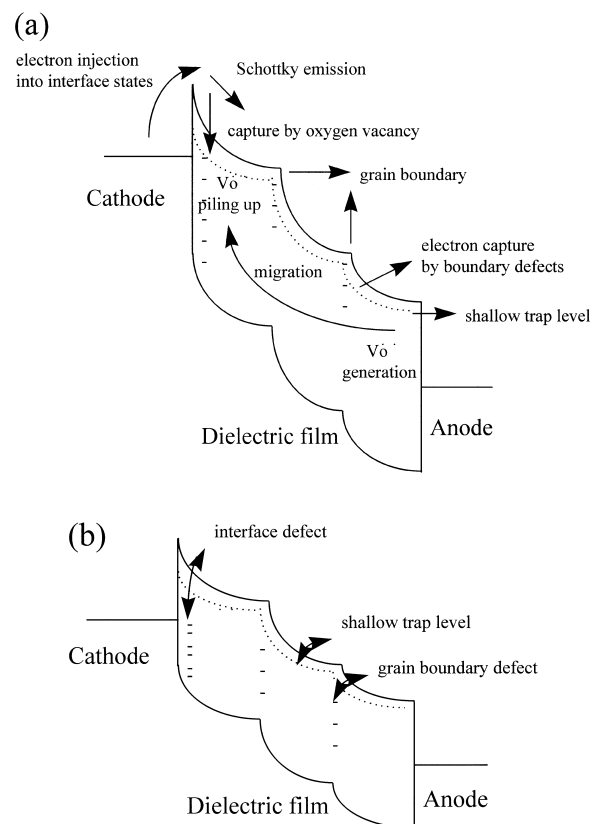

Fig. 2. Schematic band diagram for BST thin film capacitor for explaining (a) conduction and defect and (b) the catch and escape of the carriers on defects.

film has a larger grain size [14] and the work function of Ru is 4.8 eV. The electron affinity of BST is assumed to be 4.1 eV and the energy bandgap is 3.5 eV [21]. Fig. 2(a) shows the energy band after contact and the creation and

migration of defects, such as oxygen vacancies. The symbol '-' represents the electron captured by oxygen vacancy accumulated at the interface. The BST film on Pt has a large area of grain boundaries due to small grain size, and the grain boundaries would depress the oxygen vacancy migration which leads to the formation of the *n*-conducting region [16]. The barrier height at the interface of BST/Pt is larger such that there is higher resistance for the deterioration of the Schottky barrier. However, under a relatively high field, the migration and pilling up of oxygen vacancies near the cathode certainly lower the resistance of the Schottky junction. Fig. 2(b) indicates the catch and escape of the carriers in the grain boundary defect, interface defect and shallow trap level under the applied small-signal AC stress. The interface defect and grain boundary defect need larger escape-energy than the shallow trap level.

3. Complex-plane analysis

The electrical behavior of a capacitor may be expressed in terms of the admittance (Y) and impedance (Z) of a unit cube (with parallel plane electrodes) which can be defined by the following equations

$$Y = I(\omega)/V(\omega) = G_p(\omega) + jB_p(\omega) \tag{1}$$

$$Z = V(\omega)/I(\omega) = R_s(\omega) + jX_s(\omega) \tag{2}$$

$$Y = j\omega \times C(\omega) = j\omega \times (C' - jC'') = j\omega C_0 \times (\varepsilon' - j\varepsilon'') \tag{3}$$

Comparison of Eqs. (1)–(3) shows that the following relations hold,

$$G_p(\omega) = \omega C'' = \omega C_0 \varepsilon'' \tag{4}$$

$$B_p(\omega) = \omega C' = \omega C_0 \varepsilon' \tag{5}$$

where ω is the angular frequency, $I(\omega)$ and $V(\omega)$ the electrical current and applied voltage as a function of ω; $G_p(\omega)$ and $B_p(\omega)$ the parallel relative real admittance (conductance) and imaginary admittance as a function of ω; $R_s(\omega)$ and $X_s(\omega)$ the series relative real impedance (resistance) and imaginary impedance as a function of ω; C_0 the geometric capacitance in free space; ε' and ε'' the relative real and imaginary dielectric constant; C' and C'' the real and imaginary capacitance.

Fig. 3 shows the variation of C' and C'' of BST deposited on Pt with frequency in the measurement temperature range of 27–150°C. Resonance was observed at a frequency between 1 and 10 MHz. From this result, we can explain the large increase in the dielectric loss, as shown in Fig. 10(a). The resonance frequency for thickness mode is determined by electromechanical coupling factor and should be in the range of 1–10 GHz for BST films with a thickness of 0.5 μm. Therefore, the resonance observed in BST films cannot be attributed to piezoelectric resonance [9]. Another resonance can arise from the resonance of an
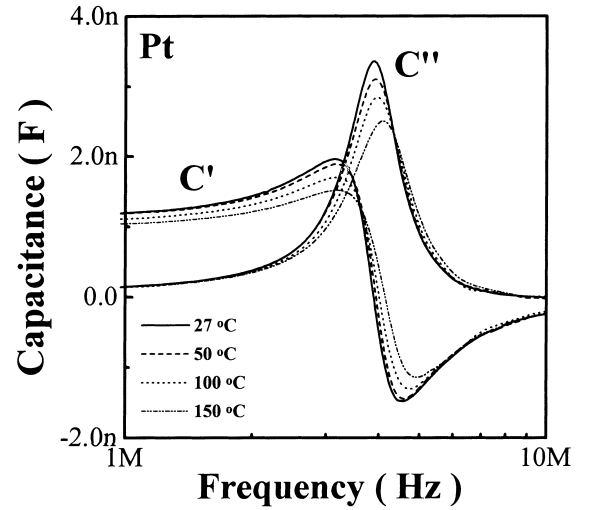

Fig. 3. Frequency dependence of relative real capacitance (C'), imaginary capacitance (C'') of BST thin films deposited on Pt bottom electrode at various temperatures.
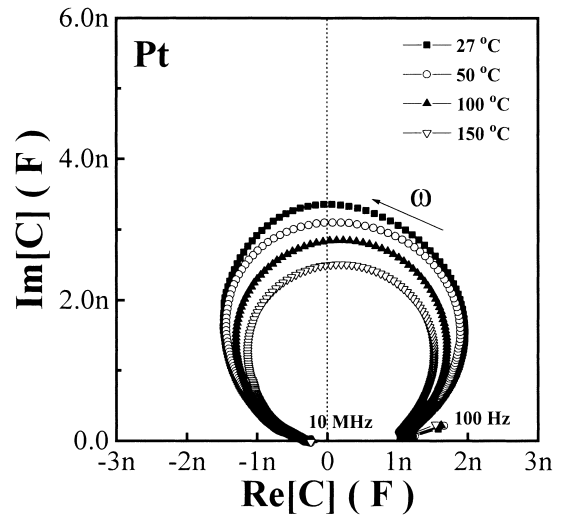

Fig. 4. Complex capacitance plot (C) of BST thin films deposited on Pt bottom electrode at various temperatures.
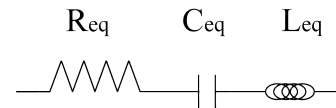

Fig. 5. The schematic equivalent circuit model for BST capacitor at frequency range from 100 Hz to 10 MHz.

electrical equivalent circuit. Fig. 4 shows the capacitance ($C(\omega)$) complex plane of BST deposited on Pt at various temperatures. We proposed a practical equivalent circuit for BST capacitors, as shown in Fig. 5 [22]. The resonance frequency of the electrical equivalent circuit $\omega_{re}(C' = 0)$ is determined by the following equation:
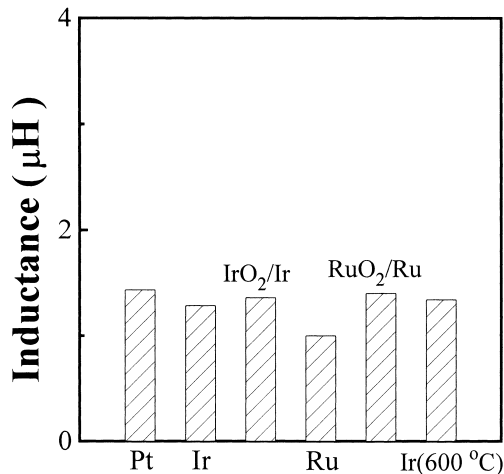
$$\omega_{re}(C' = 0) = (L_{eq}C_{eq})^{-1/2} \tag{6}$$

Fig. 6. Inductance of various bottom electrodes at frequency 100 kHz.

Fig. 7. Complex impedance plot (Z) of BST thin films deposited on Pt bottom electrode at various temperatures.

where L_{eq} and C_{eq} are the inductance and the capacitance of the equivalent circuit. The capacitance (C_{eq}) of the equivalent circuit is mainly determined by the capacitance of the BST film. The inductance (L_{eq}) of the equivalent circuit is determined by the conductivity of the electrode and BST film. But the resonance is not observed in BST films with a different range of capacitances, supporting the argument that the origin of the resonance is the equivalent circuit [9]. Therefore, this phenomenon is due to electrical resonance which is related to the electrode area of the films (255 μm diameter). Fig. 6 shows that the L_{eq} at 100 KHz for Pt, Ir, IrO$_2$/Ir, Ru, RuO$_2$/Ru and Ir(600°C) (BST on Ir annealed at 600°C for 20 min O$_2$ ambient after deposition) bottom electrodes at 27°C. And L_{eq} values of Pt, Ir, IrO$_2$/Ir, Ru, RuO$_2$/Ru and Ir(600°C) are about 1–14 μH. These L_{eq} values are the same at the frequency range from 100 Hz to 1 MHz.

The physical difference between relaxation and resonance lies in the fact that the latter corresponds to an oscillatory time domain response, where the discharge current changes signs periodically, and this is associated with the presence in the system of two complementary forms of energy storage. In R–C–L circuit the capacitance stores electrostatic energy while the inductance stores the magnetic energy, in its mechanical counterpart, the compliance stores potential energy, the inertia stores kinetic energy. In the case of an electromagnetic wave we have electrostatic and magnetic energies in the components of the electric and magnetic fields of the wave. These two energies may interchange, producing periodic oscillations which are damped through the dissipative processes, represented by the resistance R gradually reduce the total energy of the system. The other types of circuit consisting only of capacitances and conductances, cannot transfer energy to another form and therefore give in the time domain a continuous decay without overswing into the other sense of current flow. The resistance (R_{eq}) of the equivalent circuit
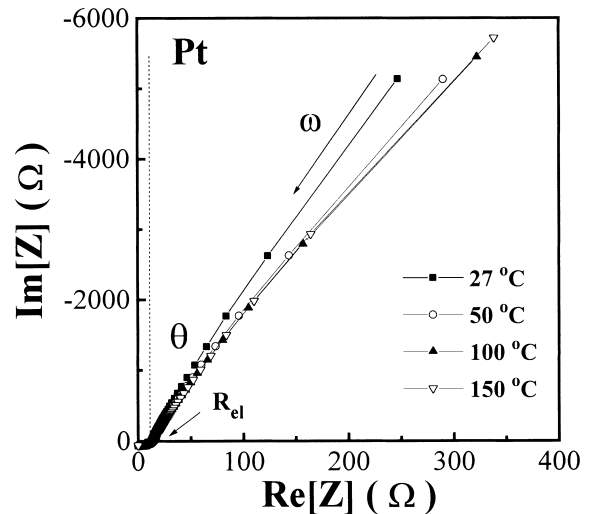
is determined by the resistance of electrode, grain boundary defect and interface defect.

The impedance (Z) of the equivalent circuit (Fig. 5) is

$$Z = R_{eq} + j\omega L_{eq} + 1/j\omega C_{eq} \tag{7}$$

For the frequency range of 100 Hz $\leq f \leq$ 1 MHz, the value of inductance can be neglected, because the ωL_{eq} value is 1–2 order smaller than the $1/\omega C_{eq}$ value. Hence, we can simplify the equivalent circuit consisting of only capacitance (C_{eq}) and resistance (R_{eq}). Fig. 7 shows the impedance (Z) complex plane plots of BST deposited on Pt at various temperatures. Fig. 8 shows the admittance (Y) complex plane plots of BST deposited on Pt at various temperatures. These Z and Y complex quantities can be expressed in terms
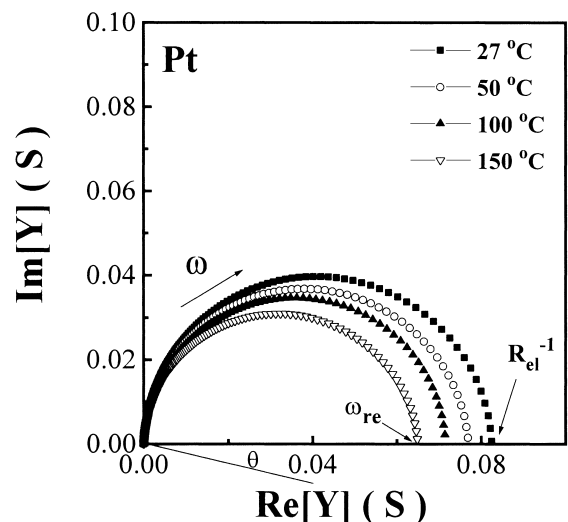

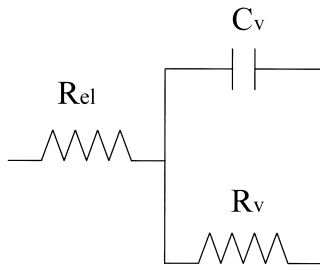Fig. 8. Complex admittance plot (Y) of BST thin films deposited on Pt bottom electrode at various temperatures.

Fig. 9. The schematic equivalent circuit model for BST capacitor at frequency range from 100 Hz to 1 MHz.

of G_p and C_p. C_p and G_p are the equivalent parallel capacitance and conductance of the entire circuit.

$$Z(\omega) = \text{Re}[Z] + j\text{Im}[Z] = R_s + jX_s \qquad (8)$$

$$Y(\omega) = \text{Re}[Y] + j\text{Im}[Y] = G_p + j\omega C_p \qquad (9)$$

The admittance (Y) data forms a semicircle, as shown in Fig. 8. Hence, the series RC combination appears to be a satisfactory representation of AC response for the frequency range of $100\,\text{Hz} \leq f \leq 1\,\text{MHz}$. On the basis of Z and Y planes analysis [22,23], we proposed a practical equivalent circuit for BST capacitors, as shown Fig. 9. The R_{el} represents the electrode resistance, C_v is the frequency-dependent capacitance due to the grain, and R_v is the frequency-dependent resistance due to grain boundary and interface. The frequency-dependent resistance R_v and capacitance C_v, where C_v is parallel with R_v can be determined as follows [23]:

$$G_p(\omega, T) = a(T) \times \omega^n = 1/R_v \qquad (10)$$

$$B_p(\omega, T) = b(T) \times \omega^n = \omega C_v \qquad (11)$$

$$n = 1 - (2\theta/\pi) \qquad (12)$$

$$R_s(\omega, T) = A(T) \times \omega^{-n} \qquad (13)$$

where n is a constant, a and b are the coefficients as a function of temperature, and θ is the depression angle of a semicircular response in the impedance (Z) and admittance (Y) complex planes. Thus by assuming an exponential distribution of $G_p(\omega,T)$ and $B_p(\omega,T)$, we are able to transform the total impedance into an equivalent circuit containing frequency dependent resistor, R_v, in parallel with a frequency dependent capacitor, C_v. The exponent n, which is extracted from the depression angle θ and suggested to be associated with the loss degree of the material, shows a temperature dependence similar to that of a useful parameter extracted from the AC conductivity-frequency measurements [24].

4. Experimental

BST thin films were deposited on metals/SiO$_2$/(100)Si (with Pt, Ir, IrO$_2$/Ir, Ru and RuO$_2$/Ru as bottom electrodes)

by RF magnetron sputtering. The starting p-type silicon wafer was cleaned by a standard initial cleaning process and chemically etched in a dilute HF solution. The 100 nm thick SiO$_2$ layer was thermally grown at 1050°C in a dry oxidation furnace. The metal layers on SiO$_2$/Si substrate with a thickness of 100 nm were deposited using a separate RF magnetron sputtering system. The Pt, Ir and IrO$_2$ films were prepared at a fixed power of 50 W (power density is 2.55 W cm^{-2}), constant pressure of 5 mTorr a substrate temperature of 350°C. The Ru and RuO$_2$ films were prepared at a fixed power of 100 W (power density is 5.1 W cm^{-2}), constant pressure of 10 mTorr and substrate temperature of 350°C. IrO$_2$ and RuO$_2$ films were formed by RF magnetron sputtering with Ar and O$_2$ mixture in the mixing ratio of 4:1. The measured resistivities of Pt, Ir, IrO$_2$, Ru and RuO$_2$ were about 16.9, 27.1, 67, 228 and 370 μΩ cm, respectively, at room temperature.

The BST (Ba/Sr = 0.5/0.5) targets with a diameter of 3 in. and a thickness of 1/4 in. were synthesized using standard solid-state reaction process. The sputtering chamber was evacuated to a base pressure of 2×10^{-6} Torr. All films were prepared at a fixed power of 100 W (power density is 2.26 W cm^{-2}) and constant pressure of 10 mTorr which was maintained by a mixture of argon and oxygen in the mixing ratio of 1 : 1 with a total flow of 20 sccm. All the BST films have the same thickness of around 80 nm. The substrate temperature of the sputtered BST films was at 500°C. The composition of BST thin films is Ba/Sr = 0.47/0.53. The compositional difference between target and thin film is due to sputtering yield. After deposition, the BST thin films were post-annealed at temperatures ranging from 500°C to 700°C in O$_2$ atmosphere using a quartz tube furnace (FN) for 20 min. Finally, the 50 nm thick top Pt electrodes with diameters of 165, 255 and 350 μm were sputter-patterned by the shadow mask process.

The film thickness was determined by ellipsometry. The structure was characterized by X-ray diffraction (XRD, Siemens D5000). On the basis of XRD data, the average grain size was determined by using Scherrer's formula [6]. The surface roughness and morphology were examined by atomic force microscopy (AFM, Digital Instruments NanoScope III). The capacitance–voltage (C–V) characteristics were measured on the metal–insulator–metal (MIM) structure by measuring the capacitance at 100 kHz as a function of a swept positive-to-negative voltage bias. Dielectric constant of the films was calculated from the capacitance measured at 100 kHz without bias voltage. The admittance and impedance spectra were measured as a function of frequency with a Hewlett–Packard (HP) 4194A impedance gain phase analyzer and the temperature was varied from 27 to 150°C. The AC electrical data, in the form of parallel capacitance and conductance, were recorded in the frequency range of 100 Hz–10 MHz at an AC signal amplitude of 0.1 V.

5. Results and discussion

The bottom electrode had a pronounced effect on the dielectric constant and the leakage current density of the BST films measured at 100 kV cm^{-1} with a delay time of 30 s. It has been indicated in a previous study that the BST film deposited on Ru bottom electrode had a maximum dielectric constant of 548 and leakage current density of 3.94×10^{-7} A cm^{-2} [14]. The BST film deposited on Pt bottom electrode had the minimum dielectric constant of 219 and leakage current density of 2.2×10^{-8} A cm^{-2}. The leakage current of BST thin films was expected to be affected by contact potential barrier and polarization loss. The details were described before [14]. It has also been shown that the dielectric constant and leakage current of BST thin films were dependent on the post-annealing temperature. The BST films deposited on Pt, Ir, IrO$_2$/Ir and RuO$_2$/Ru after post-annealing were more stable than BST on Ru. From the viewpoints of the dielectric constant, leakage current and reliability, the optimum material for the bottom electrode with post-annealing is Ir. The details were given in reference [15].

Fig. 10(a) shows the variation of ε', ε'', and loss tangent (tan$\delta = \varepsilon'/\varepsilon''$) of BST deposited on Pt with frequency in the measurement temperature range of 27–150°C. The ε' decreases from a high value at low frequency to a low value at high frequency and the curve has an inflective point. The ε' becomes a negative value after inflective frequency because the inductance (L_{eq}) of the equivalent circuit determined by the conductivity of the electrode dominates. And the ε' decreases with increasing temperature before the inflective frequency because the Curie temperature of BST (Ba/Sr = 0.47/0.53) is lower than room temperature. The ε'' and loss tangent have the same peak values at frequencies $(\omega_{re} = \tau_{re}^{-1})$ about 3.89, 3.95, 4.00 and

4.15 MHz, at temperatures 27°C, 50°C, 10°C and 150°C, respectively. The peak frequency (ω_{re}), which was reported to be located near the emission rate of a trap [18,19], increases with increasing temperature. But the dielectric constants (ε' and ε'') are almost independent of the temperature and frequency for the frequency range of 100 Hz $\leq f \leq$ 1 MHz, as shown in Fig. 10(b), and the details will be mentioned later.

The conductance G_p of a Schottky junction can be described as a sum of the shallow trap conductance G_{ts}, the deep trap conductance G_{td} (grain boundary defect and interface defect) and DC component G_{DC} [18,19],

$$G_p(\omega, T) = G_{DC} + G_{td}(\omega) + G_{ts}(\omega, T) \qquad (14)$$

By applying a small AC signal and varying the temperature, the peak of G_p/ω vs. ω or ε'' vs. ω (Eq. (4)) occurs when the angular frequency of an AC signal equals the emission rate (e_n) of electron transition in the trapping state [18,19]. The time dependence of the charge transition is expressed via the relation,

$$\tau_{re}^{-1} = \omega_{re} = e_n = e_{n0}\exp[-(E_c - E_t)/kT] \qquad (15)$$

where ω_{re} the peak frequency, τ_{re} the relaxation time, E_c the energy at the bottom of the conduction band, k the Boltzmann constant, E_t the shallow trap level energy. Fig. 11 shows the G_p/ω vs. ω of BST/Pt thin film at various temperatures. The peak frequency (ω_{re}) increases with increasing temperature. On the basis of Eq. (15), the activation energies, ($E_c - E_t$), can be obtained from the slopes of the linear regions of the plots ln(ω_{re}) vs. 1000/T (Fig. 12), respectively, in the BST deposited on Pt, Ir, IrO$_2$/Ir, Ru, RuO$_2$/Ru, and Ir(600°C) on the basis of the Arrhenius plot. Fig. 13 depicts the ($E_c - E_t$) values of BST deposited on various bottom electrodes. The measured ($E_c - E_t$) values of Pt(5.14 meV), Ir(4.19 meV), IrO$_2$(5.13 meV),
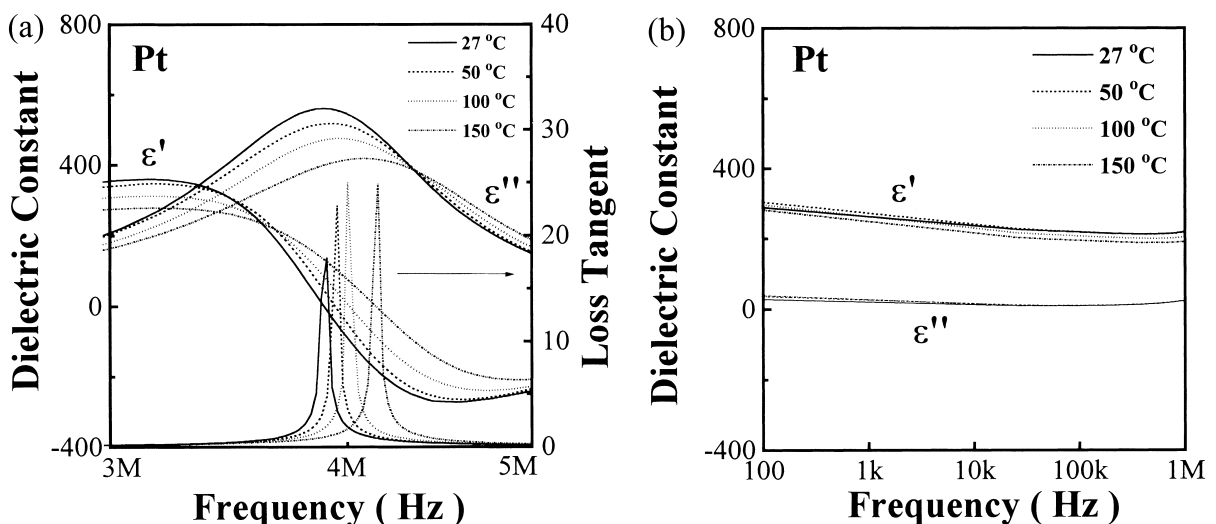

Fig. 10. Frequency dependence of relative real dielectric constant (ε'), imaginary dielectric constant (ε'') and loss tangent (tan$\delta = \varepsilon''/\varepsilon'$) of BST on Pt at various temperatures. (a) 3–5 MHz and (b) 100 Hz–1 MHz.
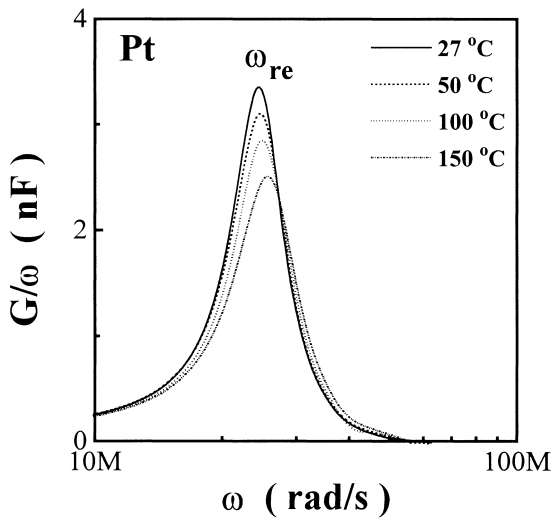
Fig. 11. $G(\omega)/\omega$ of BST on Pt as a function of frequency at various temperatures.
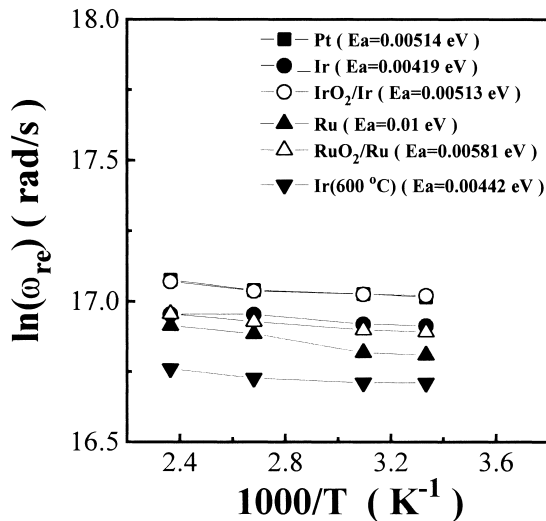

Fig. 12. An Arrhenius plot of $\ln(\omega_{re})$ vs. $1000/T$ of BST deposited on various bottom electrodes for obtaining the trap activation energy (E_t).
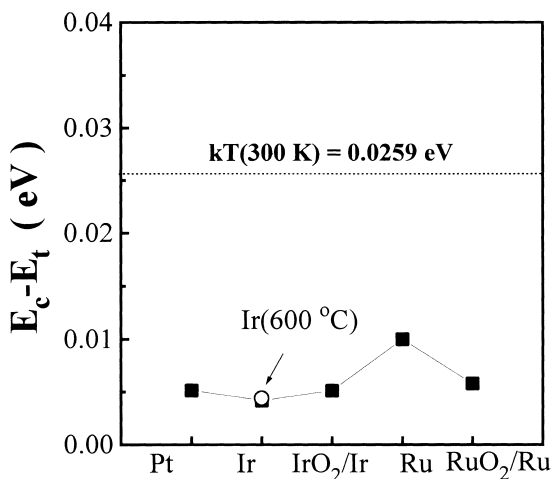

Fig. 13. $E_c - E_t$ of BST deposited on various bottom electrodes.

Ru(10 meV), RuO_2 (5.81 meV) and Ir(600°C)(4.42 meV) are smaller than the thermal energy (kT) 25.9 meV at 27°C. The electrons in the trap states gain sufficient energy at room temperature and exchange between the conduction band and the shallow trap level. The shallow trap level cannot trap any electrons which can move freely between the conduction band and the shallow trap level. Therefore, the effect of the shallow trap level can be neglected at the normal temperature range of DRAM operation: 0–70°C ambient and 0–100°C on chip. From the viewpoint of the trapping phenomena, the contribution of the shallow trap level on the electrical properties of BST thin film would be absent for the frequency range of 100 Hz $\leq f \leq$ 1 MHz, and the details were mentioned later. Hence, we propose that the shallow trap level term is not included in the equivalent circuit of BST thin film in the frequency range of 100 Hz $\leq f \leq$ 1 MHz. The equivalent circuit of BST thin film has contribution from the grain, grain boundary defect and interface defect of BST/metal.

Fig. 14(a)–(c) show the $G_p(\omega,T)$ and $B_p(\omega,T)$ of BST thin films deposited on Pt, Ir and Ru with frequency (100 Hz $\leq f \leq$ 1 MHz) at various temperatures. The G_p and B_p approach is independent of the temperature, so that the $a(T)$ and $b(T)$ values can be expressed as a constant at various temperatures, the C_v and R_v can be almost independent of the temperature for 100 Hz–1 MHz on the basis of Eqs. (10) and (11). The result is the same with Fig. 10(b). The log(G_p) vs. log(ω) curves are almost parallel to the log (B_p) vs. log(ω) curves, from which we can obtain the n values. Hence, the contribution of the shallow trap level on the electrical properties of BST thin film is absent for the frequency range of 100 Hz $\leq$ f $\leq$ 1 MHz because C_v and R_v can be almost independent of the temperature. Therefore, the equivalent circuit of BST thin film has contributions only from grain, grain boundary defect and interface defect of BST/metal.

Table 1 lists the related parameters of the equivalent circuit of the plots shown in Figs. 7–9 and 14 at various temperatures. The frequency dependent resistance R_v and capacitance C_v were calculated on the basis of Eqs. (10) and (11). The electrode resistance R_{el} of various bottom electrodes increases with increasing temperature because metal resistance increases with increasing temperature. The electrode resistance R_{el} of Ru has the maximum value because the Ru electrode may be slightly oxidized during BST deposition at high oxygen ratio, as indicated from XRD and SIMS data [14,15]. As the n values of BST on Pt, Ir, IrO_2/Ir, RuO_2/Ru and Ir(600°C) approached 1, the measured C_v except the Ru case will be almost independent of frequency (100 Hz $\leq f \leq$ 1 MHz), as shown in Fig. 15. The result is same with Fig. 10(b). The n value of BST on Ru is 0.475, the C_v will decay with increasing frequency (Fig. 15) and the slope is -0.59 which is about ($n-1$) value. Hence, the BST on Ru has larger dielectric relaxation. The measured R_s of BST deposited on various bottom electrodes decreases with increasing frequency, as shown in Fig. 16,
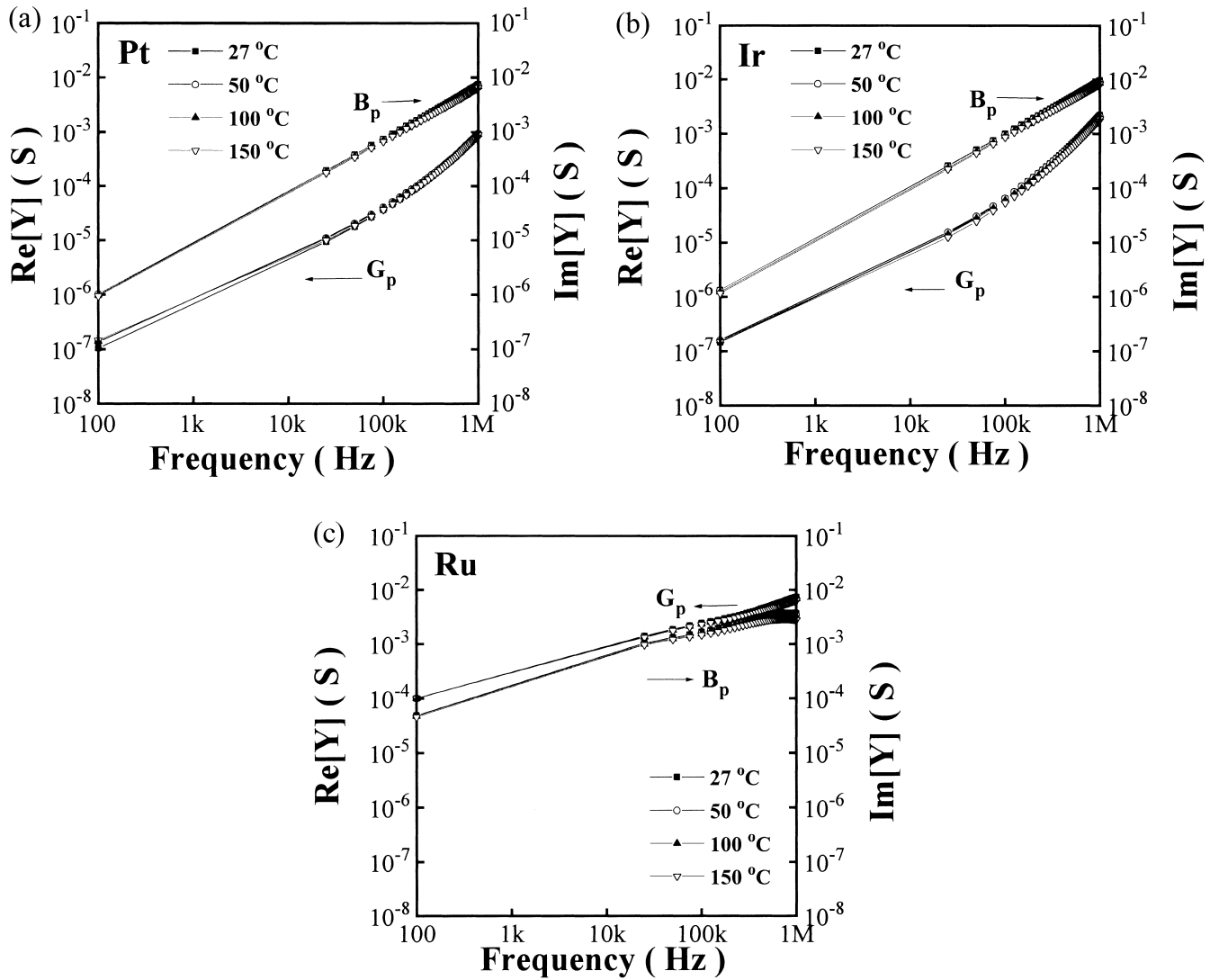
Fig. 14. The $G_p(\omega,T)$ and $B_p(\omega,T)$ of BST thin films deposited on (a) Pt, (b) Ir and (c) Ru with frequency at various temperatures.

Table 1
Calculated parametric values of the equivalent circuit shown in Figs. 7–9 and 14 at various temperatures extracted from analyses of the Y and Z planes

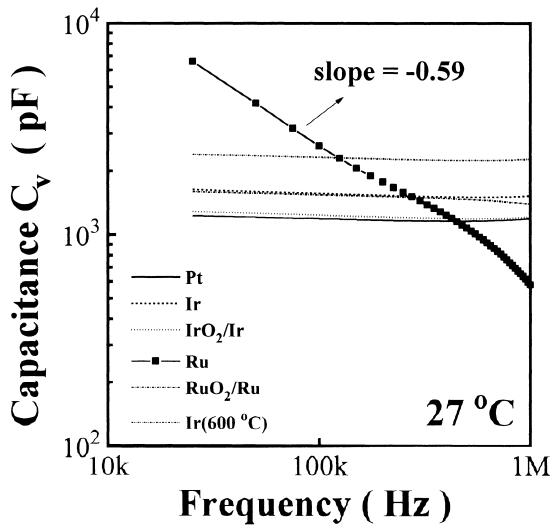|	Bottom electrode	Pt	Ir	IrO_2/Ir	Ru	RuO_2/Ru	Ir(600°C)
	a (S s^n rad^{-n})	6.26×10^{-11}	9.95×10^{-11}	6.69×10^{-11}	4.26×10^{-6}	1.06×10^{-10}	1.52×10^{-10}
	b (S s^n rad^{-n})	1.89×10^{-9}	2.51×10^{-9}	1.98×10^{-9}	2.82×10^{-6}	2.34×10^{-9}	5.6×10^{-9}
	n	0.96928	0.96479	0.96715	0.47556	0.97017	0.93861
27°C	R_{el} (Ω)	12.14	17.98	9.4	83.9	34.4	17.9
	θ (degree)	2.559	3.06	2.96	50.46	2.277	1.75
50°C	R_{el} (Ω)	13	18.6	9.5	88.4	35.2	18.74
	θ (degree)	2.718	3.06	2.97	50.46	2.277	1.75
100°C	R_{el} (Ω)	13.9	19.68	9.6	95.1	36.52	20.47
	θ (degree)	2.719	3.06	2.96	50.47	2.278	1.75
150°C	R_{el} (Ω)	15.3	20.6	9.7	102.2	38	22.52
	θ (degree)	2.718	3.06	2.96	50.46	2.279	1.75

Fig. 15. Capacitance C_v of BST thin films deposited on Pt, Ir, IrO$_2$/Ir, Ru, RuO$_2$/Ru and Ir(600°C) with frequency at room temperature.
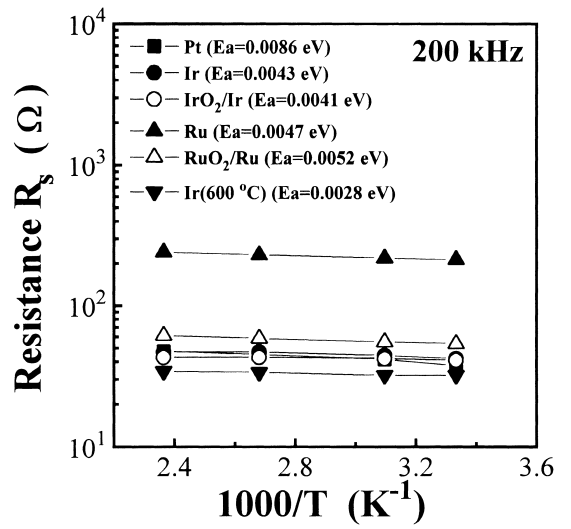

Fig. 17. An Arrhenius plot of R_s vs. 1000/T of BST deposited on various bottom electrodes for obtaining the activation energy.
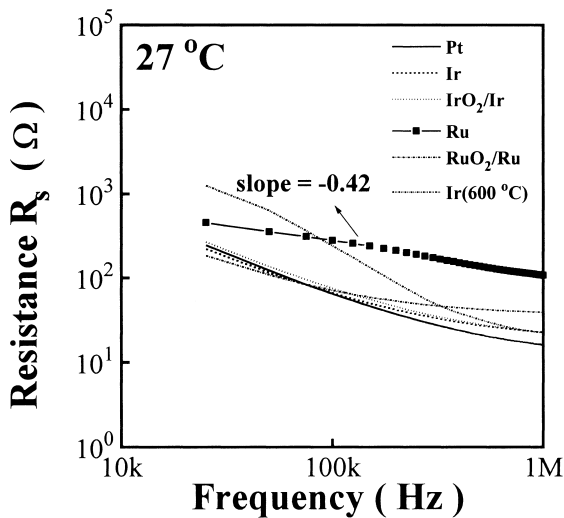

Fig. 16. Resistance R_s of BST thin films deposited on Pt, Ir, IrO$_2$/Ir, Ru, RuO$_2$/Ru and Ir(600°C) with frequency at room temperature.

and the slope of BST/Ru is -0.42 which is about $-n$ value. On the basis of Eq. (13), the activation energies can be obtained from the slopes of the linear regions of the plots, log(R_s) vs. 1000/T (Fig. 17) for the BST deposited on Pt, Ir, IrO$_2$/Ir, Ru, RuO$_2$/Ru, and Ir(600°C), respectively, on the basis of the Arrhenius plot. The values of R_s are almost independent of the temperature.

The resistance (R_{eq}) of the equivalent circuit is determined by the resistance of the electrode, grain boundary defect and interface defect. The resistance (R_{eq}) consists of contribution from R_v and R_{el}. R_v is the frequency-dependent resistance due to grain boundary and interface. The grain boundary defect and the interface defect of BST/metal are considered to be a donor when it becomes neutral or positive by donating an electron. When an AC voltage is applied the

defect levels move up or down with respect to the valence and conductance bands while the Fermi level remains fixed. A change of charge in the defect occurs when it crosses the Fermi level. The value of G_p/ω is C'' by Eqs. (10) and (4). Once C'' is known (Fig. 3), the defect density is obtained by using the relation $D_{df} = C''/qA$, where A is the metal plate area and q the elementary charge [25]. Fig. 18 shows the defect density of grain boundary defect and interface defect of BST deposited on various bottom electrodes. The defect density of BST on Ru is larger than that of other bottom electrodes. Hence the dielectric relaxation of BST on Ru is more serious than those of BST deposited on other bottom electrodes. The results (Fig. 18) have a good agreement with the results shown in Figs. 15 and 16.

The depression angle θ of a semicircular response in the impedance (Z) and admittance (Y) complex planes is non-
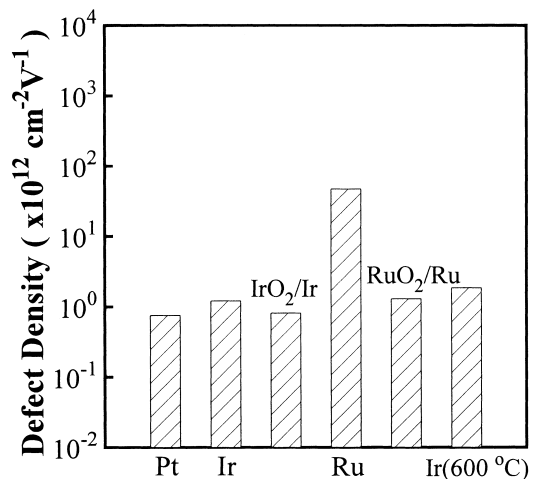

Fig. 18. Defect density of BST deposited on various bottom electrodes.

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zero, which corresponds to the distribution of relaxation time as reported [26] and reflects the degree of uniformity in the conductance relaxation. Joncher [27] showed that θ is related to the extent of the screening effect caused by the hopping charges when it cannot follow the changes of polarization brought about by an alternating electric field. The θ values of BST of Pt, Ir, IrO_2/Ir, Ru, RuO_2/Ru and Ir(600°C) are about 2.7, 3.06, 2.97, 50.46, 2.27 and 1.75 degree, respectively, at various temperatures (Table 1). The θ value of BST on Ru has the maximum value. That means the BST on Ru has larger loss degree of the material. On the other hand, the θ value of BST on Ir(600°C) has the minimum value. Therefore, the BST on Ir(600°C) presents smaller screening effect. Taking account of a DRAM application, the dielectric relaxation would result in less than 10% loss of storage charge during the refresh cycle. From the viewpoints of the dielectric constant, leakage current, trapping phenomena, dielectric relaxation, the depression angle and leakage resistance, the optimum material for the bottom electrode with post-annealing is Ir, because the BST on Ir(600°C) has a large dielectric constant, smaller dielectric relaxation and larger leakage resistance, as shown in Figs. 15 and 16.

6. Conclusions

The trapping dielectric relaxation and defect quantity of BST thin films deposited on various bottom electrodes, such as Pt, Ir, IrO_2/Ir, Ru, RuO_2/Ru before and after annealing in O_2 ambient were explored through the measurement of dielectric dispersion as a function of frequency (100 Hz $\leq f \leq$ 10 MHz) and temperature (27°C $\leq T \leq$ 150°C). An equivalent circuit was proposed on the basis of the admittance and impedance spectra, which can well explain the AC response and identify frequency-dependent resistance on the electrical properties contributed by the defects of BST thin film. A shallow trap level located at 0.005–0.01 eV below the conduction band was observed from the admittance spectral studies in the temperature range of 27–150°C. The grain boundary defect and interface defect existed in the films were the major origin of dielectric relaxation and defect concentration. From the viewpoints of the dielectric constant, leakage current, trapping phenomena, dielectric relaxation, and the depression angle, Ir is the optimum material for the bottom electrode with post-annealing.

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