A New Approach to Simulating n-MOSFET Gate Current Degradation by Including Hot-Electron Induced Oxide Damage

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***Abstract*—A new gate current model which considers the hot-electron induced oxide damage in n-MOSFET's was developed for the first time. The spatial distributions of oxide damage, including the interface state $(N_{\rm it})$ and oxide trapped charge $(Q_{\rm ox})$, were characterized by using an improved gated-diode current measurement technique. A numerical model feasible for accurately simulating gate current degradation due to the stress generated $N_{\rm it}$ and $Q_{\rm ox}$ has thus been proposed. Furthermore, the individual contributions of $N_{\rm it}$ and $Q_{\rm ox}$ to the degradation of gate current can thus be calculated separately using these oxide damage. For devices stressed under maximum gate current biases, it was found that the interface state will degrade the gate current more seriously than that of the oxide trapped charge. In other words, the interface states will dominate the gate current degradation under $I_{G,\max}$. Good agreement of the simulated gate current has been achieved by comparing with the measured data for pre-stressed and post-stressed devices. Finally, the proposed degradation model is not only useful for predicting the gate current after the hot-electron stress, but also provides a monitor that is superior to substrate current for submicron device reliability applications, in particular for EPROM and Flash EEPROM devices.**

I. Introduction

Channel-hot-electron injection (CHEI) into the gate oxide has been recognized as a major limitation to the long term reliability of short channel n-MOSFET devices. In particular, it has also been widely used as the programming method in EPROM's and Flash EEPROM's. Therefore, an understanding of the hot electron related issues becomes of great importance to the device design and reliability study. In recent years, many experimental techniques and theoretical models have been developed to explore and investigate the physics of CHEI through gate leakage current measurement [1]–[3]. However, most of them are focused on the modeling of devices without incurring any hot-electron stress. In other words, the effects of hot-electron stress-induced oxide damage, including interface states $(N_{\rm it})$ and oxide trapped charges $(Q_{\rm ox})$, on the gate current have not been reported in the literature. The difficulties for developing a gate current model of MOS devices after the stress are twofold. One is the difficulty in determining stress generated oxide damage. The other one is the unknown correlation between the gate current and generated oxide damage.

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In terms of the oxide damage characterization, many efforts have been devoted to determine their spatial distributions [4]–[6]. But, most of them are focused on the characterization of the localized $N_{\rm it}$ near the drain region only [4]. Quite a few studies [5]–[6] are able to simultaneously extract $N_{\rm it}$ and $Q_{\rm ox}$. Recently, we have successfully demonstrated a method to separate $Q_{\rm ox}$ from $N_{\rm it}$ such that the study of these two oxide damage on the gate current degradation becomes feasible [7]. As a consequence, the investigation of the gate current degradation due to hot-carrier stress becomes possible.

On the other hand, to investigate the degradation mechanism of gate current after the stress, Marchetaux *et al.* [8] observed that the gate current decreases with the aging time. However, due to a lack of the damage profiling technique, the degradation mechanism and model of gate current have never been presented. More recently, the degradation mechanism of gate current and its impact on Flash EEPROM devices, such as the cell programming speed retardation and the operation window closure, have been proposed by an indirect experimental observation [9]. Furthermore, Peng *et al.* [10] proposed a physically-based interface state and oxide charge generation models for simulating the gate current after the stress. However, both of them cannot explain the experimental data in [8].

In this paper, a new gate current degradation model which considers the hot-electron stress generated $N_{\rm it}$ and $Q_{\rm ox}$ will be proposed. The spatial distributions of both $N_{\rm it}$ and $Q_{\rm ox}$ will be first calculated using an improved gated-diode current measurement technique that we developed in [7]. Then, the individual contributions of $N_{\rm it}$ and $Q_{\rm ox}$ to the degradation of gate current will be studied. Section II describes the device conditions used in this work. The technique for characterizing the oxide damage is described in Section III. The proposed new gate current model is shown in Section IV. Results and discussion are presented in Section V. Section VI gives the summary and conclusions.

II. Device Preparation

The devices used in this study were fabricated by 0.35-μm CMOS technology. The test samples have mask length

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$L_{\rm mask} = 0.5$ μm, mask width $W_{\rm mask} = 20$ μm, and gate oxide thickness $t_{\rm ox} = 7$ nm. The device threshold voltage was adjusted by using BF_2 implant with an energy of 25 keV and a dose of 3×10^{12} cm^{-2}. The conventional n$^+$ source/drain structure was performed by using Arsenic implant with an energy of 80 keV and a dose of 5×10^{15} cm^{-2}. The simulated channel profile and source/drain profile have been calibrated against SIMS data.

III. Oxide Damage Profiling Technique

In order to investigate the gate current characteristics after the hot-carrier stress, the stress-generated $N_{\rm it}$ and $Q_{\rm ox}$ should be determined first. We used an improved gated-diode measurement technique that we developed recently in [7] to separate $N_{\rm it}$ and $Q_{\rm ox}$. Its basic principle will be summarized as follows.

We first stressed the device at the maximum gate current bias since the gate current at this bias is of great interest to us for practical applications such as nonvolatile memories which use this maximum gate current for programming purposes. Under such bias stress condition, both $N_{\rm it}$ and $Q_{\rm ox}$ will be generated [7]. The measurement method is based on the gated-diode current measurement technique as illustrated in Fig. 1(a). By applying a small negative voltage on the drain side with source floating, and by sweeping the gate voltages from zero to more negative values, the gated-diode current $(I_{\rm GD})$ can be measured from the drain. The notations ϕ_e and ϕ_h shown in Fig. 1(a) represent the quasi-Fermi levels for electrons and holes respectively, which coincide with the intrinsic level E_i. The region Δx at the surface between ϕ_e and ϕ_h shows where electron and hole recombination occurs. For a certain applied gate voltage, the region Δx is dependent on the drain voltage. The more negative the applied drain voltage, the larger the electron/hole recombination region becomes. Therefore, the measured $I_{\rm GD}$ is easier to be observed by using more negative drain voltage without sacrificing the accuracy. But, Speckbacher *et al.* [11] suggest that the applied drain voltage greater than -0.3 V is better. In this paper, the applied drain voltage of -0.2 V is used. For a fresh device, its $I_{\rm GD}$ is shown in Fig. 1(b) as solid lines. After the maximum gate current stress, $I_{G,\max}$, both $N_{\rm it}$ and $Q_{\rm ox}$ will be generated, and an excess recombinaion of electron and hole in the region Δx will give rise to an increasing $I_{\rm GD}$ (as shown in dashed lines of Fig. 1(b). In the meantime, the generated $Q_{\rm ox}$ will not contribute to the recombination current but will affect the parameters ϕ_e and ϕ_h at the surface. In order to separate $Q_{\rm ox}$ from $N_{\rm it}$, we use a detrapping or neutralization technique to achieve this purpose, i.e., by applying hot hole injection from the drain to the gate oxide, until $Q_{\rm ox}$ was filled and eliminated totally. The $I_{\rm GD}$ current will shift to the left [as shown in solid circles in Fig. 1(b)] with a negative oxide trapped charge in this study. If $Q_{\rm ox}$ is totally eliminated, the $I_{\rm GD}$ current difference between fresh (solid lines) and detrapped (solid circles) curves is caused by $N_{\rm it}$ alone. The difference between the stressed (dashed lines) and detrapped/neutralized (solid circles) $I_{\rm GD}$ currents can be used to determine the values of $Q_{\rm ox}$.

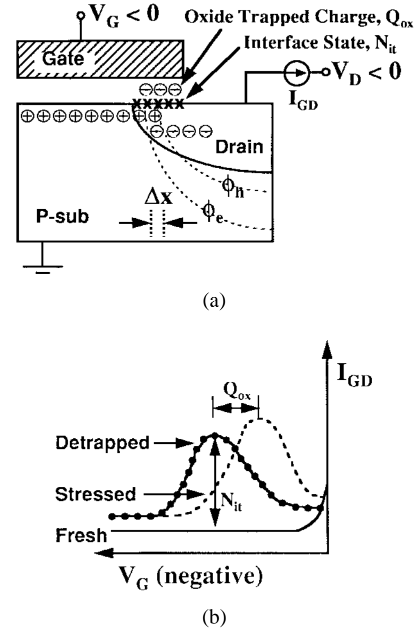

Fig. 1. (a) Schematic diagram of the present gated-diode current measurement technique. (b) The qualitative expression of the measured gated-diode currents ($I_{\rm GD}$) for fresh (solid lines), hot-electron stressed (dashed lines), and detrapped/neutralized (solid circles) conditions.

The equations to calculate $N_{\rm it}$ and $Q_{\rm ox}$ are given as follows. First, from the difference of the two curves (solid lines and circles), the equation used to calculate $N_{\rm it}$ is given by [7]

$$\Delta I_{\rm GD}(V_G) = \frac{1}{2} q W v_{\rm th} \sigma \Delta N_{\rm it}(x) \Delta x(V_G) n_i \exp\left(\frac{q|V_D|}{2kT}\right) \tag{1}$$

where W is the device channel width and $v_{\rm th}$ and σ represent the thermal velocity and the defect capture cross section, respectively. n_i is the intrinsic carrier concentration and Δx represents the region where electron-hole recombination occurs and is a function of the gate voltages. From the difference of the two curves (dashed lines and solid circles) in Fig. 1(b), a modified form of (1) to calculate $Q_{\rm ox}$ can be obtained from

$$\Delta I_{\rm GD}(V_G) = \frac{1}{2} q W v_{\rm th} \sigma \Delta N_{\rm it}(x) \Delta x\left(V_G + \frac{Q_{\rm ox}}{C_{\rm ox}}\right) n_i \times \exp\left(\frac{q|V_D|}{2kT}\right) \tag{2}$$

where the recombination region Δx varies as a function of gate voltages and oxide trapped charges $Q_{\rm ox}$. Δx can be determined from two-dimensional (2-D) device simulation. Based on the above two equations, both $N_{\rm it}$ and $Q_{\rm ox}$ can be determined.

IV. Gate Current Degradation Model

The measured gate and substrate currents as a function of stress time are shown in Fig. 2. The stress conditions are biased at the maximum gate current ($I_{G,\max}$@$V_{\rm GS} = 5.5$ V and $V_{\rm DS} = 5$ V) and at the maximum substrate current ($I_{B,\max}$@$V_{\rm GS} = 2$ V and $V_{\rm DS} = 5$ V), respectively. The gate current (I_G) is measured at $V_{\rm GS} = 5.5$ V and $V_{\rm DS} = 5$ V.

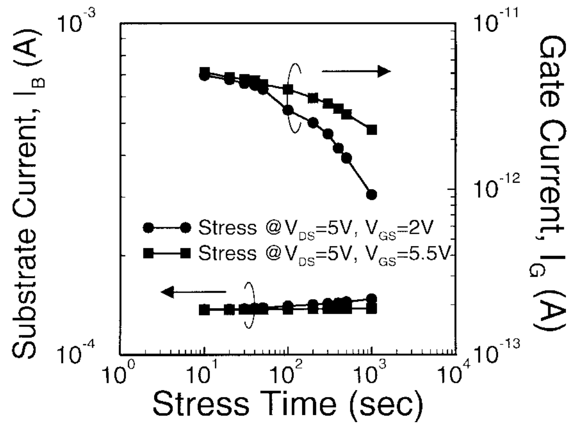

Fig. 2. Measured gate and substrate currents as a function of stress time. The stress conditions are biased at maximum substrate current ($I_{B,\max}$) and maximum gate current ($I_{G,\max}$).

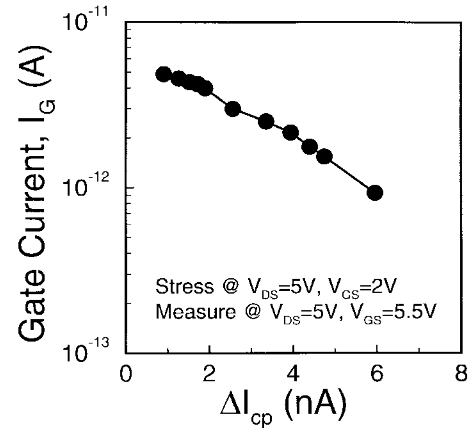

Fig. 3. Correlation between measured gate current and charge-pumping current variation after $I_{B,\max}$ stress.

The substrate currents (I_B) are measured at $V_{\rm GS} = 2$ V and $V_{\rm DS} = 5$ V. As seen from Fig. 2, we observe that I_B increases slightly with the stress time but I_G decreases. The increase of I_B is attributed to the enhancement of local electric field as well as the electron energy caused by the generation of $N_{\rm it}$ and $Q_{\rm ox}$. However, it cannot explain the decay of I_G [3], [10]. Also, we found that the variation of both I_G and I_B after $I_{B,\max}$ stress is significantly greater than that after $I_{G,\max}$ stress. Here, it should be noted that at $I_{B,\max}$ stress condition $Q_{\rm ox}$ will not be generated. Therefore, the generation of $N_{\rm it}$ at $I_{B,\max}$ as well as $I_{G,\max}$ will cause an apparent degradation of I_G. Reported results [10] did not provide the correlation between gate current degradation and $N_{\rm it}/Q_{\rm ox}$. Therefore, here we propose a new degradation model of gate current by considering the effects of both $N_{\rm it}$ and $Q_{\rm ox}$ as follows.

The generation of channel-hot-electron injection induced gate current includes several steps: 1) channel electrons gain energy from field and become "hot"; 2) redirection of hot electrons due to the scattering; 3) hot electrons surmount the Si/SiO_2 potential barrier and are injected into the oxide; and finally 4) hot electrons are collected by the gate. According to this, the gate leakage current model for devices without considering any hot-electron stress can be described by [3]

$$J_G = \int_{\Phi_b}^{\infty} qnv_z(w_n)f(w_n)\,dw_n \qquad (3)$$

where q is the electronic charge, n is the electron concentration, and w_n is the electron energy calculated by energy balance equations. Φ_b represents the potential barrier height for the electrons to overcome the barrier. $v_z(w_n)$ and $f(w_n)$ represent the electron velocity in the direction normal to the Si/SiO_2 interface and the electron energy distribution (EED) function, respectively. As $N_{\rm it}$ and $Q_{\rm ox}$ are generated after the stress, they will increase the lateral electric field as well as the electron energy (from the increase of substrate current). Therefore, $v_z(w_n)$ and $f(w_n)$ after the stress will be larger than those before the stress. Carrier concentration will also be reduced as a result of $N_{\rm it}$ which can be supported by 2-D simulation. As a result, for the increase of w_n and the reduction of carrier concentration due to $N_{\rm it}$, the simulated gate current will increase as described in [10, eq. (3)]. However, it is in contradiction to the measured data in Fig. 2 here. And hence, it is believed that there is another factor responsible for the degradation of gate current as seen from Fig. 2.

In Fig. 3, the measured gate currents after $I_{B,\max}$ stress have been shown as a function of charge-pumping current variation (or interface states $N_{\rm it}$). According to Fig. 3 and the correlation of $I_{\rm CP}$ and $N_{\rm it}$, $\Delta I_{\rm CP} = qA_G f\Delta N_{\rm it}$, the correlation between gate current and $N_{\rm it}$ is drawn as an exponential relationship. The factor $e^{-\alpha_{\rm nit}\Delta N_{\rm it}}$ is proposed and regarded as Coulomb scattering due to trapped interface-state charges as described in [12]. In other words, the generated interface states filled with the electrons can be served as Coulomb scattering centers and then suppress the hot-electron injection capability. In addition, the generated $Q_{\rm ox}$ trapped in the oxide after $I_{G,\max}$ stress will also inhibit the hot-electron injection probability. Here, we consider the effects of generated $Q_{\rm ox}$ on the changes of the effective potential barrier height of hot-electron injection at the Si/SiO_2 interface. Therefore, the gate current model which considers the effects of generated $N_{\rm it}$ and $Q_{\rm ox}$ can be formulated as

$$J_G = \int_{\Phi_b}^{\infty} qnv_z(w_n)f(w_n){\rm exp}(-\alpha_{\rm nit}\Delta N_{\rm it}(x))\,dw_n \qquad (4)$$

where $\alpha_{\rm nit}$ is a fitting parameter for the gate current simulation by considering the $N_{\rm it}$ effect. The effective potential barrier height Φ_b, which considers the stress generated $Q_{\rm ox}$ can be modified as

$$\Phi_b = 3.2 - 2.59 \times 10^{-4} E_{\rm ox}^{1/2} - 4. \times 10^{-5}\ E_{\rm ox}^{1/3} + \frac{qQ_{\rm ox}}{C_{\rm ox}}. \qquad (5)$$

The quantity 3.2 V is the Si/SiO_2 interface barrier height. The second term in (5) represents the barrier lowering effect due to the image field. The third term in (5) accounts phenomenologically for the finite probability of tunneling between the silicon and the silicon dioxide. The spatial distributions of both stress-induced $N_{\rm it}(x)$ and $Q_{\rm ox}(x)$ for gate current simulation can be determined by the modified gated-diode current measurement technique [7].

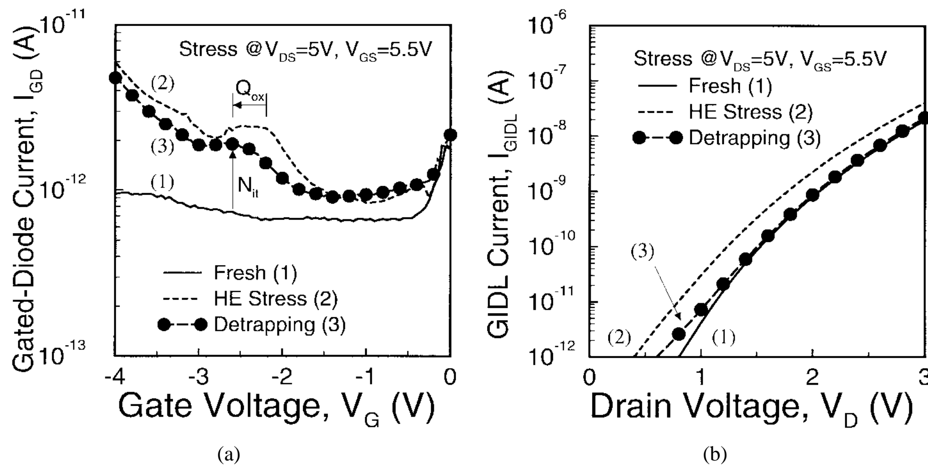

Fig. 4. (a) Measured $I_{\rm GD}$ for devices at fresh (curve 1), after hot electron stress (curve 2), and after detrapped/neutralized (curve 3) conditions. (b) M easured gate-induced-drain-leakage currents $(I_{\rm GIDL})$ for devices at fresh (curve 1), after hot electron stress (curve 2), and after detrapped/neutralized (curve 3) conditions.

V. Results and Discussion

A. Characterization of $N_{\rm it}$ and $Q_{\rm ox}$

Fig. 4(a) and (b) show the measured gated-diode currents $(I_{\rm GD})$ and gate-induced-drain-leakage currents $(I_{\rm GIDL})$ for fresh, hot-electron stressed, and detrapped/neutralized devices. Here, $I_{\rm GD}$ currents will be used to calculate $N_{\rm it}$ and $Q_{\rm ox}$, while $I_{\rm GIDL}$ currents will be used as a monitor for the generation and elimination of $Q_{\rm ox}$ after the hot-electron stress and after the detrapping/neutralization step. The hot-electron stress, $I_{G,\max}$ stress, is performed at the bias condition of $V_{\rm GS} = 5.5$ V and $V_{\rm DS} = 5$ V for 1000 s. Under this bias condition, both $N_{\rm it}$ and negative $Q_{\rm ox}$ will be generated. The detrapping/neutralization step for eliminating $Q_{\rm ox}$ is performed at $V_D = 3$ V and $V_G = -4.5$ V for 50 sec. After this detrapping process, the $I_{\rm GIDL}$ of a stressed device is moved from dashed curve to the right (in solid circles) until the current matches with that of fresh devices at high V_D (e.g., $V_D > 1.2$ V). This means that the stress generated $Q_{\rm ox}$ is totally detrapped/neutralized. Therefore, the difference of $I_{\rm GD}-V_G$ curves between the fresh (curve 1) and detrapped (curve 3) devices is caused by $N_{\rm it}$ alone and can be used to determine $N_{\rm it}$ by (1). Furthermore, the differences of $I_{\rm GD} - V_G$ curves between the detrapped curve (curve 3) and hot-electron stressed curve (curve 2) can be used to calculate $Q_{\rm ox}$ by (2). Fig. 5 shows the extracted $N_{\rm it}$ and $Q_{\rm ox}$ for different stress times. We see that $N_{\rm it}$ and $Q_{\rm ox}$ are both localized in the gate–drain overlap region. In addition, the maximum value of stress-induced $Q_{\rm ox}$ is about four times greater than that of stress-induced $N_{\rm it}$ at the maximum gate current stress bias.

B. Simulation of Gate Current and the Comparison with Experiment

By incorporating the extracted lateral distributions of both $N_{\rm it}$ and $Q_{\rm ox}$ as given in Fig. 5 into a 2-D simulator—ATLAS2 [13], both the device characteristics before and after the stress can be simulated. Fig. 6 shows the simulated lateral electric field distributions at the $\rm Si/SiO_2$ interface for fresh and after

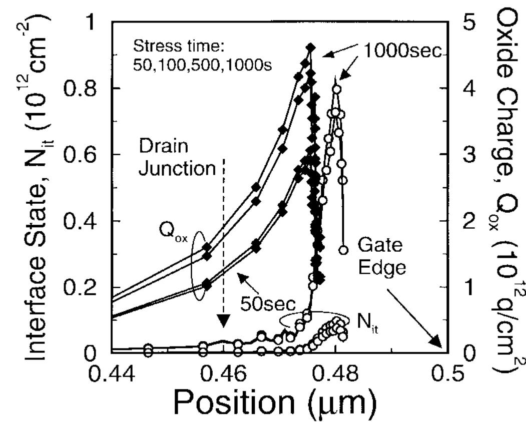

Fig. 5. Extracted spatial distributions of interface states $(N_{\rm it})$ and oxide trapped charges $(Q_{\rm ox})$ after the $I_{G,\max}$ stress for different stress time.

1000-s stressed devices at $V_{\rm GS} = 5.5$ V and $V_{\rm DS} = 5$ V. From a comparison of the extracted $N_{\rm it}$ and $Q_{\rm ox}$ shown in Fig. 5, we see that the peak values of maximum $N_{\rm it}$ and $Q_{\rm ox}$ are about several hundred angstrom away from that of maximum lateral electric field. Furthermore, it was also found that the lateral electric field of stressed device is slightly greater than that of a fresh one since the channel resistance increases due to the localized $N_{\rm it}$ and $Q_{\rm ox}$ buildup during the stress. From Fig. 6, the enhancement of electric field after the hot-electron stress can properly explain the increase of substrate current (shown in Fig. 2) since the impact-ionization rate also increases. However, the gate current degradation still can not be explained from the gate current model in [3]and [10]. From the decrease of gate current with stress time as observed in Fig. 2, an additional degradation factor due to oxide damage exists. Therefore, we suggest that the interface states filled with electrons can be served as a new scattering center to the injected hot electron which reduces the hot-electron injection probability.

Fig. 7 is used to support the above argument. In this figure, the measured and simulated gate current characteristics are shown for devices at fresh, after hot-electron stressed, and

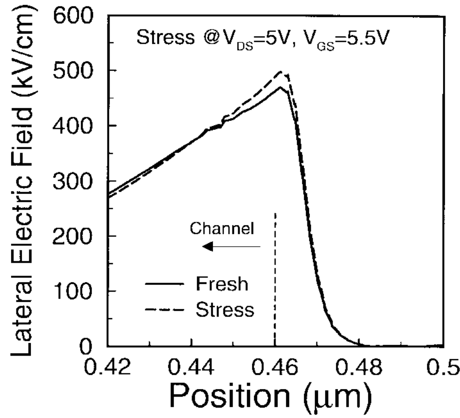

Fig. 6. Simulated lateral electric field distributions of devices before and after $I_{G,\max}$ stress.

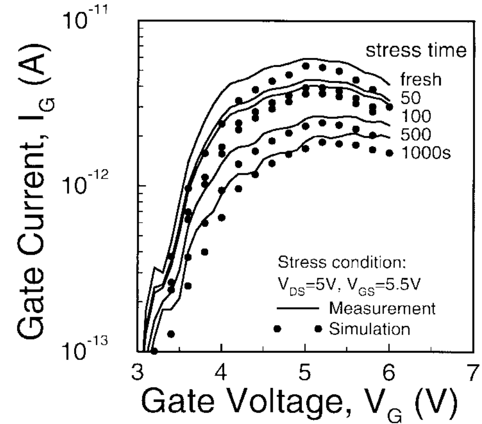

Fig. 8. Measured and simulated gate current characteristics after the $I_{G,\max}$ stress for different stress time.

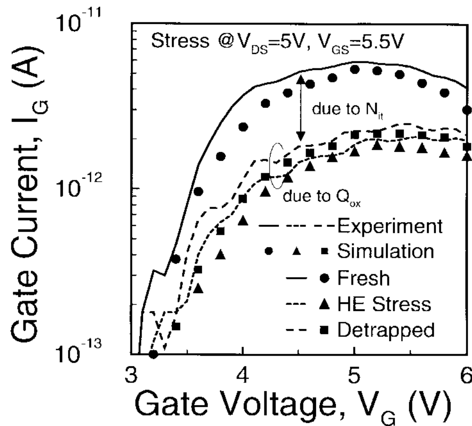

Fig. 7. Measured and simulated gate current characteristics for devices at fresh, after hot electron stress, and after detrapped conditions. Note that $N_{\rm it}$ is dominant for the I_G degradations.

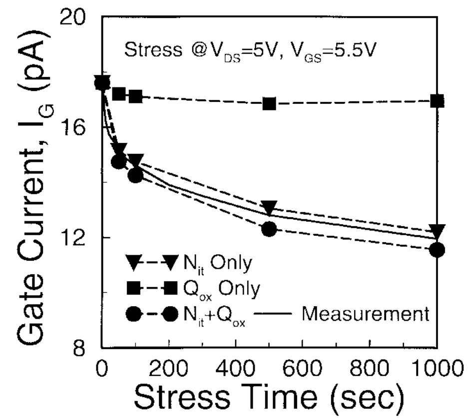

Fig. 9. Simulated gate current variation by considering $N_{\rm it}$ and/or $Q_{\rm ox}$, and their comparison with the measurement data. Note that $N_{\rm it}$ dominates the degradation of gate current.

after detrapped conditions at $V_{\rm DS} = 5$ V, respectively. The detrapping step is used to eliminate $Q_{\rm ox}$. The GIDL current is given as a monitor for the oxide charge detrapping, as shown in Fig. 4(b). From the simulation data, we see that the difference of I_G between the HE stressed (solid triangles) and the detrapped (solid rectangles) conditions is due to the $Q_{\rm ox}$ effect. Also, the difference between the fresh (solid circles) and the detrapped (solid rectangles) curves is due to the $N_{\rm it}$ effect. Obviously, the I_G degradation due to $N_{\rm it}$ is much larger than that due to $Q_{\rm ox}$. This can also explain why the gate current degradation after $I_{B,\max}$ stress is much more serious than that after $I_{G,\max}$ stress. From measurement data, we also observed that the I_G degradation rate $(\Delta I_G/I_G)$ first increases gradually with the increasing gate voltage and then decreases. The reasons are as follows. The scattering of injected hot electron due to $N_{\rm it}$ is dependent on the amount of electrons filled in the interface states. As the gate voltage increases, the amount of electrons filled in these states also increase. As a result, we see that $\Delta I_G/I_G$ increases as the gate voltage increases initially. However, by further increasing the applied gate voltages, the charge screening effect occurs and $\Delta I_G/I_G$ becomes moderate. From the simulated data shown in Fig. 7, the degradation of I_G has been successfully simulated by using the the new model described in (4). The parameter, $\alpha_{\rm nit}$, value with 1.16×10^{-12} cm^{-2} is used. Furthermore, Fig. 8 shows the measured and simulated gate current characteristics among different stress times. Reasonable agreement of the gate currents between simulated and the measured results has been achieved.

Fig. 9 shows the simulated gate current differences at $V_{\rm DS} = 4$ V and $V_{\rm GS} = 4.6$ V by considering $N_{\rm it}$ and/or $Q_{\rm ox}$, and their comparison with the measurement data for different stress time. The stress condition is also at $V_{\rm GS} = 5.5$ V and $V_{\rm DS} = 5$ V. It was found that the degradation of gate currents due to $Q_{\rm ox}$ will saturate after a long stress time. Furthermore, it was also seen that degradation of I_G is mainly due to the generated $N_{\rm it}$. Finally, as the device is continued to scale, we believe that the effects of $N_{\rm it}$ will become more crucial to the gate current rather than $Q_{\rm ox}$.

VI. Conclusion

In summary, we have successfully developed a new gate current model which takes the hot-electron stress generated interface states and oxide trapped charges into account. In this model, we suggest that the interface states will serve as a new scattering center to the injected hot electron and then reduce

the hot-electron injection probability. The generated oxide charges are also introduced as an additional factor affecting the injection potential barrier at the Si–SiO_2 interface. However, the oxide charges are normally located inside the gate oxide such that they have only minor effect to the barrier height. As a result, the influence of $Q_{\rm ox}$ on the gate current degradation is smaller than that of $N_{\rm it}$. In other words, the interface state generation will dominate the gate current degradation not only at the maximum substrate current stress condition but also at the maximum gate current stress condition. Results of the simulated gate currents show a good agreement with the measurement data for pre-stressed and post-stressed devices. Finally, the developed new gate current degradation model is especially useful for the investigation of hot carrier reliabilities in EPROM and Flash EEPROM devices, in which the maximum gate current bias is the programming bias and is crucial for these devices. In other words, the proposed gate current degradation model is most useful for studying nonvolatile memory reliabilities.

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