The Effect of Native Oxide on Thin Gate Oxide Integrity

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***Abstract*—We have studied the effect of native oxide on thin gate oxide integrity. Much improved leakage current of gate oxide can be obtained by *in situ* desorbing the native oxide using a HF-vapor treated and H_2 backed process. Furthermore, extremely sharp interface between oxide and Si is obtained, and good oxide reliability is achieved even under a high current density stress of 11 A/cm^2 and a large charge injection of 7.9×10^4 C/cm^2. The presence of native oxide will increase the interface roughness, gate oxide leakage current and stress-induced hole trap.**

I. Introduction

SCALING down the thickness of gate oxide has been studied extensively because of the improved CMOS device performance [1]–[7]. The key issues for these thin oxides are thickness uniformity and interface smoothness; unfortunately, native oxide roughens the initial surfaces. Furthermore, the reliability of oxide is also strongly degraded by the presence of native oxide [8]. Recently, we have demonstrated the *in situ* desorption of native oxide at 950 to 1000 °C, and achieved atomically smooth oxide interface [9]. In this letter, we have studied the effect of native oxide on thin gate oxide integrity. We have used HF-vapor passivation [10] to reduce the formation of native oxide and lower down the thermal budget. In combination of H_2 bake, HF-vapor treatment can result in improved oxide integrity at a growth temperature of 850 °C for the 27 Å oxide.

II. Experimental

After a modified RCA cleaning, a HF dipping, rinsing in DI water and spun dry, the 4-in [100] wafer was treated by a HF-vapor and immediately loading into the low-pressure furnace. Native oxide was desorbed in this leak-tight low-pressure furnace at 900 °C under a high flow rate of hydrogen, and lowered down to 850 °C for initiating the growth [11]. More detailed process can be found elsewhere [9], [12]. For comparison, control samples were fabricated with the same recipe except without receiving the HF-vapor treatment and *in situ* H_2 bake at 900 °C. AFM, TEM, capacitor I–V, and constant current stress are measured to study the gate oxide integrity.

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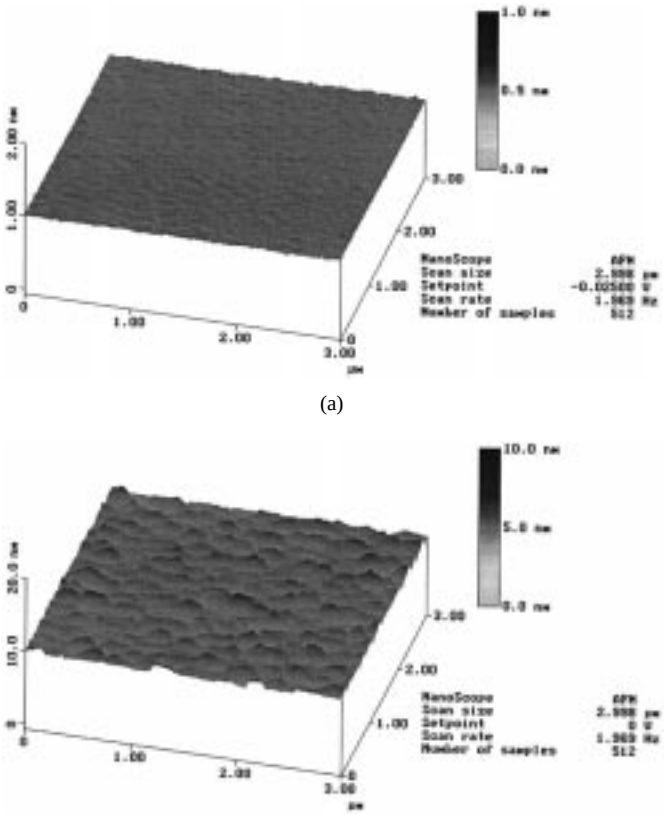


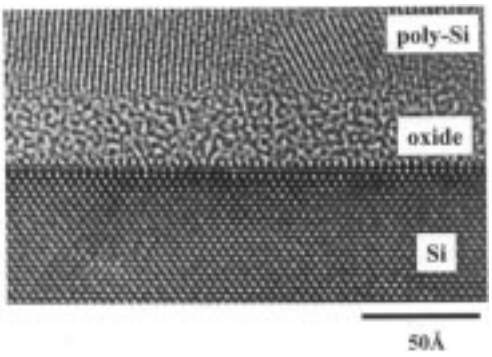
(a)

(b)

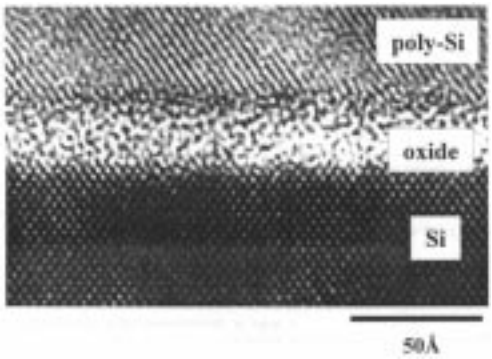
Fig. 1. AFM images of (a) with and (b) without the HF-vapor treatment and H_2 bake, and the rms values are 0.1 Å and 2.9 Å, respectively.

III. Results and Discussion

Fig. 1(a) and (b) show the AFM images of the 27 Å oxides with and without the HF-vapor treatment and *in situ* H_2 bake, respectively. Using this process, the surface rms roughness is much improved from 2.9 Å toward 0.1 Å on a broad 3 μm $\times$ 3 μm area. We have further characterized this very smooth oxide by TEM. Fig. 2(a) and (b) show the atomic lattice image of the 27 Å oxide with and without the HF-vapor treatment and *in situ* H_2 bake, respectively. Very smooth interface between oxide and Si can be observed in Fig. 2(a). Because it is extremely difficult to achieve such smooth surface by wet cleaning, surface atoms migration, after native oxide desorption, may be the explanation for this work and our previous study at higher H_2 baked temperatures [9].



(a)



(b)

Fig. 2. Cross-sectional TEM lattice images of (a) with and (b) without the HF-vapor treatment and H_2 bake.

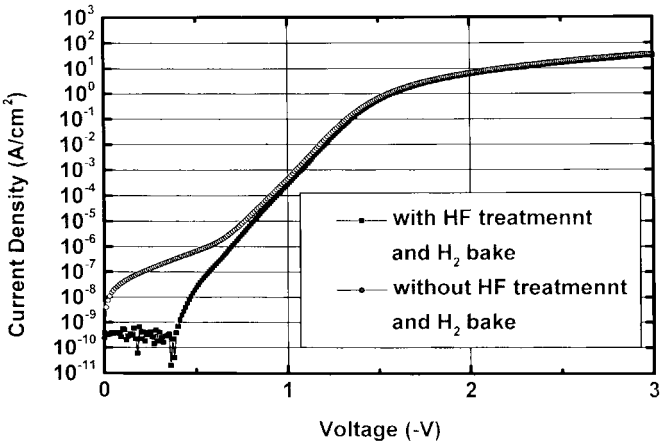


Fig. 3. J-V characteristics of the 27 Å oxide (a) with and (b) without the HF-vapor treatment and H_2 bake. The measured area is 500 μm by 500 μm.

We have also studied the dependence of leakage current on residual native oxide. Fig. 3 presents the measured J–V characteristics of MOS diodes with a 27 Å oxide. An increased gate leakage current at low voltages (<0.5 V) is observed for the control sample without the HF-vapor treatment and *in situ* H_2 bake, even considering the typical 1 Å thickness difference among these oxides. This phenomena is very similar to the stress-induced leakage current (SILC) [13], where the increased leakage current is attributed to trap generation or local thinning in oxide [14]. In fact, Liu *et al.* has also observed such excess leakage and attributed this effect as intrinsic traps

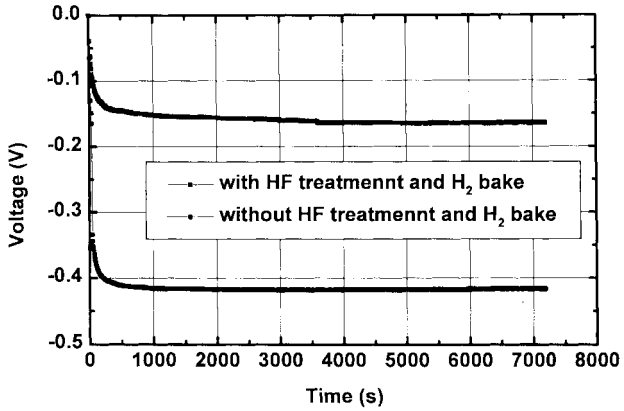


Fig. 4. Capacitor voltage change of the 27 Å oxide (a) with and (b) without the HF-vapor treatment and H_2 bake.

[15]. However, our data suggests that such intrinsic traps are process-dependent and strongly related to the presence of native oxide.

We have further studied the oxide stress effect on the presence of residual native oxide. Fig. 4 shows the measured voltage change of MOS capacitors as a function of time, under a constant stress of 11 A/cm^2. The voltage change is plotted because it is much clearer to show the stress effect. Very high current density is applied, because almost no variation can be measured at lower values. As shown in Fig. 4, no breakdown can be observed for both oxides even under a large charge injection of 7.9×10^4 C/cm^2. The good reliability is consistent with the previous report by reducing native oxide formation under an ultra-dry environment [8]. However, the voltage change is higher in control sample without HF-vapor treatment and *in situ* H_2 bake. This increased concentration of generated hole trap is consistent with the oxide leakage current and interface roughness. Therefore, the presence of residual native oxide not only creates intrinsic traps but also increases the generation rate of hole trap after stress.

IV. Conclusion

In conclusion, much improved oxide interface roughness, leakage current and stress-induced trap can be obtained by using HF-vapor treated and H_2 baked process.

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