# An Extraction Method to Determine Interconnect Parasitic Parameters

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***Abstract*—Interconnect parasitic parameters in integrated circuits have significant impact on circuit speed. An accurate monitoring of these parameters can help to improve interconnect performance during process development, provide information for circuit design, or give useful reference for circuit failure analysis. Existing extraction methods either are destructive (such as SEM measurement) or can determine only partial parasitic parameters (such as large capacitor measurement). In this paper, we present a new method for extracting interconnect parasitic parameters, which can simultaneously determine the interlayer and intralayer capacitances, line resistance, and effective line width. The method is based on two test patterns of a same structure with different dimensions. The structure consumes less wafer area than existing methods. The method shows good agreement with SEM measurement of dielectric thickness in both nonglobal planarized and chemical–mechanical polished processes, and gives accurate prediction of the process spread of a ring oscillator speed over a wafer.**

## I. Introduction

IN DEEP-SUBMICRON integrated circuits, multilevel interconnection greatly affects circuit performance [1]–[8], [11], [13]. If the interconnect parasitic parameters can be monitored or extracted during process control monitor (PCM) test right after wafer is fabricated, then these monitored parameters can allow for accurate estimation of interconnect performance [1]–[5], [14] or for backend process improvement, or can provide as a basis for circuit simulation or for circuit failure analysis. Note that here in the case of circuit failure, the failure can be traced back to possibly ill interconnect performance on the same die via the extracted parameter information. This is in analogy to the traditional approach of tracing circuit failure back to ill device performance. Interconnection, as it becomes multilevels and more complex, can have a comparable impact on circuit speed as the device.

Major interconnect parameters include wire capacitance and resistance [3]–[5], [13], [14]. Wire capacitance, whether intralayer or interlayer, is determined by dielectric thickness and wire dimension, and wire resistance is determined by wire dimension and wire resistivity. However, as dielectric thickness variation is significant in both chemical–mechanical-polished (CMP) process and nonglobal planarized (SOG-based) process, interconnect effect can vary greatly. The CMP

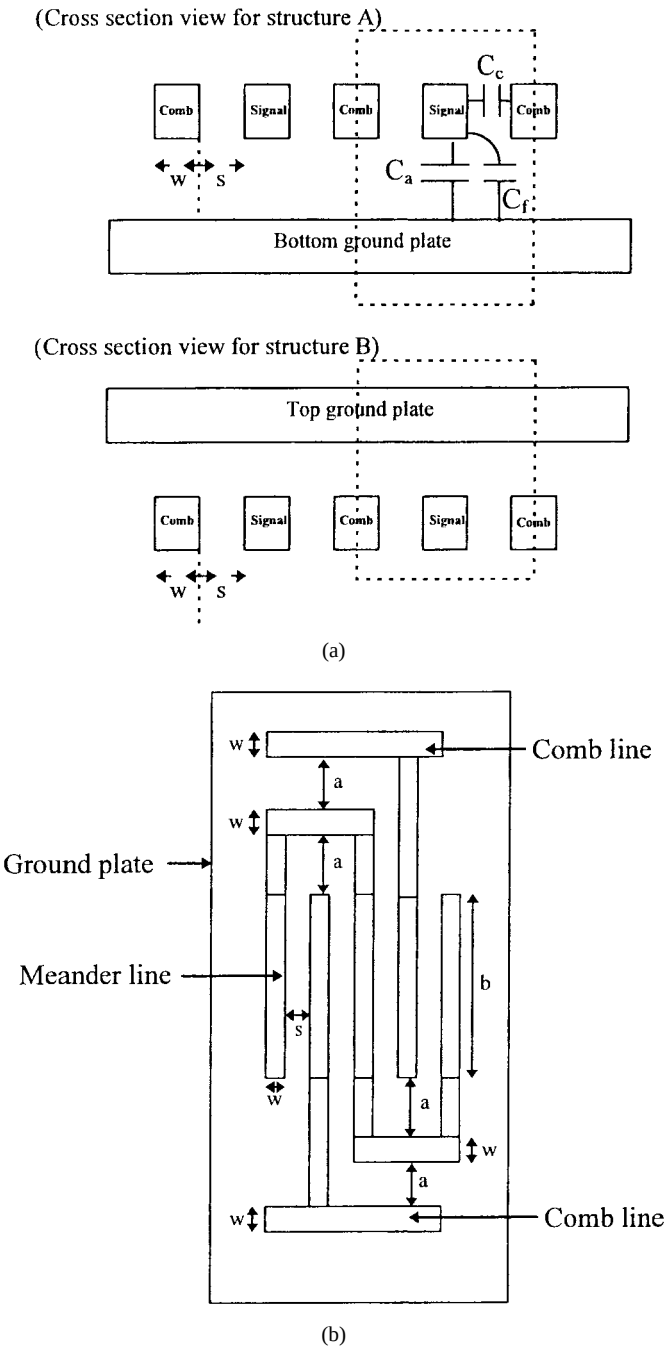


Fig. 1. Top view and cross section of interconnect parasitic test structure.

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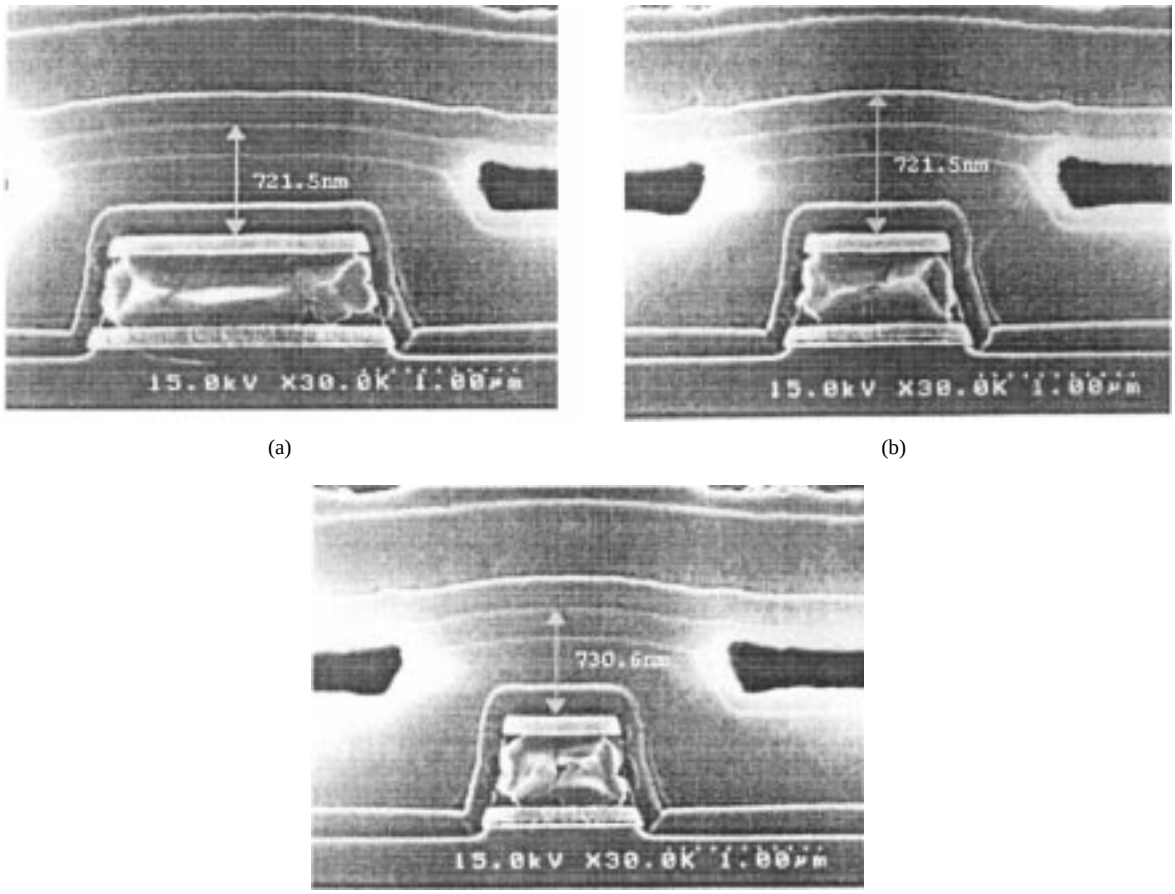



Fig. 2. Dielectric thickness variation versus metal wire width: (a) $W = 1.5$ $\mu$m, (b) $W = 0.8$ $\mu$m, and (c) $W = 0.6$ $\mu$m.

method improves local dielectric planarity, thus lithography uniformity, but gives considerable intrawafer variation [2]. The SOG-based process exhibits much better intrawafer uniformity than CMP, but shows considerable local thickness variation with strong pattern sensitivity of the underlying layer [3], [6], [7]. Wire dimension variation is also significant due to limited photolithography and etching controllability, causing great fluctuations of wire fringe capacitance and resistance. Hence, a close monitoring of these interconnect parameter variations is essential to an accurate estimation of interconnect performance.

In conventional methods, dielectric thickness was monitored using optical method [8], off-line scanning electron microscope (SEM) [2], [3], or large capacitor measurement, whereas wire dimensions were measured using on-line SEM or resistance measurement based on several resistors of different widths or the Van-der-Pauws structure. The optical and SEM measurements are manually executed and require huge test patterns, and the off-line SEM measurement is destructive. The large capacitor measurement and resistive measurement allow for nondestructive test, but they do not provide information of intralayer capacitance, and the combination of them takes large wafer area. These conventional methods are not suitable or adequate for PCM test. In [9], Hu developed a dc method for measuring only metal capacitance based on inverter power supply current. Laguai *et al.* [10] gave a voltage method for also measuring small metal capacitance. For process optimization and circuit failure analysis, one needs a method which has an efficient test structure and which can yield all the required parasitic parameters.

In this paper, we develop a new extraction method to simultaneously determine interlayer and intralayer capacitances, line resistance and effective line width. The method is based on only two test patterns per pair of metal layers, with the two patterns being of identical structure but different dimensions. Results of our method show good agreement with the SEM measurement of dielectric thickness, the numerical simulation [12] of resistance–capacitance correlation, as well as a measured ring oscillator speed with wiring loading across a wafer. The method also has the advantage of consuming much less silicon area than existing methods [3], [10], [14], and is particularly useful in capturing the severe intrawafer dielectric thickness variation in CMP process and the underlying-wire-pitch dependent dielectric thickness in a nonglobal planarized process.

The paper is organized as follows. In Section II, the test structure and extraction methodology are given. In Section III, the results of the new method are verified, along with some discussion. The paper is concluded in Section IV.

## II. Test Structure and Extraction Methodology

Our main goal of extraction is the following: a set of dimensional or electrical parameters can be calculated based

on measured data, and combinations of these parameters can provide accurate indication of interconnect performance. The set of parameters of interest are defined to be interlayer dielectric thickness, wire width reduction from the drawn width (which is equal to the interwire spacing increase with fixed wire pitch), intralayer line-to-line coupling capacitance and wire sheet resistance; they are denoted in order as $t_{ox}$ (or alternately, $C_a$, the capacitance per unit area), $\delta W$, $C_c$, and $R_{sh}$, respectively. The capacitance components $C_c$ and $C_a$ are shown in the interconnect cross-section view of Fig. 1(a). There also exists a fringe capacitance component $C_f$ which is the corner fringe flux from wire to ground; this component will be canceled in our extraction method, as it only weakly depends on the underlying oxide thickness and does not provide oxide thickness information. Note that here the effective width $W_{\text{eff}}$ is given by

$$W_{\text{eff}} = W_{drawn} - \delta W \tag{1}$$

with $W_{drawn}$ denoting the drawn width. From the delay model derived by Sakurai [11], the set of parameters can give analytical wire delay estimation. The test structure for extracting these parameters is defined and shown in Fig. 1, with Fig. 1(a) giving the cross-section view and Fig. 1(b) the top view. The structure is based on a long meander line with several turns of a total length $L$ [Fig. 1(b) only shows two turns for simplicity of presentation], which is accompanied by two adjacent comb lines placed very close to the meander line. The structure is laid out with two line widths, $W = W_1$ and $W = W_2$, and with equal interline spacing $S$, corner-to-comb distance $a$ and meander-to-comb overlapping length $b$. To take care of pattern sensitivity of nonglobal planarized process, this structure is further expanded into two structures, structures A and B, as shown in Fig. 1(a). Technology with global planarization (such as CMP) uses structure A only, and technology with only local planarization (such as SOG) uses both structures A and B.

The interconnect parameters are measured and extracted via the following algorithm. For structure A, we measure the unit-length meander line to ground-plane capacitance $C_{W_1}$ and $C_{W_2}$ of width $W_1$ and $W_2$, respectively, the resistance of meander $R_{W_1}$ and $R_{W_2}$, and the coupling capacitance $C_c$ between meander line and neighboring comb lines, all in unit of Farads per unit meander line length. In measuring the meander to ground-plane capacitance, neighboring comb lines are connected to system ground, so that the current signal through $C_c$ is not detected by the sensing node of capacitance–voltage ($C$–$V$) meter (HP4284). As a result, $C_c$ is not included into $C_{W_1}$ and $C_{W_2}$. Note that similarly, the bottom plane is connected to ground when measuring $C_c$. In addition to the direct measured $C_c$, metal line parameters are calculated as

$$C_a = \frac{\varepsilon}{t_{ox}} = \frac{C_{W_1} - C_{W_2}}{W_1 - W_2} \tag{2}$$

$$\delta W = W_1 - \frac{(W_1 - W_2)R_{W_2}}{(R_{W_2} - R_{W_1})} \tag{3}$$

$$R_{sh} = \frac{R_{W_1}(W_1 - \delta W)}{L} \tag{4}$$

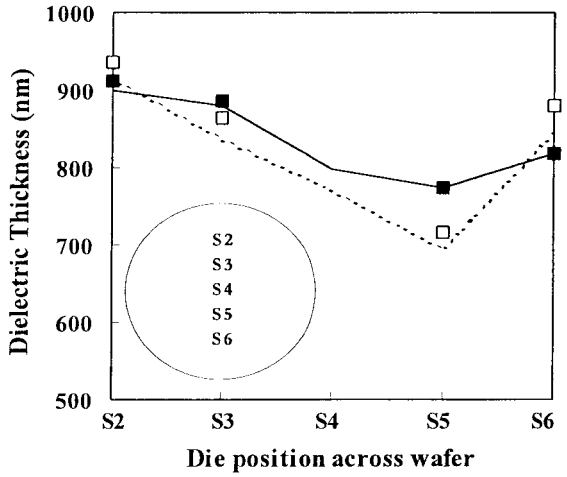



Fig. 3. Verification of measured dielectric thickness with SEM measurement. Filled square and solid line: IMD thickness from SEM and the new method. Empty square and dashed line: ILD thickness from SEM and the new method.

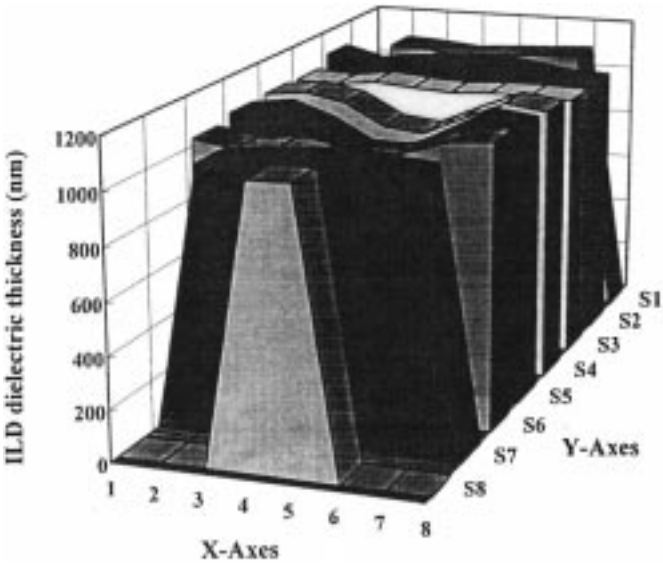



Fig. 4. Wafer map of ILD thickness obtained from our method.

where $\epsilon$ is the dielectric constant of interlayer dielectric and $L$ is the total length of the meander line. Note that in (2), the fringe component $C_f$ exists in the capacitances $C_{W_1}$ and $C_{W_2}$ with equal amount, and is thus canceled. In our analysis, we further combine the effects of $\delta W$ and $R_{sh}$ into a single resistance parameter $R$, with $R$ defined by

$$R = \frac{R_{W_1} W_1}{L}. \tag{5}$$

In both global planarized and nonglobal planarized technology, the dielectric thickness may vary with wire density of the underlying layer [3], [16]. The additional structure B in Fig. 1(a) is designed for this purpose, where the line width $W_1$ and spacing $S$ can be arbitrarily selected to investigate their influence on $t_{ox}$. However, the line width $W_2$ must be sufficiently close to $W_1$ so that the difference between $t_{ox}(W_1)$ and $t_{ox}(W_2)$ is negligible in the extraction based on (2)–(5). The dielectric thickness variation with wire width, for a layer composed of SOG and TEOS between metal-1 and metal-2, is

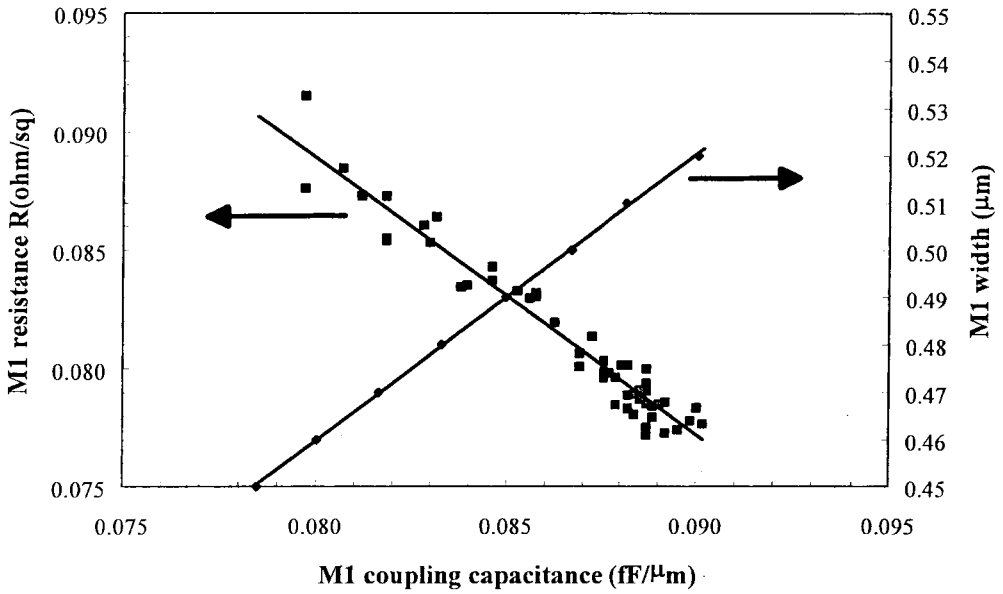



Fig. 5. Verification of resistance–capacitance-width with Raphael simulation. Symbol: data from the new method. Lines: Raphael simulation.

shown in Fig. 2(a)–(c). Here, the interwire spacings are 10 $\mu$m for all wire widths so that wire width dependence of $t_{ox}$ can be easily observed. It is clearly shown that $t_{ox}$ only varies from 7215 to 7306 Å, for a width variation from $W = 1.5$ $\mu$m to $W = 0.6$ $\mu$m, demonstrating that constant $t_{ox}$ can be obtained within reasonable width variation. Based on the criterion that $W_1$ and $W_2$ are reasonably close, (2)–(5) can be used to calculate the dependence of the dielectric thickness on $W$ and $S$.

## III. Results and Discussion

For verification, our method is applied on two processes: a 0.35-$\mu$m twin-well CMOS technology with single level poly and quadruple-level metals, and a 0.5-$\mu$m CMOS technology with triple-level metals. In the 0.35-$\mu$m process, one-pad CMP is used in all-layer dielectric planarization [2]. The fabrication sequence is as follows: after silicide formation on gate and diffusion, a layer of TEOS is deposited forming the interlayer dielectric, which is CMP planarized down to the target dielectric thickness. After contact opening and tungsten plug, a metal-1 layer formed with AlCu (1%Cu) and TiN barrier is deposited and patterned. Similarly, CMP, tungsten plug and metallization technique are used in all subsequent metal and dielectric layers. The 0.5-$\mu$m technology is with partial-etching-back SOG (denoted as SOG) as interlayer dielectric, without any CMP. Capacitance data is measured using a HP4284 at 100 KHz, with a signal level of 50 mV and zero dc bias. The measured capacitance data is in the range of 1–10 pF. Pad and system parasitic effect is excluded beforehand using dummy open pad calibration.

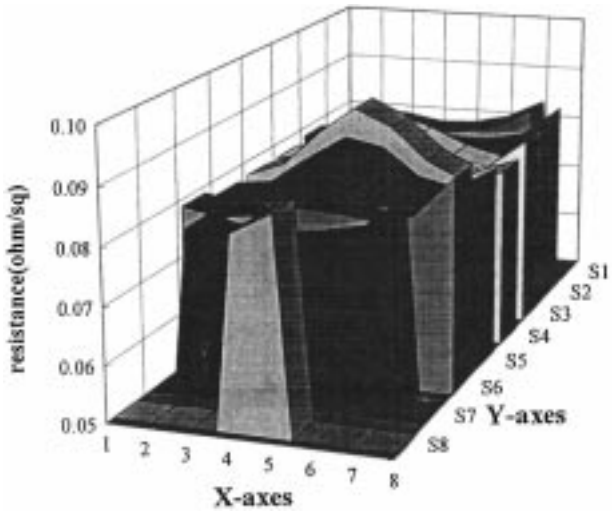
### A. Capacitance and Resistance Analysis

The extracted $t_{ox}$ of interlayer oxide (ILD, between metal-1 and active area) and intermetal oxide (IMD, between metal-1 and metal-2) across the wafer is first given and compared with the SEM measurement on the same wafer, as shown in Fig. 3. Here, in order to obtain the SEM data on the same die for capacitance measurement, dies S2, S3, S5, and S6 are cut for off-line SEM after their capacitance are measured. The values of extracted $t_{ox}$ show good agreement with the SEM measurement for both ILD and IMD layers, and the high $t_{ox}$ value near position S2 (on top of wafer) as well as the low $t_{ox}$ on S5 are both captured by our method. The wafer map of ILD thickness obtained from our method is shown in Fig. 4, which clearly describes the ILD thickness lowering along the center part of the wafer. This variation is accurately captured using our new method.

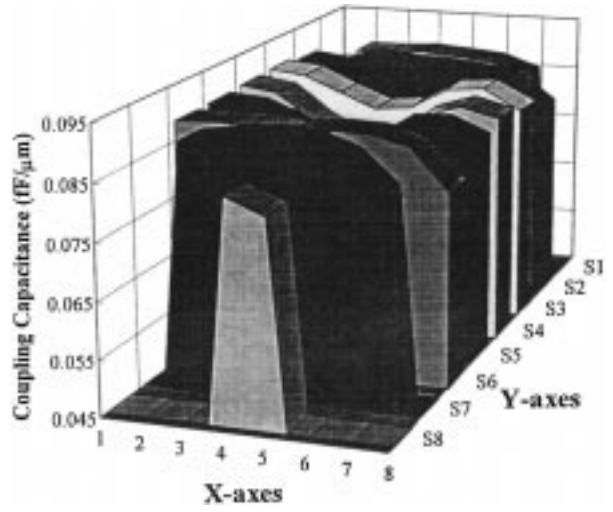
In deep submicron technology, wire width, which usually varies due to lithography fluctuations, dominates coupling capacitance and line resistance [11]. Monitoring of the effect of line width variation on wire resistance and capacitance is necessary, and a limited percentage of line width variation in manufacturing technology, e.g., $|\delta W/W_{\text{eff}}| \leq 10\%$, is often required. Within such a range, the associated capacitance and resistance variations can be modeled as a linear function of the wire width variation. As a result, the intralayer coupling capacitance $C_c$ is linearly proportional to line width due to interline space reduction, and this further makes $C_c$ correlate linearly with line resistance $R$; the correlation has a negative slope as $R$ reduces with increased wire width. This linear correlation is successfully predicted based on the data extracted using our method, as shown in Fig. 5. Fig. 5 shows the extracted intralayer coupling capacitance $C_c$, and its correlation with the meander line resistance $R$ as well as with extracted effective metal-1 line width. The correlation is calculated to be

$$R = -1.168C_c + 0.1824. \tag{6}$$

As a further quantitative verification, simulation of resistance and coupling capacitance using Raphael [12] is executed based on extracted line widths from various dies. In our simulation, the measured ILD and IMD thickness based on (2)–(5) are used, with their dielectric constants being 3.9 and 4.1, respectively. The simulated coupling capacitance and wire resistance




(a)



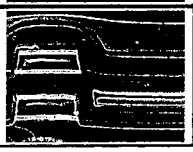

(b)

Fig. 6. Wafer map of Metal 1 measurement: (a) resistance and (b) coupling capacitance.

using Raphael agree well with our extracted data, further demonstrating the quantitative accuracy of our method. The verification of the resistance–capacitance correlation indicates that our method, in addition to accurately capturing oxide thickness, can further capture line width and related effects, which are essential for process control monitor and statistical metrology. The wafer map of $R$ and $C_c$ in Fig. 6(a) and (b) also confirms this statement, as the negative linear correlation is clearly shown on every location on the wafer. The negative linear correlation relationship inherent in (6) can be adapted to apply to manufacturing testing so that $C_c$ can be directly obtained via measured $R$, allowing for efficient parametric test. Impact of ILD thickness is negligible here, as both line width and spacing are relatively small compared to ILD thickness, giving negligible interlayer capacitance compared to the intralayer capacitance $C_c$.

To verify the accuracy of our method in nonglobal-planarized technology, the extracted oxide thickness from the SOG backend process is compared with the SEM measurement

TABLE I
COMPARISON OF THE NEW METHOD AND SEM

| Inter-metal dielectric thickness | | | | |
|---|---|---|---|---|
| Width (μm) | Space (μm) | Cross Section | SEM (Å) | New Method (Å) |
| 0.75 | 0.75 |  | 10400 | 10864 |
| 0.75 | 14.0 |  | 6000 | 5679 |

for both dense and sparse underlying arrays, as shown in Table I. The cross-section pictures are also shown. The obvious dielectric thinning of the sparse array, as shown by the SEM picture, is accurately captured by our extraction method. This comparison demonstrates the applicability of our method in calculating dielectric thickness of nonglobal planarized technology.

### *B. Delay Time Analysis*

Next, the delay time variation across the wafer induced by interconnect parasitic effect is investigated. Ring oscillators with metal wiring loading has been fabricated and measured. The configuration of the ring oscillator is shown in Fig. 7(a), with the layout of loading section being similar to our test structure as shown in Fig. 1. Two types of ring oscillators have been included: one with the adjacent comb lines with $S = 0.45$ $\mu$m (namely ring-1), one without the adjacent comb lines (namely ring-2), both with $L = 1334.3$ $\mu$m, $W = 0.5$ $\mu$m, $a = 5$ $\mu$m, and $b = 300$ $\mu$m. An additional ring oscillator without wiring loading has also been included for the purpose of comparison, with $L = 68.3$ $\mu$m from intrinsic inverter-to-inverter interconnections. All ring oscillators are with device channel length of 0.35-$\mu$m and channel widths of 20 and 8-$\mu$m for PMOS and NMOS, respectively. This effective delay induced by unit wire loading, $t_{dunit}$, is calculated as

$$t_{dunit} = (t_{dload} - t_{dring})/L \tag{7}$$

where $t_{dload}$ denotes the delay time per stage in the ring oscillator with loading, $t_{dring}$ denotes the delay time per ring oscillator stage without wiring loading.

To verify the accuracy of our extraction method, SPICE simulations are executed based on extracted $\delta W$, $C_c$, and $R$ for calculating ring oscillator speed, and the result shows good agreement with measured delay $t_{dunit}$ on the same die, as shown in Table II. In these simulations, HSPICE level-28 model [15] (with all device parameters extracted from the same wafer as our capacitance extraction), is used for simulating the device characteristics in the inverters. Table II gives the comparison of simulated and measured ring oscillator speed for both metal-1 and metal-2 loading.

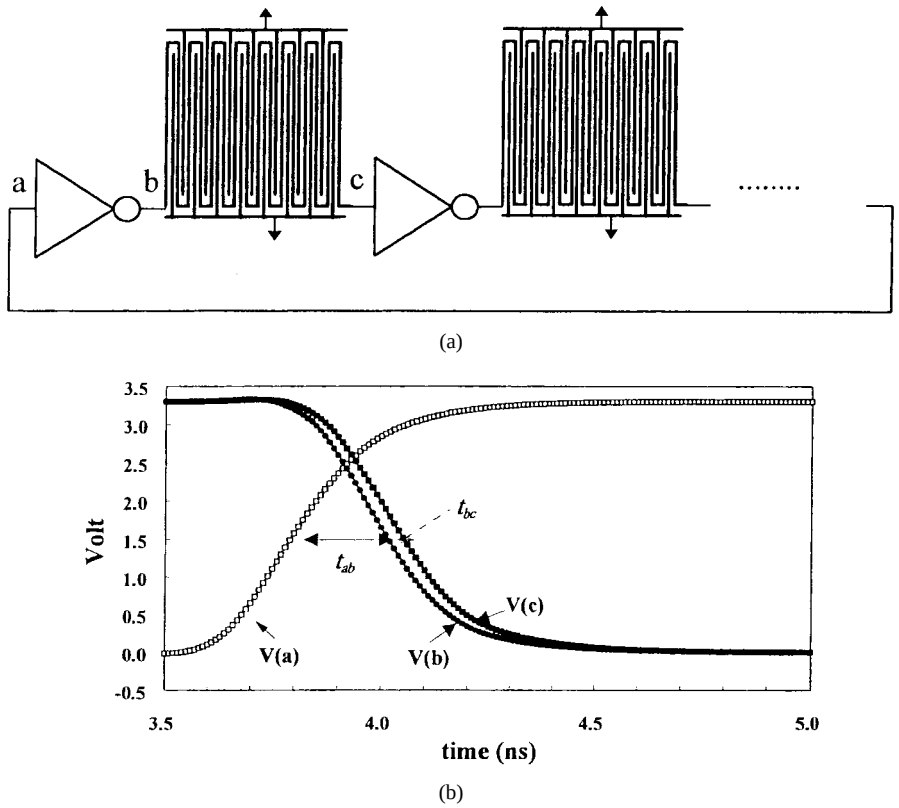



Fig. 7. (a) Ring oscillator with wire loading and (b) transient response.

TABLE II
COMPARISON OF SIMULATION, CALCULATION, AND MEASUREMENT

| Ring oscillator delay with Metal-1 loading | | | |
|---|---|---|---|
| Width (μm) | Space (μm) | Measurement (ps/μm) | Simulation (ps/μm) |
| 0.5 | 0.45 | 0.133 | 0.133 |
| 0.5 | 0.90 | 0.099 | 0.093 |
| **Ring oscillator delay with Metal-2 loading** | | | |
| Width (μm) | Space (μm) | Measurement (ps/μm) | Simulation (ps/μm) |
| 0.6 | 0.50 | 0.120 | 0.119 |
| 0.6 | 1.00 | 0.083 | 0.079 |

The distribution of $t_{dunit}$ across the wafer is now analyzed. Generally, $t_{dunit}$ is dominated by $t_{dload}$, which can be decomposed into two parts: $t_{ab}$ which is the delay from inverter input (point $a$) to inverter output (point $b$), and $t_{bc}$ from inverter output to next inverter input (point $c$) through the metal wire, as depicted in Fig. 7(b). The quantity $t_{ab}$ is determined by device driving ability in the inverter and also the effective loading capacitance at node $b$ which includes the drain junction capacitance of NMOS and PMOS, gate capacitance of next stage, and most importantly, the loading wire capacitance. Note that here, the delay time increase in the ring oscillator with load is induced by the fact that the inverter devices need to drive the additional wire loading which does not exist in the ring oscillator without load. As a result, $t_{ab}$ and hence $t_{dunit}$ have strong dependence on device driving ability, though $t_{dring}$ has been excluded. The effect of gate capacitance of the next stage is not negligible, although its impact may be partially shielded by the loading wire. The quantity $t_{bc}$ is determined by the wire resistance, wire capacitance, and also gate capacitance of the next stage [1], [11], [14] which is identical to the gate capacitance affecting $t_{ab}$. Among $t_{ab}$ and $t_{bc}$, the longer one will dominate $t_{dunit}$, and its associated capacitance components will also dominate $t_{dunit}$. Here, in our ring oscillators, $t_{ab}/t_{dload} = 84.3\%$ for ring-1 (the meander line with adjacent grounded-comb), and $t_{ab}/t_{dload} = 82.9\%$ for ring-2 (the meander line without adjacent grounded-comb). Hence, $t_{dunit}$ is dominated by $t_{ab}$.

Fig. 8 gives the measured wafer map of $t_{dunit}$ in a ring oscillator. For the oscillator ring-1 with $S = 0.45$ $\mu$m, the total capacitance on the loading wire is dominated by the interline coupling capacitance $C_c$. As a result, based on the aforementioned fact that $t_{dunit}$ is dominated by $t_{ab}$, which strongly depends on loading wire capacitance, the $t_{dunit}$ distribution shown in Fig. 8(a) is similar to that of $C_c$ distribution shown in Fig. 6(b). On the contrary, ring-2 has its wire loading capacitance dominated by line to ground capacitance ($C_c$ is zero here), and ring oscillator delay distribution across the wafer shown in Fig. 8(b) is clearly correlated with the $t_{ox}$ distribution shown in Fig. 4. That is, at locations where $t_{ox}$ is small (e.g., in the center of the wafer), line to ground capacitance is high, and $t_{dunit}$ is high.

For quantitatively verifying the accuracy of our method, $t_{dunit}$ is simulated using HSPICE [15] based on extracted $C_a$, $C_c$, $R_{sh}$, and $\delta W$ on each die. The result is shown in Fig. 8(c) and (d) for ring-1 and ring-2, respectively. Good agreement between measured and simulated $t_{dunit}$ distribution

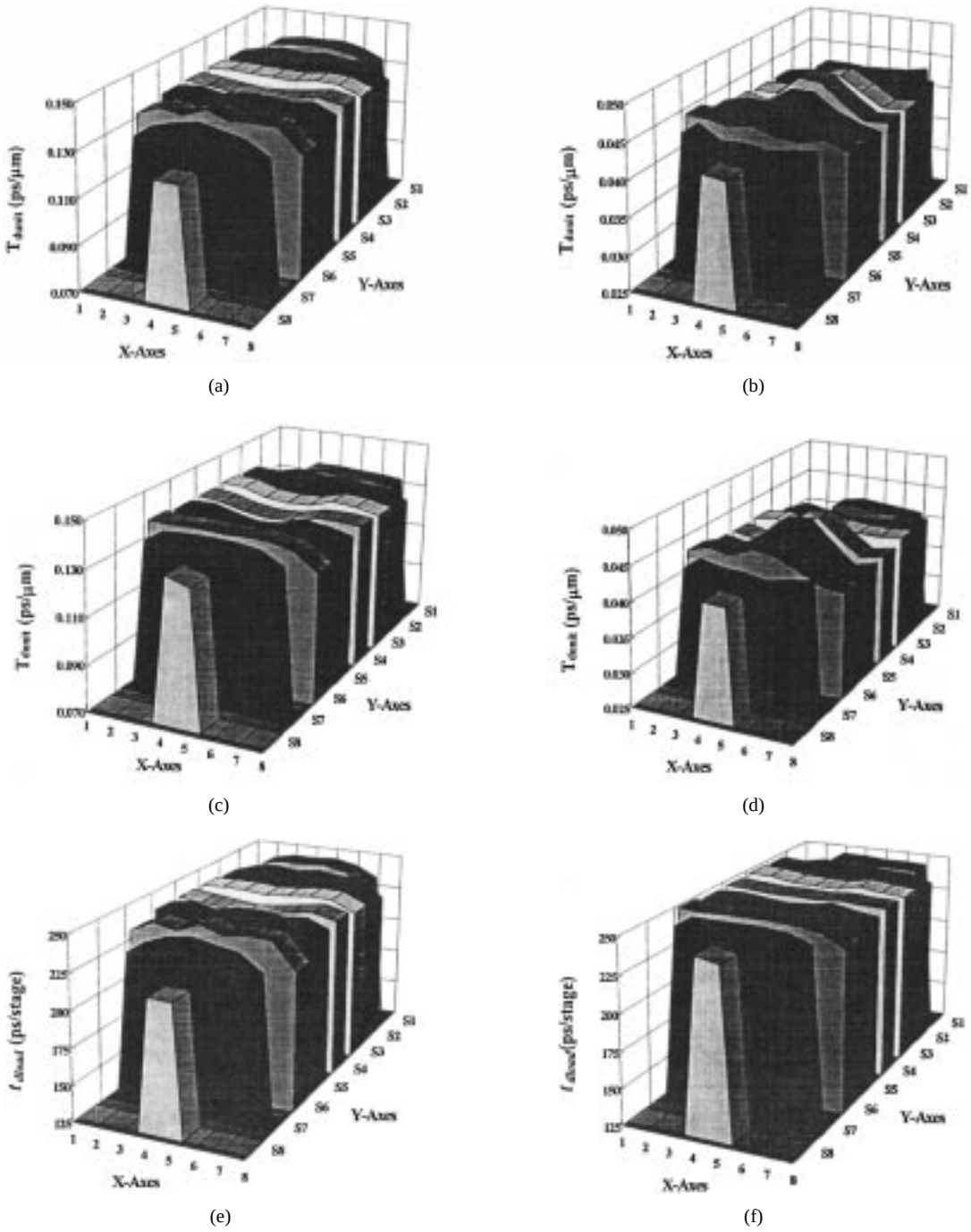



Fig. 8. Comparison of simulated and measured ring oscillator delays with metal loading: (a) measured $t_{dunit}$: ring-1, (b) measured $t_{dunit}$: ring-2, (c) simulated $t_{dunit}$: ring-1, (d) simulated $t_{dunit}$: ring-2, (e) measured ring oscillator delay ($t_{dload}$): ring-1, and (f) calculated ring oscillator delay ($t_{dload}$): ring-1.

across the wafer is shown for both ring-1 and ring-2. The means of simulated $t_{dunit}$ are 0.134 and 0.042 ps/$\mu$m, the means of measured $t_{dunit}$ are 0.133 and 0.0431 ps/$\mu$m, for ring-1 and ring-2, respectively. The root-mean-square errors are 2.23% for ring-1 and 3.25% for ring-2. The agreement between measurement and simulation verifies that our extraction provides valuable interconnect parasitic parameters, as our method accurately predicts process spread of ring oscillator delay caused by interconnect loading.

The calculated interconnect parameters can also be used for analytical estimation of wiring delay [11]. Delay estimation can be obtained based on the equivalent circuit in Fig. 9. Based on this circuit, the delay time of ring oscillator with interconnect loading can be calculated as

$$t_{dload} = 2R_tC_t + 2R_tC_l + 2R_lC_t + 0.8R_lC_l, \qquad (8)$$

where $C_t = C_g + C_d$, $C_{wire} = C_aW_{\text{eff}} + 2C_c + C_f$, $C_l = C_{wire}L$, and $R_l = R_{sh}L/W_{\text{eff}}$. In (8), $R_l$ and $C_l$ denote the total line resistance and line capacitance on the loading wire, respectively; $L$ denotes the total loading wire

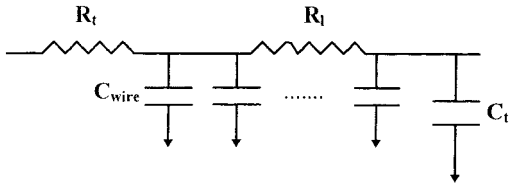



Fig. 9. Equivalent circuit for delay calculation.

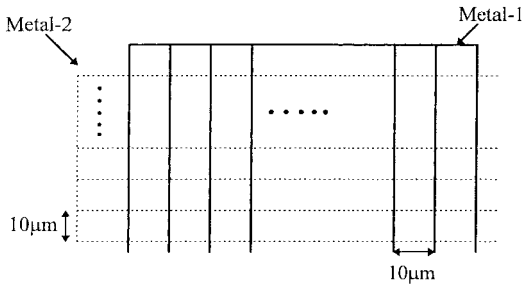



Fig. 10. Cross wiring test structure.

length between any two inverters, which is obtained from test pattern layout; $R_t$ is the input resistance of the previous stage and is modeled by $R_t = V_{ds}/I_{ds}$ in the linear regime with $V_{ds} = 0.1$ V; $C_g$ is the effective gate capacitance including both NMOS and PMOS in the inverter of next stage; $C_d$ is the effective drain capacitance including both NMOS and PMOS of previous stage; $C_t$ is the total loading capacitance seen by the line. Since $C_g$ and $C_d$ vary with drain and gate bias, averaged value calculated by $C_g = \int_{t_1}^{t_2} C_{gate}(t)\,dt$ and $C_d = \int_{t_1}^{t_2} C_{drain}(t)\,dt$ are used, with $t_1$ and $t_2$ denoting the time when $V(a) = 0.5$ $V_{dd}$ and $V(b) = 0.5$ $V_{dd}$, respectively, and $C_{gate}(t)$ and $C_{drain}(t)$ denoting the total gate and drain capacitance at time $t$. Based on (8), delay time caused by wire loading on each die of the wafer is calculated via measured $C_c$, $\delta W$, $t_{ox}$, and $R$. The parameters used in this calculation are: $C_g = 48.23$ fF, $C_d = 5.03$ fF, $R_t = 267.3\,\Omega$, and $L = 1334.3$ $\mu$m. The measured $t_{dload}$ and calculation result of ring-1 are given in Fig. 8(e) and (f), respectively, showing good agreement with a root-mean-square error of 4.44%.

Our extraction method, though based on test elements of parallel lines, can be easily applied to obtain the capacitance of cross wiring structures. A test structure with 33 metal-1 lines and 44 metal-2 lines, with metal-1 lines crossing metal-2 lines as shown in Fig. 10, has been fabricated. The measured metal-2 capacitance, including both metal-2 to metal-1 crossing capacitance and metal-2 to ground capacitance, are then divided by the number of crossings, to give a metal-2 capacitance per crossing. Based on the extracted $t_{ox}$ and $\delta W$, the simulated metal-2 capacitance is 1.04 fF/per crossing, which agrees well with the measured 1.009 fF/per crossing.

## IV. Conclusion

A novel method for extracting interconnect parasitic parameters is developed. This method gives accurate dielectric thickness, line resistance, width reduction and coupling capacitance simultaneously based on only two area-efficient structures. Results of the method agree well with SEM measurement data and give accurate prediction of a ring oscillator speed.

## References

[1] A. K. Goel, *High-Speed VLSI Interconnections: Modeling, Analysis and Simulation.* New York: Wiley, 1994, pp. 51–75.
[2] E. Chang *et al.*, "Using a statistical metrology framework to identify systematic and random sources of die- and wafer-level ILD thickness variation in CMP processes," in *IEDM Tech. Dig.*, 1995, pp. 499–502.
[3] K. J. Chang *et al.*, "Parameterized SPICE subcircuits for multilevel interconnect modeling and simulation," *IEEE Trans. Circuits Syst. II*, vol. 39, pp. 779–789, Nov. 1992.
[4] K. Rahmat, O. S. Nakagawa, S. Y. Oh, and J. Moll, "A scaling scheme for interconnect in deep submicron process," in *IEDM Tech. Dig.*, 1995, pp. 245–248.
[5] M. Bohr, "Interconnect scaling—The real limiter to high performance ULSI," in *IEDM Tech. Dig.*, 1996, pp. 241–244.
[6] J. H. Chern, J. Huang, L. Aldredge, P. Li, and P. Yang, "Multilevel metal capacitance models for CAD design synthesis systems," *IEEE Electron Device Lett.*, vol. 13, pp. 32–34, 1992.
[7] N. D. Arora *et al.*, "Modeling and extraction of interconnect capacitance for multilayer VLSI circuits," *IEEE Trans. Computer-Aided Design*, vol. 15, pp. 58–67, Jan. 1996.
[8] K. Chen, C. Hu, P. Fang, and A. Gupta, "Experimental confirmation of an accurate CMOS gate delay model for gate oxide and voltage scaling," *IEEE Electron Device Lett.*, vol. 18, no. 6, pp. 275–277, 1996.
[9] J. C. Chen, B. McGaughy, D. Sylvester, and C. Hu, "An on-chip, attofarad interconnect charge-based capacitance measurement(CBCM) technique," in *IEDM Tech. Dig.*. 1996, pp. 69–72.
[10] B. Laguai, H. Richter, and B. Hofflinger, "A new method and test structure for easy determination of femto-farad on-chip capacitance in a MOS process," in *Proc. IEEE Int. Conf. Microelectronics Test Structures*, Mar. 1992, vol. 5, pp. 62–66.
[11] T. Sakurai, "Closed-form expressions for interconnection delay, coupling and crosstalk in VLSI's," *IEEE Trans. Electron Devices*, vol. 40, pp. 118–124, Jan. 1993.
[12] *Raphael Users Guide*, Technology Modeling Associate Inc., 1996, San Jose, CA.
[13] T. C. Lee and J. Cong, "The new line in IC design," *IEEE Spectrum*, pp. 52–58, 1997.
[14] D. H. Cho, Y. S. Eo, M. H. Seung, N. H. Kim, O. K. Kwon, and H. S. Park, "Interconnect capacitance, crosstalk, and signal delay for 0.35$\mu$m CMOS technology," in *IEDM Tech. Dig.*, 1996, pp. 619–622.
[15] HSPICE Users' Manual, Meta Software, 1996.
[16] B. E. Stine, D. O. Ouma, R. R. Divecha, D. S. Boning, J. E. Chung, D. L. Hetherington, C. R. Harwood, O. S. Nakagawa, and S.-Y. Oh, "Rapid characterization and modeling of pattern-dependent variation in chemical-mechanical polishing," *IEEE Trans. Semiconduct. Manufact.*, vol. 11, pp. 129–140, Feb. 1998.

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