Application of Plasma Immersion Ion Implantation Doping to Low-Temperature Processed Poly-Si TFT's

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***Abstract*— This work applied, for the first time, plasma immersion ion implantation (PIII) for source/drain doping on low-temperature processed polysilicon thin-film transistors (poly-Si TFT's). Experimental results indicate that PIII doping can provide adequate dopant concentration and junction depth for source/drain. In addition, H_2-diluted phosphorus PIII can promote dopant activation more efficiently during RTA at 600 °C than with conventional ion implantation (II) technology. The excellent characteristics of PIII doped poly-Si TFT's resemble those of conventional II doped ones.**

I. Introduction

FABRICATING polysilicon thin-film transistors (poly-Si TFT's) on large-area glass substrates for active-matrix liquid crystal displays (AMLCD's) applications hinges on developing a low-temperature doping technique for source/drain (S/D). Conventional ion implantation (II) technology is inappropriate for AMLCD's owing to the excessively long implantation time and the inefficient activation at a low temperature. To avert these problems, a ion doping technique with low-temperature activation has been proposed [1]–[7]. However, unresolved problems still arise regarding charge-up on the oxide and heavy-metal contamination from grids.

A previous work has proposed another high dose-rate and large-area doping technique utilizing plasma immersion ion implantation (PIII) [8]. In the PIII system, oxide charge-up can be avoided by applying a negative pulse bias to the substrate. The PIII system's design is relatively simple, leading to a lower production cost. Moreover, PIII process does not lead to any detrimental contamination. Owing to these merits, PIII has been extensively applied in semiconductor processing [9]–[12]. This work, for the first time, investigates the feasibility of applying PIII technology to low-temperature processed (LTP) poly-Si TFT's.

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II. Experimental

Conventional co-planar N-channel poly-Si TFT's with PIII doping were prepared on silicon substrate. The 100-nm-thick active layer was deposited at 550 °C using low pressure chemical vapor deposition (LPCVD) method and recrystallized at 600 °C for 24 h. The 39 nm-thick gate oxide was then grown by liquid-phase deposition [13]. After the gate oxide on S/D regions was removed, the S/D and the 300-nm-thick poly-Si gate were doped (5×10^{15} cm^{-2}) in 5% PH_3/H_2 gas for 5 s using the PIII method. A negative pulse bias of 10 keV with a pulse width of 4 μs and a repetition rate of 12.5 kHz was applied to the substrate during PIII doping. Dopant activation was performed using rapid thermal annealing (RTA) at 600–900 °C for 75 s or furnace annealing at 600 °C for 24 h. As a reference, TFT's with conventional II doping (5×10^{15} cm^{-2}, 10 keV) and furnace annealing at 600 °C for 24 h were also prepared. Finally, aluminum electrodes were formed and sintered at 400 °C for 30 min in N_2 gas. The resistivity and profile of the doped region was verified by initially preparing 300-nm-thick poly-Si films and, then, employing the four-point probe method and the secondary ion mass spectroscopy (SIMS).

III. Results and Discussion

Fig. 1 depicts the transfer characteristics for PIII doped TFT's under different activation conditions. Table I lists the characteristic parameters of these TFT's. For comparison, this table also contains the characteristic parameters of conventional II doped TFT's. Interestingly, the mobility of all PIII doped TFT's is independent of channel length, indicating no parasitic resistance problem at S/D regions [1], [2]. Moreover, no current crowding phenomena were observed in transfer and output characteristics, confirming that PIII doping and activation have provided adequate ohmic contact [3], [4]. Notably, the PIII doped TFT with RTA activation at 600 °C for 75 s exhibits a threshold voltage ($V_{\rm th}$) of 12.19 V, a subthreshold swing (SS) of 1.78 V/dec and a field-effect mobility ($\mu_{\rm FE}$) of 11.03 cm^2/V $\cdot$ s. The higher the RTA activation temperature, the better the TFT characteristics are obtained. It is believed that the higher RTA temperature can yield better activation effects on S/D regions and recrystallization effects, as discussed in more detail later on. With furnace activation at 600 °C for 24 h, PIII doped TFT's can obtain similar characteristics; a $V_{\rm th}$ of 8.90 V, a S.S. of 1.36 V/dec and a $\mu_{\rm FE}$

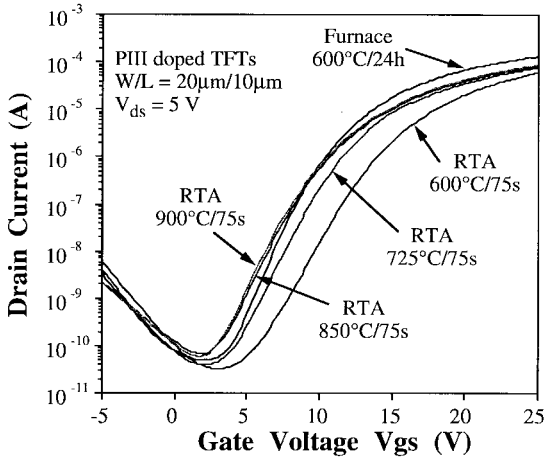

Fig. 1. Typical transfer characteristics $(I_{\rm ds} - V_{\rm gs})$ at $V_{\rm ds} = 5$ V for PIII doped poly-Si TFT's ($W/L = 20$ μm/10 μm) under different activation conditions.

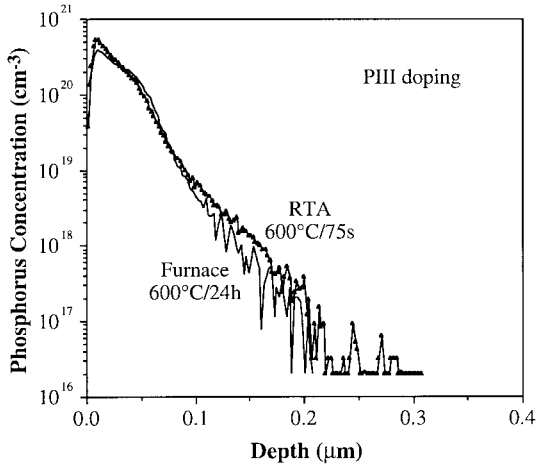

Fig. 2. Phosphorus concentration profiles in PIII doped poly-Si films under RTA activation at 600 °C for 75 s and under furnace activation at 600 °C for 24 h.

TABLE I
DEVICE CHARACTERISTIC PARAMETERS FOR POLY-SI TFT'S ($W/L = 20$mm/10mm) UNDER DIFFERENT DOPING AND ACTIVATION PROCESSES.

Doping	Activation	V_{th} (V)	S.S. (V/dec)	I_{on}/I_{off}	μ_{FE} ($cm^2/V{\cdot}s$)
Plasma Immersion Ion Implantation	RTA/600°C/75s	12.19	1.78	1.84×10^6	11.03
	RTA/725°C/75s	9.94	1.59	1.93×10^6	13.31
	RTA/850°C/75s	9.62	1.53	1.21×10^6	14.19
	RTA/900°C/75s	8.71	1.51	1.46×10^6	15.63
	Furnace/600°C/24h	8.90	1.36	2.69×10^6	15.19
Ion Implantation	Furnace/600°C/24h	8.77	1.35	3.72×10^6	15.02

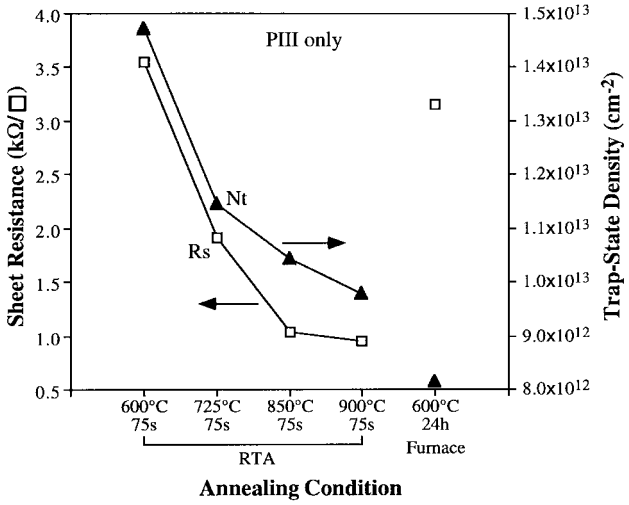

Fig. 3. Changes in sheet resistance (R_s) of PIII doped poly-Si films and trap-state density (N_t) of poly-Si TFT's under 600°C–900°C RTA activation for 75 s and under 600°C furnace activation for 24 h.

of 15.19 $cm^2/V{\cdot}s$, as II doped TFT's. These characteristics confirm that PIII doping can obviously replace conventional II as doping technology for poly-Si TFT's. Notably, under the same activation temperature of 600 °C, PIII doped sample with 75 s of RTA activation can nearly achieve the characteristics as that of II doped samples with 25 h of furnace activation. This finding suggests that PIII technology itself is helpful to the low-temperature activation. To elucidate this effect, hereinafter, we also investigated how activation conditions influence the resistivity of PIII doped regions. The influences of S/D resistivity on TFT characteristics were analyzed as well.

S/D resistivity is related to the doped profile and the dopant concentration, accounting for why we initially analyzed two doped profiles after 600 °C activation. Fig. 2 displays the SIMS profiles of PIII doped films activated with RTA at 600 °C for 75 s and with furnace at 600 °C for 24 h, respectively. According to this figure, the two profiles closely resemble each other due to the low activation temperature of 600 °C. The profiles also reveal that the peaks are located at about 10 nm. The profile depths with the concentration exceeding 1×10^{19} cm^{-3} reach 90 nm, i.e., nearly equal to the active layer's thickness. According to these results, PIII doping with RTA activation at 600 °C for 75 s can provide optimum S/D junction depth and dopant concentration for TFT's.

Next, we investigated the resistivity variation of PIII doped regions under different activation conditions. Fig. 3 illustrates the changes in sheet resistance (R_s) of PIII doped poly-Si films under different activation conditions. The higher the RTA activation temperature, the lower the R_s is obtained. For TFT devices, the lower S/D resistivity implies better TFT characteristics. Notably, the R_s (3.55 kΩ/□) under 600 °C RTA activation for 75 s is nearly the same as that (3.16 kΩ/□) under 600 °C furnace activation for 24 h. In addition, the R_s of PIII doped samples with 600°C activation also resemble that of conventional II doped ones. This finding confirms that PIII technology accompanying with RTA at 600 °C for 75 s is sufficient to provide excellent S/D resistivity for TFT's.

Although the activation effects are comparable at 600 °C, the characteristics of TFT's with RTA activation obviously differ from those with furnace activation. In fact, the thermal treatment also has a recrystallization effect on the channel region in addition to S/D activation. As Fig. 3 depicts, the trap-state density (N_t) is 8.15×10^{12} cm^{-2} and 1.47×10^{13} cm^{-2} for TFT's activated with furnace at 600 °C for

24 h and with RTA at 600 °C for 75 s, respectively. It reveals that for TFT's activated with RTA, the high N_t largely accounts for the poor characteristics. Therefore, as long as trap states in the active layers are effectively reduced, PIII doping accompanied by RTA activation at 600 °C can yield excellent TFT characteristics.

IV. Summary

This work has successfully applied PIII phosphorus doping technology to LTP poly-Si TFT's. Its depth profile and dopant concentration can satisfy the requirement of thin active layer. While possessing the implantation of hydrogen ions, PIII technology can promote activation. In addition, the doped regions exhibit low sheet resistance without parasitic resistance, and thus can provide excellent S/D regions. Moreover, the characteristics of PIII doped TFT's are comparable with those of conventional ion-implanted TFT's. Therefore, the novel PIII technology is a promising alternative to conventional ion implantation for large-area AMLCD's.

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