Briefs

An Analytical Grain-Barrier Height Model and Its Characterization for Intrinsic Poly-Si Thin-Film Transistor

Hsin-Li Chen and Ching-Yuan Wu

***Abstract*— An analytical model for the grain-barrier height of the intrinsic poly-Si thin-film transistors (TFT's) is developed, in which the grain-barrier height for the applied gate voltage smaller than the threshold voltage is obtained by solving the charge neutrality equation and the grain-barrier height for the applied gate voltage larger than the threshold voltage is obtained by using the quasi-two-dimensional (2-D) method. Good agreements between experimental and simulation results are obtained for wide gate voltage range.**

***Index Terms*—GB states, grain-barrier height, grain size, intrinsic poly-Si TFT.**

I. Introduction

The intrinsic poly-Si thin-film transistors (TFT's) have received extensive attention for their potential applications in the large-size active-matrix liquid crystal display (AMLCD) [1]–[3] and the high-density TFT SRAM and nonvolatile memory [4]. The grain boundary trapped theory has been studied by several works [5]–[8] to interpret the transport behaviors in poly-Si based devices. Serikawa *et al.* [7] had used an empirical formula to fix the grain-barrier height of 0.55V at the threshold voltage (V_{T0}). Lin *et al.* [8] had considered the charge coupling between the gate bias (V_{GS}) and grain boundary (GB) states by using the quasi-two-dimensional (2-D) method to obtain the grain-barrier height. However, these models are all developed for the doped poly-Si TFT's and are invalid for the intrinsic poly-Si TFT's.

In this paper, an analytical grain-barrier height model for the intrinsic poly-Si TFT's is proposed by considering the charge neutrality condition between the intrinsic free carriers and the grain-boundary states in $V_{GS} \leq V_{T0}$ regime. For $V_{GS} > V_{T0}$, due to part of the induced electrons trapped into the GB states, the electrical coupling between the gate voltage and the GB states appears and the grain-barrier height in this regime is obtained by solving the two-dimensional electrostatic problem. Comparisons of the grain-barrier height between experimental values and theoretical results are made and excellent agreements are obtained.

II. The Grain-Barrier Height Model

A. For $V_{GS} \leq V_{T0}$

Due to the few free concentration (with the intrinsic carrier concentration of Si, n_i), the crystalline regions within intrinsic poly-Si grains will be fully depleted. The cross-section view of the intrinsic n-channel poly-Si TFT is shown in Fig. 1(a) with $x_d = L_G/2$. For simplicity, only one grain along the channel is shown. Assume there are enough intragrain defect-states to trap the free holes to form the depletion region. The monoenergetic trap level (E_T) is used to characterize the distribution of the GB states within the bandgap. The charge neutrality equation within a fully depleted grain is obtained as follows:

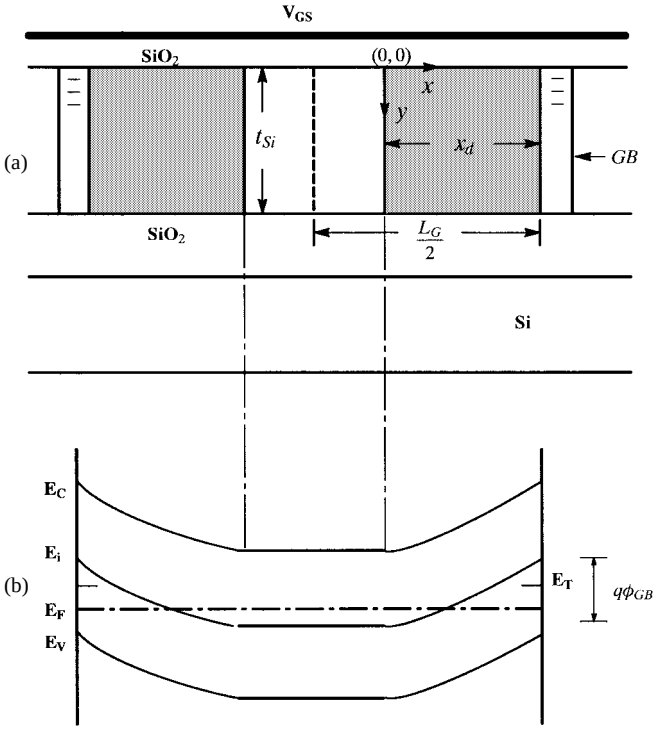

Fig. 1. (a) The cross section view of the intrinsic n-channel poly-Si TFT around a grain; (b) the corresponding energy band diagram. Only one grain is shown for simplicity. The dark region is the depletion region where the potential distribution function is solved by using quasi-2-D method.

$$qL_G n_i = \frac{qN_{ST}}{1 + \frac{1}{2}\exp\left(\frac{E_T - E_F|_{x=L_G/2}}{kT}\right)} \tag{1}$$

where L_G is the grain size, N_{ST} is the density of the GB trap state per area, and E_F is the Fermi level. From the energy band diagram shown in Fig. 1(b), the following relationship can be obtained:

$$(E_T - E_F)|_{x=(L_G/2)} = (E_T - E_i) + q\phi_{GB} - (E_F - E_i)|_{x=0}. \tag{2}$$

From (1) and (2), the grain-barrier height can be obtained as follows:

$$\phi_{GB} = \frac{kT}{q}\ln\left[2\left(\frac{N_{ST}}{L_G n_i} - 1\right)\right] - \frac{E_T - E_i}{q} + \frac{E_F - E_i|_{x=0}}{q}. \tag{3}$$

Because the poly-Si film is intrinsic, $(E_F - E_i)|_{x=0}$ in (3) can be approximated to be zero.

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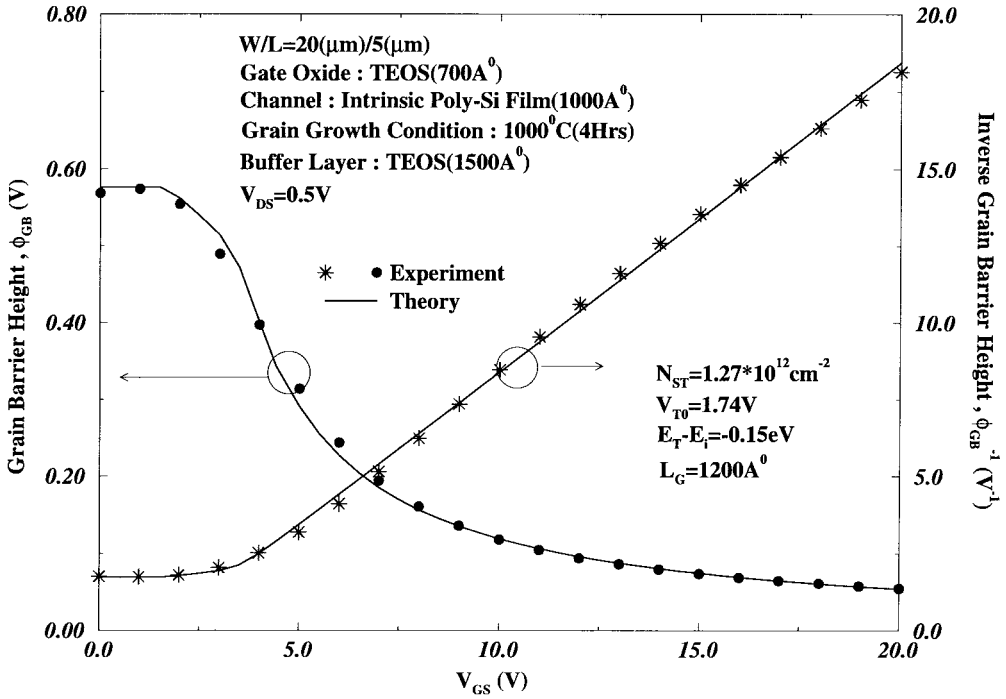

Fig. 2. The curves showing comparisons of the grain-barrier height and its inverse versus the gate voltage of the intrinsic n-channel poly-Si TFT between the experiment and simulation results.

B. For $V_{GS} > V_{T0}$

The depletion region, i.e. the dark region shown in Fig. 1(a), is composed of the electrons with concentration n_i trapped in the intragrain defect-states. The potential distribution function is assumed to be of the form: $\psi(x,y) = \psi(0,0) + \phi(x)$, where $\psi(0,0)$ is the potential at the depletion edge along the surface and $\phi(x)$ represents the potential variation accounting for the formation of the grain-barrier height. The dependence of $\psi(x,y)$ on the depth direction (y) is neglected because of the thin poly-Si film. From the Gauss's law, the integral equation for $\psi(x,y)$ is obtained as follows:

$$-\frac{C_{OX}}{\epsilon_{\rm Si}}\int_0^x [V_{GS} - V_{FB} - \psi(x',0)]\,dx' - \int_0^{t_{\rm Si}} \frac{\partial}{\partial x}\psi(x,y')\,dy' = -\frac{qn_i t_{\rm Si} x}{\epsilon_{\rm Si}} \tag{4}$$

where $t_{\rm Si}$ is the thickness of the poly-Si film. By solving (4) with appropriate boundary conditions, the grain-barrier height can be obtained as follows:

$$\phi_{GB} = |\phi(x_d)| = \left[V_{QN}^2 + \left(\frac{Q_{ST}}{2K\epsilon_{\rm Si}}\right)^2\right]^{1/2} - V_{QN} \tag{5}$$

where $K = ((C_{OX}/\epsilon_{\rm Si})(1/t_{\rm Si}))^{1/2}$, $V_{QN} = V_{GS} - V_{FB} - \psi(0,0) - (qn_i t_{\rm Si}/C_{OX})$, and $Q_{ST} = (qN_{ST}/1 + (1/2)\exp((E_T - E_F|_{x=x_d}/kT))$. The asymptotic form of the grain-barrier height from (5) with high V_{GS} can be obtained as follows:

$$\phi_{GB} = \frac{t_{\rm Si}}{C_{OX}(V_{GS} - V_{T0})}\,\frac{(qN_{ST})^2}{8\epsilon_{\rm Si}} \tag{6}$$

where $V_{T0} = V_{FB} + \phi_{\sin v} + (qn_i t_{\rm Si}/C_{OX})$. The factor $t_{\rm Si}$ in (6) accounts for the fully depleted condition of the intrinsic poly-Si film, as compared to the partially depleted one of the doped poly-Si film, denoted by the factor $y_{d\rm inv}/3$ in [8]. From (6), the reciprocal relationship between ϕ_{GB} and V_{GS} is obvious.

III. Results and Discussion

In order to test the validity of the grain-barrier height model developed, n-channel intrinsic poly-Si TFT's, which were obtained by the standard fabrication process as the conditions detailed in Fig. 2, are characterized. The curve of ϕ_{GB} versus V_{GS} is shown in Fig. 2, where ϕ_{GB} is obtained from the Arrhenius plot for the drain-source current. From the experimental curve of $1/\phi_{GB}$ versus V_{GS} in $V_{GS} > V_{T0}$ regime and invoking (6), N_{ST} and V_{T0} can be extracted, as listed in Fig. 2. By optimizing the fitting results with (5), $(E_T - E_i)$ and $(E_F - E_i)|_{x=0}$ can be extracted. $(E_F - E_i)|_{x=0}$ is 0.4 eV, which is reasonable for the intrinsic poly-Si in the strong inversion condition. L_G, extracted from $V_{GS} \le V_{T0}$ regime by using (3) with the parameters extracted previously, is 1200 Å, close to the TEM measurement result. As shown in Fig. 2, good agreements are obtained between experimental and simulation results over wide gate voltage range. The deviation in $V_{GS} \le V_{T0}$ regime in [8] has been successfully corrected by our developed model. This correction shows that the charge neutrality condition between the free carriers and GB states accounts for the fixed ϕ_{GB} in $V_{GS} \le V_{T0}$ regime. As shown in (3), the value of the fixed ϕ_{GB} is determined by the process conditions through L_G and N_{ST}.

IV. Conclusion

An analytical grain-barrier height model for the intrinsic poly-Si TFT's has been obtained for wide gate voltage range based on the charge neutrality equation and the quasi-2-D method. By this model and invoking the distinct characteristics of the fully depleted grains for the intrinsic poly-Si film, the grain size can be accurately extracted and the formation mechanism of the fixed ϕ_{GB} in $V_{GS} \le V_{T0}$ regime can be clarified. The grain-barrier height of the fabricated intrinsic poly-Si TFT's has been measured and characterized. Very good agreements are obtained between experimental and simulated results with the reasonably acceptable parameters.

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Tunnelling Transport in Al-n-GaSb Schottky Diodes

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***Abstract*— Investigations of Al Schottky contacts to n-GaSb are presented. Barrier heights of 0.60 ± 0.02 eV are found. Forward bias ideality factors between 2 at 300 K to 60 at 10 K, are explained by electron tunneling. Ideality factors yield donor concentrations significantly greater than nominal, accentuated by annealing, suggesting modification of the reactive GaSb surface.**

***Index Terms*—Gallium antimonide, ideality factor, interface modification, Schottky diode.**

I. INTRODUCTION

Reliable metallization processes are crucial to device fabrication, but little attention appears to have yet been paid to the case of GaSb. GaSb has a relatively small heat of formation, so is susceptible to surface thermal degradation and a low thermal budget protocol for ohmic contacts to both n- and p-type GaSb has been reported [1]. Little consistency is found in reports on the rectifying properties of GaSb Schottky barriers [2]–[5]. The fragility of the surface is manifest in the preferential loss at relatively low temperatures of antimony, [2], reactivity with adventitious or deposited species is also high. The refractory metals, attractive as rectifying contacts to the n-type semiconductors because of their compatibility with ohmic metallization of p-GaSb, tend to be highly reactive.

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We present here a study of Al used as a Schottky barrier to n-GaSb because of its technological utility. Al is the preferred choice, since it is easy to use, compatible with existing fabrication technologies, and can be simultaneously used as an ohmic contact to p-type GaSb, thus leading to simpler technological recipes for bipolar devices. We show that suitable ex-situ surface preparation and deposition routines lead to GaSb Schottky diodes with good and reproducible rectifying properties, behavior which persists even after heating to 500 °C. We show the dominant role of forward bias tunnel current, and, by using the tunnel current as a probe, we illustrate the GaSb surface modification resulting from quite modest thermal processing.

II. EXPERIMENTAL

Diodes were fabricated on (100) Te-doped n-GaSb wafers with nominal doping concentrations of 6 to 9 × 10^{17} cm^{-3}. Ohmic contacts were formed first, using AuNiGe annealed at 200 °C for 1 min in a nitrogen atmosphere [1]. Schottky barrier formation required the removal of native oxide layers before metal deposition, a critical step since GaSb has a high atmospheric oxidation rate [4]. After etching with dilute HCl for one minute, samples were briefly rinsed in deionized water, spin-dried in a dry nitrogen jet and quickly loaded into a vacuum metal deposition chamber. Test structures with dimensions 500 × 500 μm and 400 × 400 μm were examined. The $C-V$ characteristics were taken at 1 MHz. $I-V$ curves were measured at 10 K intervals between 10 and 370 K. Thermal post-treatment used a standard RTA furnace in dry N_2 atmosphere.

III. RESULTS AND DISCUSSION

The C^{-2}-V plot of an Al/n-GaSb diode gives a barrier height of 0.62 eV while the slope gives a donor concentration at the edge of the depletion region of 9 × 10^{17} cm^{-3}, in good agreement with the measured value for the wafer. I-V characteristics yield room temperature forward-to-reverse current rectification ratios of approximately 5 at 0.2 V and 15 at 0.3 V. Semilogarithmic plots of the I-V characteristics of a typical Al/n-GaSb diode over a temperature range of 10–370 K show good linearity in the forward direction, so ideality factors can be derived. In view of the high doping levels and small effective mass of electrons both tunnelling and thermionic emission processes need to be considered as contributing to forward current. For a Schottky barrier on a highly-doped n-type semiconductor, tunnelling through the barrier dominates the forward bias current [6]. The forward current is given by

$$I = I_0 \exp \frac{qV_E}{nkT} \tag{1}$$

where the ideality factor $n = \eta \coth \eta$. The parameter η depends on the depletion charge density N_D through $\eta = (q\hbar/2kT)\sqrt{N_D/\epsilon m^*}$. Here $\hbar$ is the reduced Planck constant and m^* is the electron effective mass taken as equal to the conductivity effective mass of 0.38 × 10^{-31} kg. The ideality factor n can be derived from the linear part of the experimental $I-V$ curves using (1), and shows a strong temperature dependence—the value of n is 2 at room temperature, falling to about 1.75 at 370 K but rising smoothly to 60 at 10 K. The ideality factor as a function of temperature predicted by (1) is included in Fig. 1 as a solid line. The fit is excellent over the full temperature range for an assumed donor density of 6 × 10^{18} cm^{-3}. This value is a factor of seven higher than that obtained from the