

Full Control of a PWM DC-AC Converter for AC Voltage Regulation

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The design and implement action of a DSP-based fully digital-controlled single-phase pulsewidth modulated (PWM) dc-ac converter for ac voltage regulation is described. The proposed multiloop digital controller (MDC) consists of a current controller, a voltage controller, and a feedforward controller. This MDC was realized using a single-chip digital signal processor (DSP). The PWM gating signals are determined at every sampling instant by the proposed multiloop digital control scheme using a set of detected feedback signals. A software current control scheme has been developed to achieve fast current control of the PWM inverter and decouple the inductor of the output filter. Experimental results have been given to verify the proposed digital control scheme. The constructed DSP-based PWM dc-ac converter system can achieve fast dynamic response and with low total harmonic distortion (THD) for rectifier type of loads.

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I. INTRODUCTION

In recent years, closed-loop regulated pulsewidth modulated (PWM) dc-ac converters have found their wide applications in various types of ac power conditioning systems, such as automatic voltage regulator (AVR) systems, uninterruptible power supply (UPS) systems, and programmable ac source (PAS) systems. In these applications, the PWM dc-ac converters are required to maintain a sinusoidal output waveform under various types of loads and this can only be achieved by employing feedback control technique.

To minimize the total harmonic distortion (THD) in the output voltage, selected harmonic elimination PWM and programmed PWM techniques have been used to regulate the fundamental amplitude and eliminate low-order harmonics [1, 2]. However, these kinds of control techniques cannot meet the stringent requirements of modern high-performance ac power conditioning systems. Therefore, closed-loop regulation of PWM inverters becomes an important issue in application of high performance ac power conditioning systems.

During the past several years, various closed-loop control schemes for the PWM inverter with instantaneous feedback by using analog techniques have been proposed to achieve both good dynamic response and low harmonic distortion [3, 4]. The instantaneous feedback control with adaptive hysteresis regulates the PWM inverter with direct current and voltage feedback [5, 6]. This control scheme changes the hysteresis width as a function of the voltage reference, but its dynamic responses to large load change or rectifier types of load are left unsolved. Instantaneous voltage feedback with an inner current loop was also developed for the control of PWM inverters.

Although frequency-domain-based analog control schemes are predominantly used in compensator design of power converters, there are several drawbacks that hinder the performance of analog controllers, such as temperature drift, aging effect, complexity in component adjustment, and susceptibility to electromagnetic interference (EMI). With the rapid progress in microelectronics technology, digital control of power converters using advanced microcontroller and digital signal processor (DSP) becomes an active research area [7, 9]. Microprocessor-based deadbeat control technique has been applied to the closed-loop regulation of PWM inverters for UPS applications [10, 11]. Deadbeat control scheme has the disadvantages of highly sensitive to parameter and load variations and requiring large peak-to-average ratio of control signals to achieve dead beat effect. Recently, discrete sliding mode control (DSMC) technique has been developed for the regulation of PWM inverters [12]. The main

advantage of the DSMC scheme is its insensitivity to parameter variations and load disturbances, which leads to invariant steady-state response in the ideal case, while its disadvantages are that it is not easy to find an appropriate sliding surface and its performance will be degraded with a limited sampling rate.

With the availability of 16-bit high-performance DSP chips, most of its instructions can be accomplished in one instruction cycle and complicated control algorithms can be executed with fast speed. This work describes the design and implementation of a DSP-based fully digital-controlled single-phase PWM inverter for ac voltage regulation. The proposed digital controlled PWM inverter system employs a single-chip DSP to realize a multiloop control scheme with sinusoidal reference. The PWM gating signals are determined at every sampling instant by the proposed multiloop digital control scheme using a set of detected feedback signals.

There has been some research on the digital control of PWM inverters for ac voltage regulation, but theoretical analysis and realization of the digital controller still need further study. This work proposes a multiloop digital control scheme for the closed-loop regulation of PWM inverters used for high-performance UPS and AVR systems. Section II makes an analysis of the dynamic behavior of the dc-ac converter of an ac voltage regulator. Section III introduces the proposed multiloop control scheme for the closed-loop regulation of a PWM inverter. Section IV describes the implementation of the digital controller using a single-chip DSP. Section IV gives some simulation and experimental results to verify the proposed multiloop digital control strategy. Section V is the conclusion.

II. DYNAMIC ANALYSIS OF DC-AC CONVERTERS

A. DSP Control of a PWM DC-AC Converter

The dc-ac converter used in an UPS/AVR system usually consists of a pulsewidth modulated H-bridge inverter and an LC filter. The block diagram of the proposed DSP-controlled dc-ac converter used for ac voltage regulation is shown in Fig. 1, where the dc-ac converter and the connected load is considered as the plant of a closed-loop digital feedback system. The DSP controls the inverter switches so that the output voltage can track the sinusoidal reference at each sampling instant. In the proposed system, the inductor current and the output voltage are sensed as feedback variables, and the control algorithm computes the required pulsewidth for the dc-ac converter.

There are many consideration factors in the selection of a microprocessor in the design of a digital control system. After a thorough consideration of performance, price, simplicity in hardware design, and software support, we choose a single-chip DSP

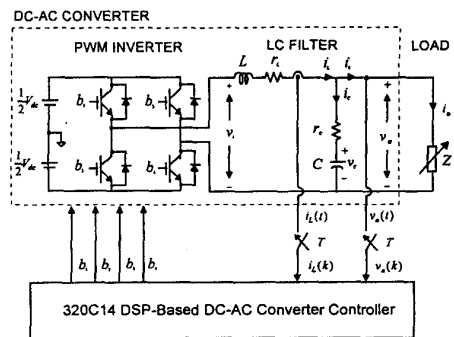


Fig. 1. DSP-based digital control of a dc-ac converter for ac voltage regulation.

(TMS320C14) from Texas Instruments to realize the digital controller for ac voltage regulation [13]. The TMS320C14 has many good features, which make it a good candidate to realize digital control for power converting systems, such as multiple independent programmable timers, 160 ns instruction cycle, 16-bit parallel multiplier, and on-chip RAM and ROM, etc.

B. Modeling of DC-AC Converter

In this work, we present a control strategy based on linear system theory. However, the dc-ac converter concerned here is a nonlinear system by nature due to the existence of the solid-state switches. A nonlinear system must be first linearized around its operating point before the linear controller can be designed. The performance of the controlled system in the neighborhood of that operating point can be guaranteed if the designed controller is robust enough. The wider the bandwidth of the system, the larger the neighborhood. Here, a nominal resistive load is set as the operating point for linearization.

Fig. 2(a) shows the equivalent circuit of a dc-ac converter with connected load. The dc-ac converter system shown in Fig. 1 is a discrete nonlinear system. A linear sampled-data model was developed for the analysis and synthesis of a discrete dead beat controller [14]. Essentially, a digital-controlled power converting system is a multirate digital control system because there are two frequency components: one is the sampling frequency of the digital controller, and the other is the switching frequency of the power converter.

In the past, because of the limited computation speed of available microprocessors, the sampling frequency is much lower than the switching frequency. This hinders and hesitates the application of digital control techniques to the power converting systems, especially in the area of the dc and/or ac power supplies. However, the switching frequency of a power converting system is still limited due to the irreducible switching losses of the power devices and magnetic cores. But in the mean time, there is a great

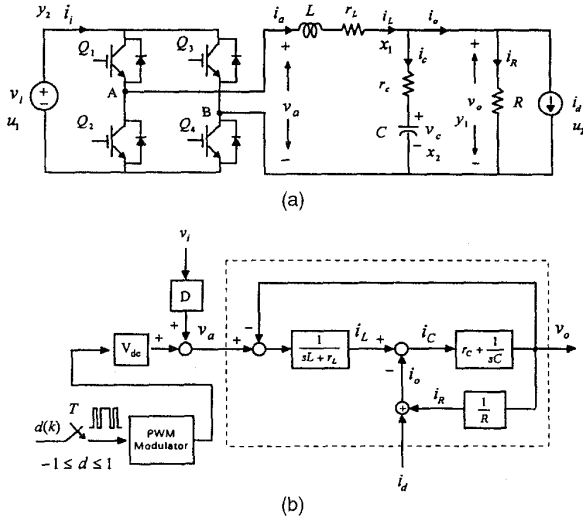


Fig. 2. Modeling of a dc-ac converter. (a) Equivalent circuit. (b) Block diagram representation.

improvement in the performance of microprocessors and digital control integrated circuits (ICs) [15]. With the recently developed high-performance DSP, realization of digital controllers with higher sampling rate becomes possible and this makes the sampling frequency gradually approach the switching frequency of a digital-controlled power converting system.

The dynamics of a dc-ac converter is mainly determined by the LC filter and connected load. The complexity in the modeling and control of a dc-ac converter used for UPS applications comes from the connected load. The load connected to an UPS system may be nonlinear, periodically switched, regenerative, highly inductive, or time varying. Because of the diversity of these loads, it is not possible to formulate a general model to cover every kind of load. However, we can define a load as a nominal operating condition point to derive its linear model and consider the load variations and model uncertainties as a specified load disturbance. The LC filter with a nominal resistive load can be modeled as a continuous time second-order system with state variables v_C and i_L , output load voltage v_0 and input voltage v_a , which takes three values $0.5V_{dc}$, $0.5V_{dc}$, or zero. Consider the inductor equivalent series resistance (ESR) r_L and capacitor ESR r_C , the state equation and output equation become

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} \frac{r_L r_C + R(r_L + r_C)}{L(R + r_C)} & -\frac{R}{L(R + r_C)} \\ \frac{1}{C(1 + r_C/R)} & \frac{1}{RC(1 + r_C/R)} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} v_a \quad (1)$$

$$v_0 = \begin{bmatrix} \frac{r_C}{R + r_C} & \frac{R}{R + r_C} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix}. \quad (2)$$

The transfer function of the inverter output voltage v_a to the filter output voltage v_0 is

$$G_p(s) = \frac{v_0(s)}{v_a(s)} = \frac{b_1 s + b_0}{a_2 s^2 + a_1 s + a_0} \quad (3)$$

where $b_1 = r_C RC$, $b_0 = R$, $a_2 = (R + r_C)LC$, $a_1 = L + (r_L + r_C)RC + r_L r_C C$, and $a_0 = r_L + R$. The open-loop output impedance is defined as

$$Z_0(s) = \frac{v_0(s)}{i_0(s)} = \frac{r_C LC s^2 + (r_C r_L C + L)s + r_L}{LC s^2 + (r_L + r_C)Cs + 1}. \quad (4)$$

It can be observed from (3) that the capacitor ESR r_C will introduce a zero located at $z_c = -1/r_C C$. This left-half plane zero compared with the natural resonant pole of the LC filter located at $p_0 = -1/\sqrt{LC}$ has a ratio of

$$\frac{z_c}{p_0} = \frac{1}{r_C} \sqrt{\frac{L}{C}}. \quad (5)$$

The capacitor ESR r_C is usually very small and this zero is high above the resonant frequency of the LC tank. If the ESRs of the LC filter are small enough and can be neglected, (1) and (2) can be simplified as

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & \frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_a \quad (6)$$

$$v_0 = [0 \quad 1] \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad (7)$$

and (3) and (4) can also be reduced as

$$G_p(s) = \frac{v_0(s)}{v_a(s)} = \frac{R}{RLC s^2 + Ls + R} \quad (8)$$

$$Z_0(s) = \frac{v_0(s)}{i_0(s)} = \frac{Ls + 1}{LC s^2 + 1}. \quad (9)$$

The modeling of a digital-controlled PWM dc-ac converter can be represented by a block diagram as shown in Fig. 2(b). As shown in Fig. 2(b), there is a discrete duty ratio $d(k)$ applied to a PWM modulator. The $d(k)$ is determined at every sampling interval T_D from a digital controller. The PWM modulator generates the PWM gating signals according to a modulation strategy. A variety of PWM methods have been developed to reduce both the switching losses and current ripples [16]. The digital unipolar PWM method as shown in Fig. 3 has characteristics of minimum current ripple and simple switching mechanism and is adopted here for the generation of the PWM switching patterns.

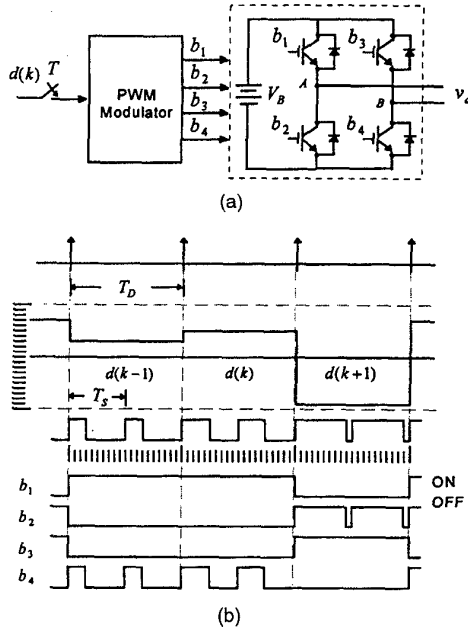


Fig. 3. Unipolar pulsewidth modulation of a full-bridge converter. (a) Circuit diagram. (b) Timing diagram.

C. Analysis of Current-Loop Control

Current mode control techniques are usually employed in the design of power converters and motor drives. Fig. 4 illustrates the employment of an inner current loop within the outer voltage loop in the closed-loop regulation of a PWM dc-ac converter. If the dc-ac converter is closed-loop regulated using only voltage feedback as shown in Fig. 4(a), the increase of the voltage loop gain K_1 has a tendency to destabilize the system and its root locus is as shown in Fig. 5(a). With the adding of a current control loop, as shown in Fig. 4(b), the input-to-output transfer function of the current control loop is

$$G_c(s) = \frac{i_L(s)}{i_L^*(s)} = \frac{K_2[s(R+r_C)C+1]}{a_2s^2 + [K_2(r_C+R)C+a_1]s + (K_2+a_0)} \quad (10)$$

It can be seen from (10) that the zero introduced by the load resistor and capacitor ESR will not be changed by adding a current loop. If r_L and r_C can be neglected, (10) can be reduced as

$$G_c(s) = \frac{K_2(sRC+1)}{s^2RLC + s(K_2RC+L) + (K_2+R)} \quad (11)$$

When the current loop gain K_2 approaches to infinity, one of its poles will approach to $-1/RC$, and it will be canceled out by the zero of (11), another pole will approach to $-K_2/L$ and becomes the dominant pole. From the above analysis, the current loop has the effect of decoupling the resonant poles produced by the LC filter and the dominant pole

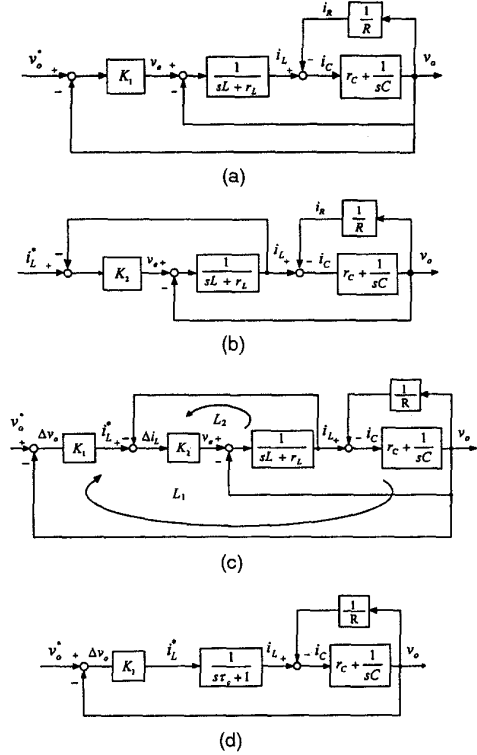


Fig. 4. Control structures for a dc-ac converter. (a) Voltage loop control. (b) Current loop control. (c) Voltage loop control with inner current loop control. (d) Simplified block diagram of (c).

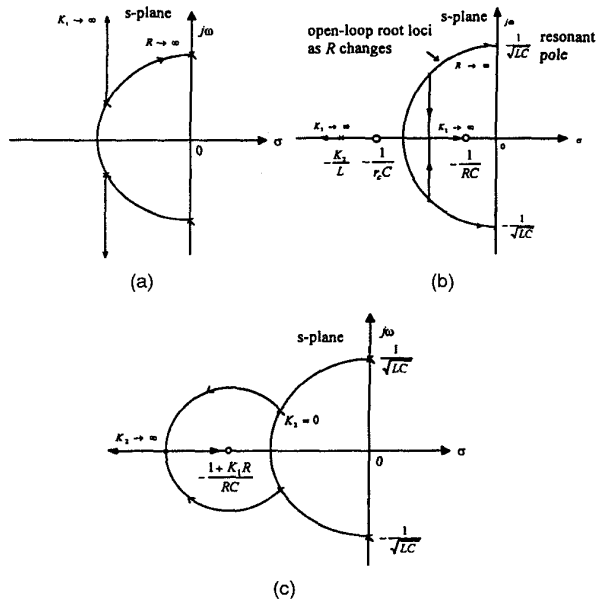


Fig. 5. Decoupling effect of analog current control, and root loci of $s^2RLC + sL + R + K_2(sRC + 1 + K_1R) = 0$.

will be limited by the filter inductor and permissible current-loop gain.

By adding a current loop to control the inductor current as shown in Fig. 4(c), the output reflected

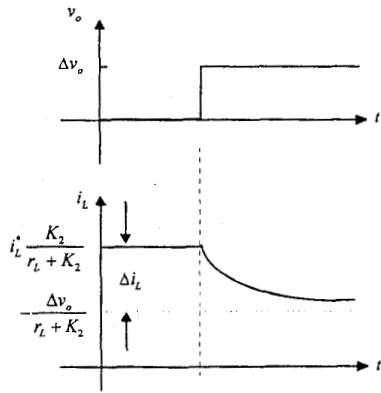


Fig. 6. Effect of output voltage change on inductor current.

voltage v_0 can be viewed as a disturbance. The inductor current can be expressed as

$$i_L = i_L^* \frac{K_2}{sL + (r_L + K_2)} - v_0 \frac{1}{sL + (r_L + K_2)}. \quad (12)$$

The current-loop gain K_2 has a unit of ohm. If v_0 is viewed as a disturbance, it can be seen from (12) that a step change of Δv_0 has an influence on i_L with magnitude of $\Delta v_0 / (r_L + K_2)$ as shown in Fig. 6. The usual condition is $r_L \ll K_2$, therefore, the influence of Δv_0 on i_L is $\Delta v_0 / K_2$. If this steady-state current error should be less than $\mu_i i_L^*$ with $0 \leq \mu_i \leq 1$, then

$$\frac{\Delta v_0}{K_2} < \mu_i i_L^* \quad (13)$$

which means $K_2 > \Delta v_0 / \mu_i i_L^*$. If we define $\Delta v_0 = \mu_v V_{dc}$ with $0 \leq \mu_v \leq 1$, then the current loop gain K_2 should satisfy the following requirement

$$K_2 > \frac{\mu_v V_0}{\mu_i i_L^*}. \quad (14)$$

In steady-state condition, $I_{L(rms)} = I_{0(rms)}$, and the requirement of the current-loop gain can be expressed as

$$K_2 > \left(\frac{\mu_v}{\mu_i} \right) \frac{V_{0(rms)}}{I_{0(rms)}} = \left(\frac{\mu_v}{\mu_i} \right) R_0 \quad (15)$$

where R_0 is the resistance of a rated resistive load. If the current-loop gain K_2 can satisfy the requirement of

(15), then (12) can be approximated by

$$i_L = i_L^* \frac{K_2}{sL + (r_L + K_2)}. \quad (16)$$

In practical condition, the inductor ESR is much smaller than K_2 and (16) can be simplified as

$$i_L = i_L^* \frac{K_2}{sL + K_2}. \quad (17)$$

With the high gain requirement of the current-loop controller (CLC), the current loop dynamics can be simplified by a first-order system with an equivalent electrical time constant τ_c as shown in Fig. 4(d). The current loop has a time constant of

$$\tau_c = \frac{L}{K_2} \quad (18)$$

and its bandwidth f_c (Hz) is

$$f_c = \frac{1}{2\pi} \frac{K_2}{L}. \quad (19)$$

The inclusion of an inner CLC in the closed-loop regulation of a PWM dc-ac converter has the following advantages:

- 1) eliminate the influences of the inductor parameter variation,
- 2) has the effect of decoupling the LC-filter resonant poles and making the design of the LC-filter easier,
- 3) inherent current limiting capability,
- 4) the minor CLC and the major voltage-loop controller (VLC) can be designed and implemented separately.

III. MULTILoop DIGITAL CONTROL SCHEME

The proposed multiloop digital controller (MDC) for the closed-loop regulation of a PWM dc-ac converter is shown in Fig. 7. The MDC consists of three controllers: the CLC, the VLC, and the feedforward controller (FC). The design of the multiloop controller is described in the following.

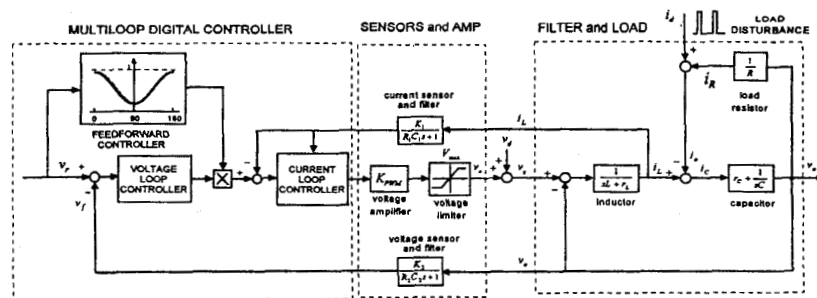


Fig. 7. Block diagram of multiloop digital control scheme for the voltage regulation of a PWM dc/ac converter for ac voltage generation.

A. Digital Current-Loop Controller

If the sampling period of the CLC is much smaller than the electrical time constant of the filter inductor, i.e., $T_D \ll L/r_L$, a linear approximation of the inductor current can be used to derive the dead beat control algorithm for the inductor current control. The proposed discrete current control algorithm is

$$\Delta i_L(k) = i_L^*(k) - i_L(k) \quad (20)$$

$$v_a(k) = \Delta i_L(k) \frac{L}{T_D} + v_0(k) + i_L(k)r_L \quad (21)$$

$$d(k) = v_a(k)/V_{dc}(k) \quad (22)$$

where $v_0(k)$ is the feedback output voltage and $V_{dc}(k)$ is the dc link voltage.

The maximum current incremental during one sampling interval can be expressed as

$$\Delta I = \frac{(V_{dc} - v_0 - i_0 r_L) T_D}{L} \quad (23)$$

This current incremental reaches its maximum when the output voltage and current are both zero, and reaches its minimum when both are maximum. If we define

$$\Delta V_{\min} = V_{dc} - v_{0(\max)} - i_{0(\max)} r_L \quad (24)$$

as the minimum effective control voltage and select the sampling interval of the CLC as

$$T_D = \frac{1}{n} \left(\frac{L}{r_L} \right) \quad (25)$$

then the maximum current incremental in the worst condition is

$$\Delta I = \frac{1}{n} \left(\frac{\Delta V_{\min}}{r_L} \right). \quad (26)$$

In the design of a high-performance ac regulator, the dc link voltage should be kept high to provide a high-current sourcing capability and this is the basis for good load disturbance rejection. Equation (23) can be used as an estimation of the converter's maximum current sourcing capability operating in the worst condition and it is also an important design parameter in the determination of dc-link voltage, filter inductor, and current-loop sampling rate.

B. Digital Voltage-Loop Controller

A variety of control schemes have been developed for the closed-loop regulation of a PWM dc-ac converter. In the proposed approach, a first-order auto-regressive moving-average (ARMA) model is used as the voltage-loop control algorithm which is expressed as

$$u(k) = b_1 u(k-1) + a_0 e(k) + a_1 e(k-1) \quad (27)$$

where

$$e(k) = v_r(k) - v_0(k). \quad (28)$$

The controller parameters of (27) are determined by using the least-squares error (LSE) fitting of a specified time response based on an identified current-controlled plant model. We can measure a time series of $\{i_L^*(k), v_0(k)\}$ when the PWM dc-ac converter is current regulated, connected with a rated resistive load, and closed-loop controlled by employing a simple proportional gain in the VLC to ensure its stability.

With the measured time series of $\{i_L^*(k), v_0(k)\}$, the plant model of the current-regulated dc-ac converter from the current command $i_L^*(k)$ to the output voltage $v_0(k)$ under closed-loop control can be identified, which is denoted as

$$v_0(k) = \hat{b}_1 v_0(k-1) + \hat{a}_0 i_L^*(k) + \hat{a}_1 i_L^*(k-1) + \hat{a}_2 i_L^*(k-2). \quad (29)$$

The model parameters of (29) can be determined by using the recursive LSE system identification technique [18].

With a specified input series of $\{v_r(k)\}$, we can define a cost function

$$J = \sum_{i=1}^N [v_r(i) - v_0(i)]^2 \quad (30)$$

where N is the number of points for the time-response curve fitting. The controller parameters $\{b_1, a_0, a_1\}$ of (27) can be determined by minimizing the cost function defined by (30) [19].

C. Digital Feedforward Controller

The nonlinear FC, as shown in Fig. 7, imposes a gain scheduling effect on the VLC according to the sinusoidal reference and has a function of

$$g(k) = \frac{K-1}{2} \cos\left(\frac{i}{N} 4\pi\right) + \frac{K+1}{2}, \quad i = \text{mod}(k, N/2) \quad \text{and} \quad k \geq 1 \quad (31)$$

where N is the length of the sine reference table, k represents the k th sampling instant of the control process, and K is a scaling constant. The VLC output is multiplied by the FC and therefore the current command to the CLC is

$$i_L^*(k) = u(k)g(k). \quad (32)$$

This nonlinear FC provides higher gain for low modulation and lower gain for high modulation, so that the system can have a higher loop gain for small signal perturbations during low modulation range. While in the high modulation range, the permissible control force is limited by the system voltage limit, and therefore the system should have

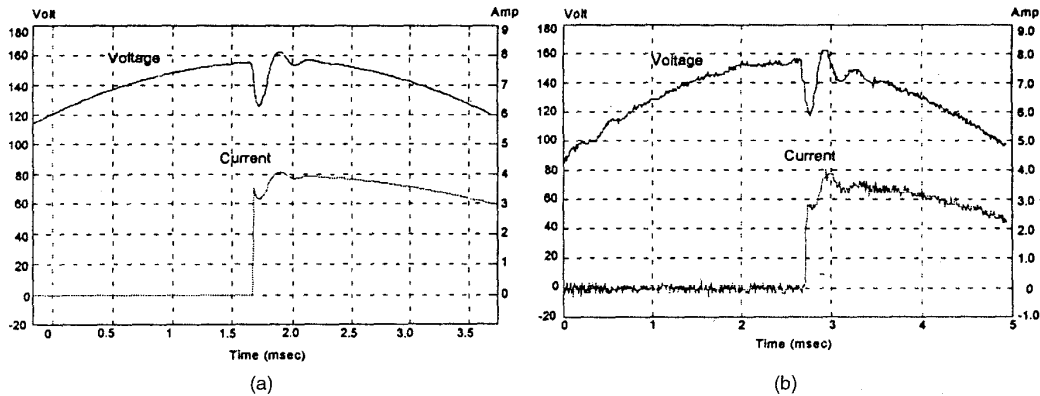


Fig. 8. Output voltage and current waveforms under rated step resistive load change. (a) Simulation. (b) Experimental results.

a lower loop gain to keep stability and prevent from limit-cycle ringing. The FC proposed here is designed empirically. It is hard to prove the stability of the converter system analytically. In this paper, the stability is checked experimentally by applying the worst loading conditions.

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

To verify the proposed control scheme, a 1 kW PWM dc-ac converter using the IGBT GT50J101 from the Toshiba Co. [20] was constructed. A single-chip DSP from Texas Instruments (TMS320C14) was chosen to implement the proposed digital control scheme. The TMS320C14 is essentially a 16-bit microcontroller with DSP architecture; most of its instructions can be executed in one instruction cycle of 160 ns. This single-chip DSP includes a 16-bit digital I/O, 4 timers, 6 channels of PWM, 4 capture inputs, a serial port with UART mode, and 15 interrupts. With its high operation speed and on-chip I/Os, this single-chip DSP is a good choice for the control of power converters and motor drives.

The sampling frequency of the digital CLC is set at 15.36 kHz, therefore there are 256 samples in one period of a 60 Hz sinusoidal waveform. The sampling frequency of the digital VLC and FC is set at 7.68 kHz. The switching frequency of the PWM power stage should be an integral multiple of the sampling frequency to reduce sideband harmonics; at the same time, it is also easier for software and hardware design. In the designed system, the switching frequency of the PWM inverter is set at 30.72 kHz.

Fig. 8 shows the simulation and experimental results of the output voltage and current waveforms under a step load change from no load to rated resistive load. The simulation of the PWM dc-ac converter with digital control algorithm is carried out by using the EMTP circuit simulation package [17]. It can be found that the experimental results are very

close to the simulation results. Experimental results show the output voltage transient due to a step load change can be reduced to 10% within 0.6 ms.

Fig. 9 shows the experimental steady-state responses of output voltage and current waveforms. The corresponding power spectrum of each voltage waveform are also depicted in the same figure. The THD of voltage waveform was measured by a dynamic signal analyzer (HP3562A). Since only the harmonics of 60 Hz are concerned here, a frequency span of 5 kHz was set during measurement. The harmonics of sampling and switching frequencies were ignored in our application due to their little relevance to the quality of output voltage. The definition of THD is defined as

$$\text{THD} = \frac{\sqrt{\sum_{i \neq 1} v_i^2}}{v_1} \quad (33)$$

where v_i represents the i th harmonics inside the measured frequency span. The crest factor is defined as the ratio of the peak value to the rms value of a periodic waveform. For UPS applications, the output voltage is required to have a THD below 5% under rated rectifier load with a current crest factor of 3. The THD in Fig. 9(c) is -30 dB which is about 3.16%. These results show that the proposed digital control scheme can also satisfy the required performance specifications which conventionally use analog control technique.

V. CONCLUSION

In this paper, a single-chip DSP-based (TMS320C14) fully digitally controlled PWM dc-to-ac converter has been implemented to verify the proposed multiloop digital control scheme. The output voltage error for a step-rated load change can be reduced below 10% within 5 sampling intervals when operating at 110V, 15A, and 60 Hz. THD below 5% of a rated rectifier load at crest factor of 3 can be achieved. The constructed DSP-based PWM dc-to-ac

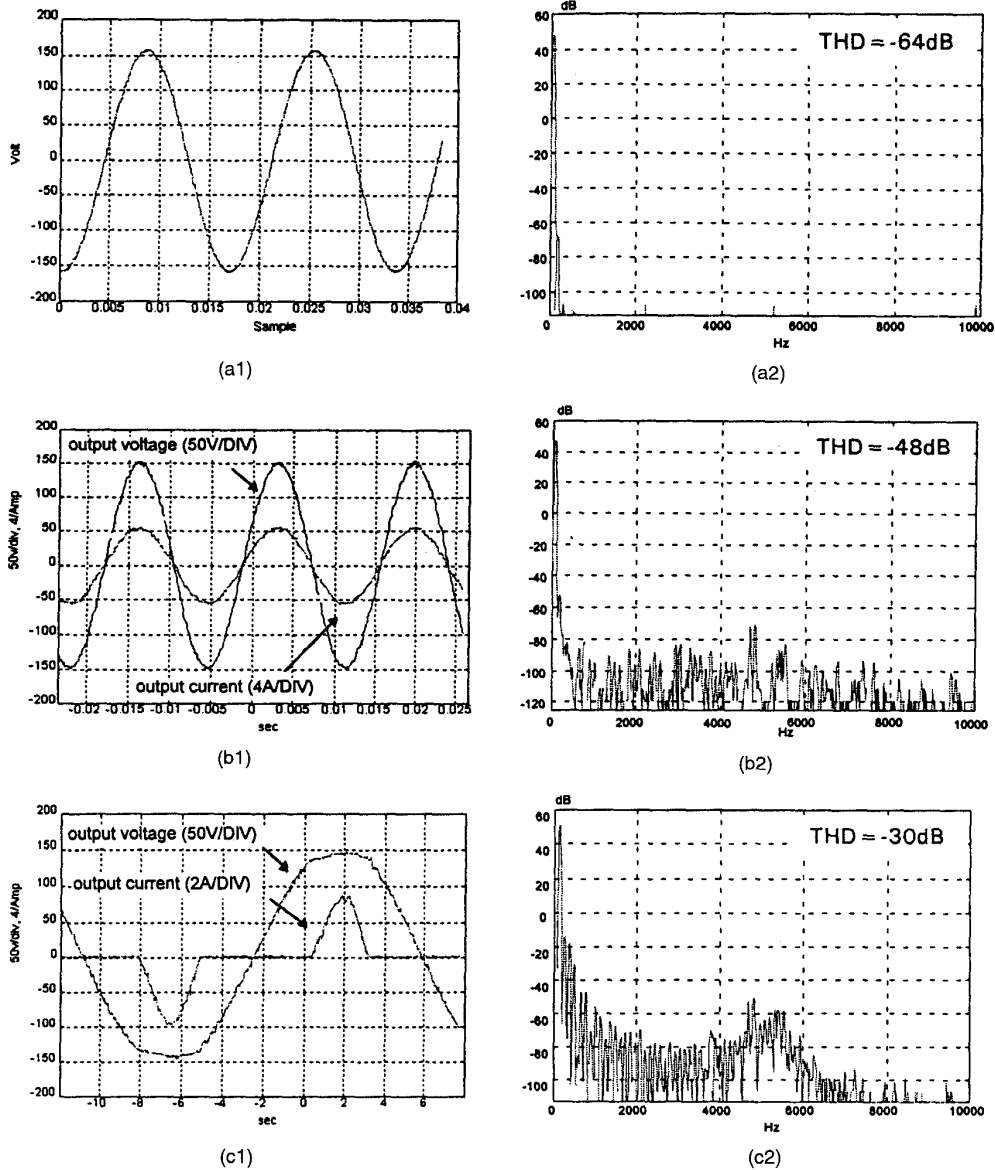


Fig. 9. Experimental steady-state output voltage and current waveforms and output voltage spectrum under (a) no-load, (b) rated resistive load, and (c) rated rectifier load with crest factor of 3.

converter system can achieve fast dynamic response and with low THD for rectifier-type loads.

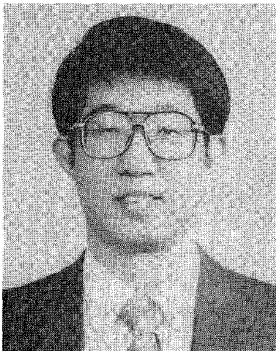
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