Effects of $CoSi_2$ on p^+ Polysilicon Gates Fabricated by BF_2^+ Implantation into CoSi/Amorphous Si Bilayers

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ABSTRACT

The integrity of thin gate oxide structures fabricated by implanting BF_2^+ ions into bilayered CoSi/amorphous silicon films and subsequent annealing has been studied as a function of cobalt silicide thickness and implantation energy. Significant degradation of gate oxide integrity and flatband voltage shifts were found with increasing cobalt silicide thickness and annealing temperature. It is shown that although thinner cobalt silicide can result in excellent gate dielectric integrity it also leads to worse thermal stability at a high annealing temperature. Moreover, shallower implantation depth and lower annealing temperature can reduce the boron penetration, but depletion effects in polycrystalline silicon gates are caused accordingly. Hence, appropriate process conditions, involving trade-offs among $CoSi_2$ thickness, implantation energy and annealing temperature, must be used to optimize the device performance while retaining the thin dielectric reliability.

Introduction

Surface channel p-type metal-oxide-semiconductor field-effect transistors (p-MOSFETs) with p^+ polycrystalline-silicon (poly-Si) gates have been investigated[1] in place of the buried-channel devices with n^+ poly-Si gates, due to superior short-channel behavior, better turn-off characteristics, lower threshold voltage operation, much less sensitivity to process tolerances,[2] and improved hot-carrier reliability[3] in the deep submicron regime. However, it has been reported that boron impurity from the B^+-doped poly-Si gate could readily diffuse through the gate oxide during high-temperature anneals.[4-7] This boron penetration effect can result in flatband voltage (V_{FB}) shift, increase of subthreshold swing and leakage current, and deterioration of gate oxide quality. On the other hand, metal silicides have been used to lower the contact resistance and sheet resistances of source/drain and gate electrodes as well as interconnections.[8-10] Cobalt disilicide ($CoSi_2$) is one of the most promising materials in the deep-submicron regimes because of its low bulk resistivity (about 18 $\mu\Omega$ cm) and good thermal stability at high temperatures. Hence $CoSi_2$ has received much attention in the self-aligned silicide (salicide) technology of ultralarge scale integrated (ULSI) devices.[11-13] In addition, the techniques which implant dopant through thin metal or metal silicide films on Si substrates have been shown to be capable of forming ultrashallow junctions.[14-17]

However, the dielectric strength of thin gate oxides beneath cobalt polycide gate electrodes is an important issue which has not been extensively investigated. In this paper, the reliability of thin gate oxides fabricated by implanting BF_2^+ ions into bilayered CoSi/amorphous silicon films has been studied. Various process conditions are examined, including the cobalt silicide thickness, the implantation conditions, and the annealing cycles.

Experimental

(100) oriented, 3-5 Ω cm, phosphorus-doped n-type Si wafers were used. Field oxides 450 nm thick were thermally grown for patterning the active regions of metal-oxide-semiconductor (MOS) capacitors. After the pattering, thin gate oxides ~8 nm thick were thermally grown at 900°C in a dry O_2 ambient. Immediately, undoped a-Si films of about 115, 131, and 146 nm thickness were, respectively, deposited onto the samples by using the low pressure chemical vapor deposition (LPCVD) system at 550°C. The gate electrode was then patterned for utilization of selective etching. Subsequently, thin Co films of about 4.5, 9, and 13.5 nm thickness were deposited onto the samples with undoped a-Si films of 115, 131, and 146 nm thickness, correspondingly, by an E-beam evaporation system. As a result, after the whole silicidation process, the $CoSi_2$ films of about 15, 30, and 45 nm thickness were formed, respectively. Moreover, the residual poly-Si thickness was about 100 nm for all the samples. To serve as a passivation layer for silicidation annealing, the samples were further covered with thin Mo films of about 6, 12, and 18 nm thickness, correspondingly. The first step anneal was performed at 450°C for 60 s by rapid thermal annealing (RTA). After the first step anneal, the undoped a-Si layer would still be amorphous, which can effectively reduce the diffusion of dopant impurities.[18] Then, Mo layers were removed in a 5:1:1 mixture of H_2O:H_2O_2:NH_4OH at 55-60°C. Subsequently, all the samples with bilayered CoSi/a-Si films were BF_2^+ implanted with various energies to a dose of 5×10^{15} cm^{-2}, as listed in Table I. The unreacted Co layers on field oxide were selectively removed in a 6:1:1 mixture of H_2O:H_2O_2:HCl at 55-60°C. The second step silicidation anneal was performed at temperatures ranging from 600 to 900°C for 30 min by furnace annealing. The resultant integrity of gate oxides was characterized by current-voltage (I-V) and capacitance-voltage (C-V) measurements. the semiconductor parameter analyzers HP 4156, the Keithley 595 quasi-static C-V meter, and the Keithley 590 C-V analyzer were conducted, respectively. In addition, the secondary ion mass spectroscopy (SIMS) was also used to investigate the dopant distributions after annealing.

Results and Discussion

In this study, the transport of ions in matter (TRIM) simulation program was used to predict the distribution of as-implanted dopants in the bilayered CoSi/a-Si films. In order to investigate the effects of $CoSi_2$ thickness on thin gate oxide reliability, various implantation energies were chosen to adapt the projected range (Rp) near predicted $CoSi_2$/poly-Si interface or deeply into poly-Si gates, respectively, for the specimens with different $CoSi_2$ thick-

Table I. The process conditions for $CoSi_2$ thickness and implant energy.

Implantation peak	$CoSi_2$ thickness		
	15 nm	30 nm	45 nm
Near $CoSi_2$/poly-Si interface (keV)	20	40	60
Deeply into poly-Si film (keV)	40	60	80

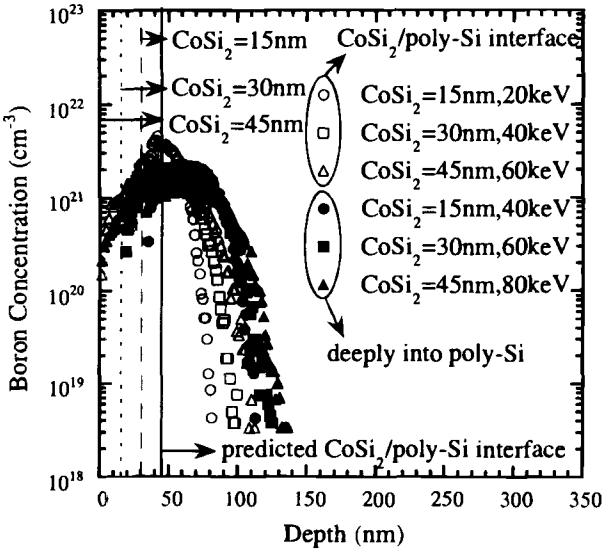

Fig. 1. The as-implanted dopant profiles simulated by TRIM program for the samples with various $CoSi_2$ thicknesses and implant energies, correspondingly.

nesses. The results are show in Fig. 1. The dopant penetration into the poly-Si film would be caused by using the deeper implantation, with a penetration depth of about 10 nm below the $CoSi_2$/poly-Si interface.

Cobalt silicides are often used as a contact material to reduce the resistance and thus increase the device speed. Figure 2 shows the sheet resistance (*Rs*) value as a function of annealing temperature for the samples with different $CoSi_2$ thicknesses and implant energies, respectively. The thicknesses of $CoSi_2$ films were 15, 30, and 45 nm, respectively. After the process of BF_2^+ implantation, the sheet resistance tracks the radiation damages caused by ion implantation. As illustrated in Fig. 2, for all specimens, *Rs* was slightly reduced with increasing the second step annealing temperature until 800°C, due to the recovery of implantation damages and/or the grain growth of formed cobalt silicide. The sheet resistance of thicker $CoSi_2$ films can remain stable even after an annealing at 900°C. However, for the 15 nm thick $CoSi_2$ films, the sheet resistance increases tremendously after an annealing at 900°C regardless of the implantation conditions. This result was attributable to the formation of island structure of the cobalt silicide at such a high-temperature annealing.

In this study, the CoSi film is used an an implantation barrier to minimize the dopant impurity diffusion by reducing the projectible range and implant-induced defects. Figure 3 indicates the dependences of flatband voltage (V_{FB}) on annealing temperature for the specimens implanted near the $CoSi_2$/poly-Si interface or deeper, with the $CoSi_2$ thickness as a parameters. The thicknesses of $CoSi_2$ films were 15, 30, and 45 nm, respectively. While implanting impurities near the $CoSi_2$/poly-Si interface, smaller V_{FB} shifts were found for the samples with thinner $CoSi_2$ film thickness, and the V_{FB} shift would lower as the annealing temperature was decreased. As for the specimens implanted deeply into poly-Si films, the samples with thicker $CoSi_2$ layers (45 nm) exhibit much larger V_{FB} shifts than those with thinner $CoSi_2$ films (15 and 30 nm), especially at the annealing temperature of 900°C. This result reflects the severe boron penetration through thin gate oxides, attributable to the fact that the higher implantation energy could result in the distribution of as-implanted dopants deeply and widely into the poly-Si gates. Hence, thinner $CoSi_2$ layers with BF_2^+ implantation near the $CoSi_2$/poly-Si interface sustain smaller V_{FB} shift as the annealing temperature is decreased. However, shallower implant projected range or lower annealing temperature could cause the depletion effect of poly-Si gates.

Figures 4a and b show the dependences of normalized high frequency C-V curves on annealing temperature for the samples with BF_2^+ implantation near the $CoSi_2$/poly-Si interface or deeper, correspondingly. The cobalt silicide thickness is 30 nm. The gate depletion effect was observed at annealing temperatures of 600 and 700°C, as shown in Fig. 4a, attributable to insufficient thermal budget. The dopant concentration could be insufficient, since the furnace annealing treatment at lower temperature would lead to less dopant drive-in from the $CoSi_2$ layer during annealing. However, the dopant drive-in efficiency has been improved at annealing temperatures above 800°C. On the other hand, as shown in Fig. 4b, higher implantation energy can also improve the gate depletion phenomenon at annealing temperature of 700°C, but which causes much more positive shifts of C-V curves at higher annealing temperature, indicating the generation of a large amount of electron traps. Moreover, the samples with 15 nm thick $CoSi_2$ films also showed similar results of gate depletion effects at lower annealing temperatures or implant energies, in comparison with those with 30 nm thick $CoSi_2$ films. In order to eliminate the gate deple-

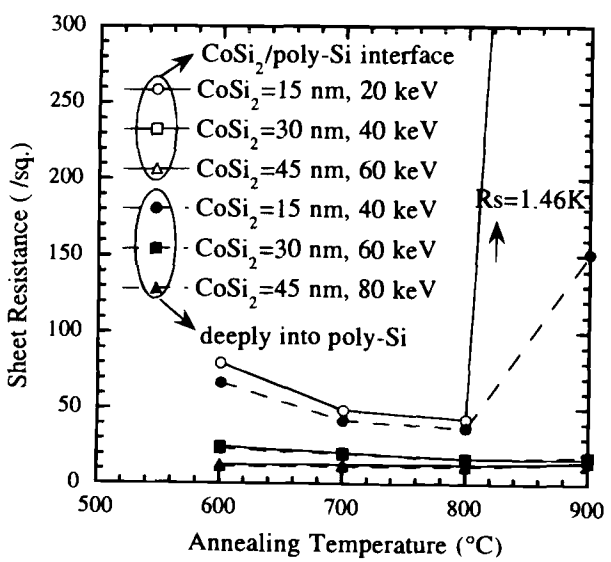

Fig. 2. Dependence of sheet resistance on function of annealing temperature for the samples with various $CoSi_2$ thickness and implantation near the $CoSi_2$/poly-Si interface or deeper, correspondingly.

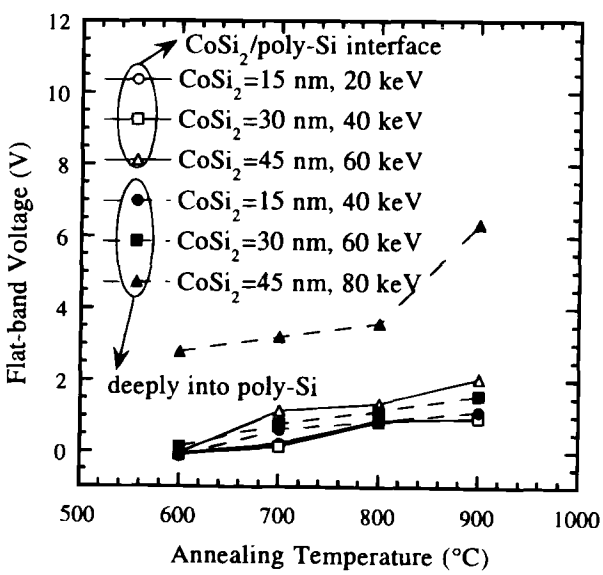

Fig. 3. Dependences of flat-band voltage on function of annealing temperature for the samples with various $CoSi_2$ thickness and implantation near the $CoSi_2$/poly-Si interface or deeper, correspondingly.

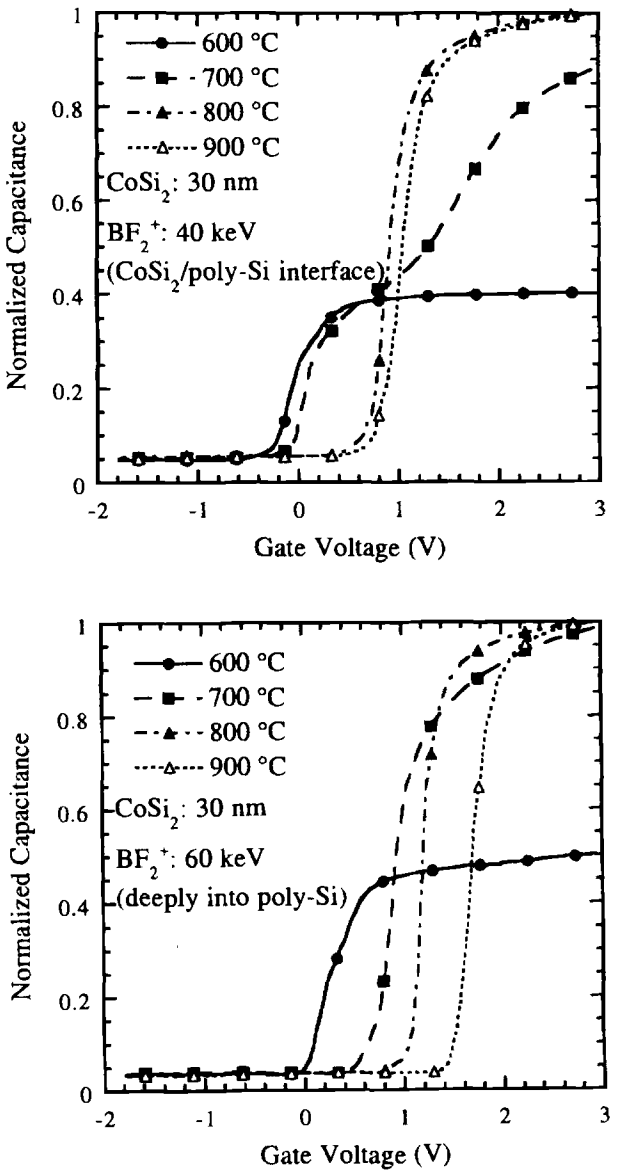

Fig. 4. The high-frequency C-V curves for the specimens with BF_2^+ implantation (a) near the $CoSi_2$/poly-Si interface or (b) deeply into poly-Si gates, annealed from 600 to 900°C for 30 min, respectively. The $CoSi_2$ thickness is 30 nm.

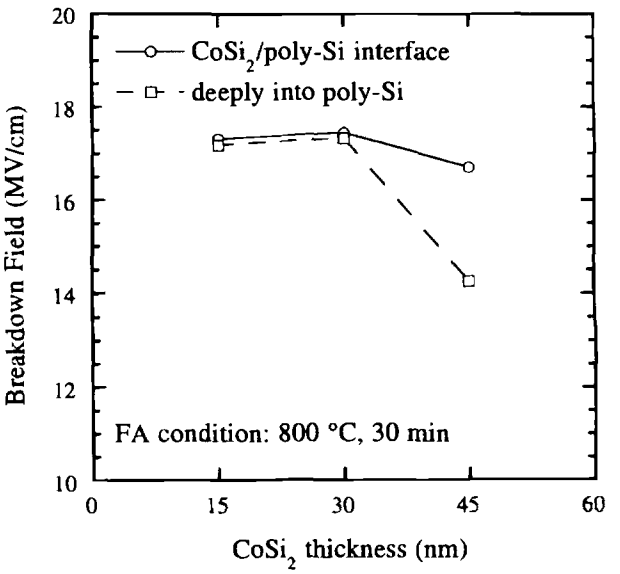

Fig. 5. Breakdown field as a function of $CoSi_2$ thicknesses for the samples with implantation near the $CoSi_2$/poly-Si interface or deeper, respectively, and annealing at 900°C for 30 min.

tion effects, an appropriate choice for implantation conditions and thermal cycles is necessary for such a promising process. For an example, the 30 nm thick $CoSi_2$ films with BF_2^+ implantation near the $CoSi_2$/poly-Si interface and annealing at 800°C can be employed.

The effects of $CoSi_2$ thickness on the gate oxide reliability are investigated. Figures 5 and 6 indicate the time zero dielectric breakdown (TZDB) results as a function of $CoSi_2$ thicknesses for the samples with BF_2^+ implantation near the $CoSi_2$/poly-Si interface or deeper and then annealed at 800 and 900°C, correspondingly. At least 20 capacitors for each sample were taken to attain the average values of breakdown fields (E_{bd}) and charges to breakdown (Q_{bd}). For the samples with implantation near the $CoSi_2$/poly-Si interface, slight degradation of E_{bd} values was found with increasing $CoSi_2$ thickness at annealing temperatures of 800 and 900°C. On the other hand, for the specimens implanted deeply into poly-Si gates, the E_{bd} values are severely degraded as the $CoSi_2$ film thickness is increased, especially for thicker $CoSi_2$ films (45 nm). The samples with thicker $CoSi_2$ would require higher implant energy to keep the same peak position of implanted impurities, thus leading to a wider as-implanted dopant profile and readily resulting in a large amount of boron impurities which diffuse through gate oxides at annealing temperatures of 800 and 900°C. Even for the samples with BF_2^+ implantation near the $CoSi_2$/poly-Si interface, the specimens with thicker $CoSi_2$ film (45 nm) still show the boron penetration effects of annealing temperatures of 800 and 900°C. However, the specimens with $CoSi_2$ layers 30 nm thick just manifest minute E_{bd} degradation even at higher implant energy and higher annealing temperature, and which almost show no deterioration at annealing temperature of 800°C. As results, excellent thin gate oxides can be achieved by the samples with thinner $CoSi_2$ films (15 and 30 nm) annealed at 800°C, regardless of the implant conditions, as well as by the samples with 30 nm thick $CoSi_2$ films and implantation near the $CoSi_2$/poly-Si interface annealed at 900°C. Furthermore, Fig. 7 indicates the Wiebull plot of charge to breakdown (Q_{bd}) for the samples with various $CoSi_2$ thicknesses and implantation near the $CoSi_2$/poly-Si interface or deeper, respectively. The annealing condition is at 800°C for 30 min. A stress current density of 100 mA/cm^2 was used, with the stress area of 1.767×10^{-4} cm^2. The sam-

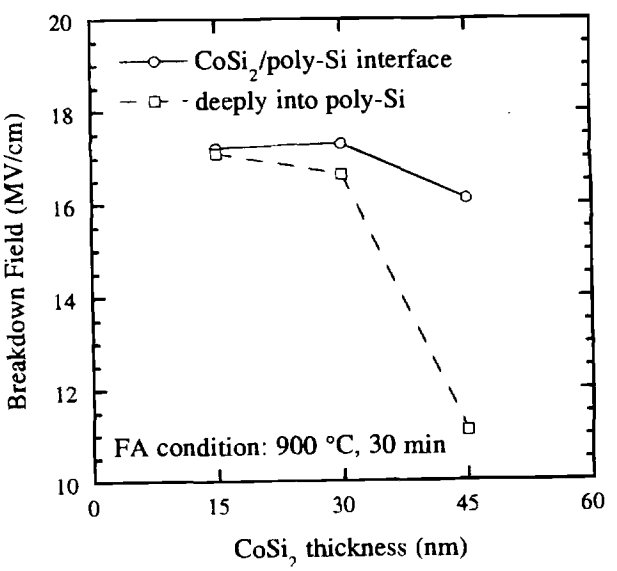

Fig. 6. Breakdown field as a function of $CoSi_2$ thicknesses for the samples with implantation near the $CoSi_2$/poly-Si interface or deeper, respectively, and annealing at 800°C for 30 min.

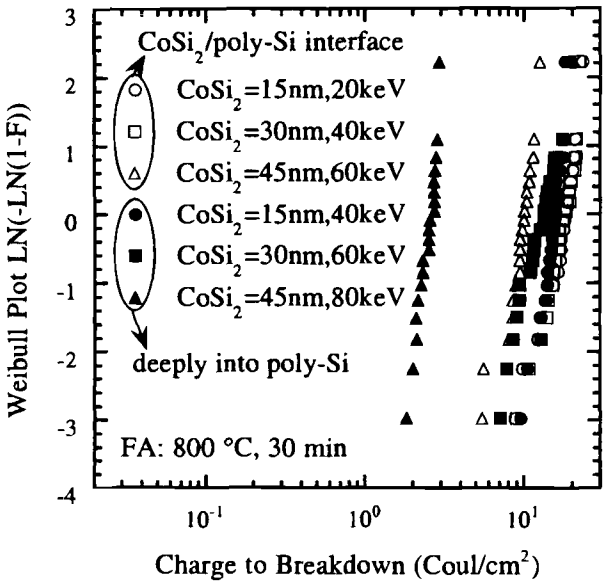

Fig. 7. The Weibull plot of charge to breakdown for the samples with various $CoSi_2$ thickness and implantation near the $CoSi_2$/poly-Si interface or deeper, correspondingly, annealed at 800°C for 30 min.

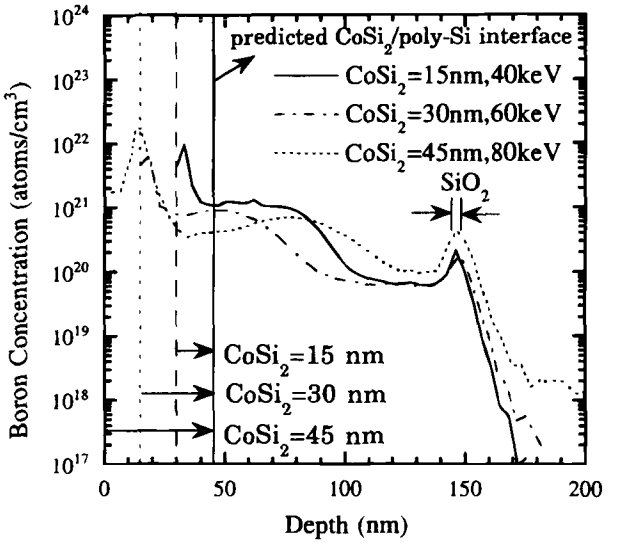

Fig. 9. Boron depth profiles measured by SIMS for the samples with implantation deeply into poly-Si gates and annealing at 800°C for 30 min.

ples exhibit negative shifts of Q_{bd} distribution as the $CoSi_2$ thickness is increased. Slight variations of Q_{bd} distribution were observe for the samples with thinner $CoSi_2$ layers (15 and 30 nm), no matter what implant conditions. However, the samples with thicker $CoSi_2$ film (45 nm) exhibit significantly deterioration of the gate oxide quality, especially for higher implant energy as 80 keV. The degraded Q_{bd} values are further identified to be consistent with the results of E_{bd} characteristics shown in Fig. 5. In addition, from the curves of gate voltage shifts against stress time for the samples annealed at 800°C, shown in Fig. 8, the samples with thinner $CoSi_2$ film thickness lead to much lower electron-trapping rate of gate oxides, regardless of the implant conditions. The samples with thicker $CoSi_2$ films as 45 nm in thickness still show an extremely large electron-trapping rate at annealing temperature of 800°C.

Figure 9 shows the measured SIMS depth profiles of boron concentration in the $CoSi_2$/poly-Si/SiO_2/Si substrate structure. The samples were BF_2^+-implanted deeply into the poly-Si gates, followed by furnace annealing at 800°C for 30 min. As can be seen, the samples with thinner $CoSi_2$ films (15 and 30 nm) exhibit much less boron penetration into Si substrates. However, a large amount of boron impurities are found to be diffused into Si substrates for the samples with 45 nm thick $CoSi_2$ films, leading to poor E_{bd} and Q_{bd} characteristics as shown in Fig. 5 and 7.

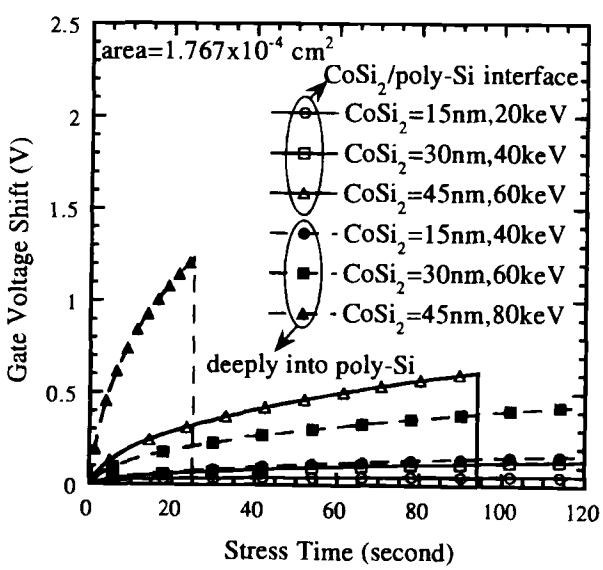

Fig. 8. Comparisons of the gate voltage shift for the samples with various $CoSi_2$ thickness and implantation near the $CoSi_2$/poly-Si interface or deeper, respectively, annealed at 800°C for 30 min. The stress current density is 100 mA/cm².

Conclusions

Significant degradation of gate oxide quality and flat-band voltage shifts were found for the samples with thicker $CoSi_2$ films and annealed at higher temperatures, attributable to the severe boron penetration. Although the samples with thinner $CoSi_2$ films (15 nm) can result in excellent integrity of gate dielectrics, poor thermal stability at an annealing temperature of 900°C is caused. Moreover, the insufficient thermal budget and the lower implantation energy would result in the depletion effect of poly-Si gates. Hence, a proper choice of process conditions is necessary to attain better cobalt silicide stability as well as thin gate dielectric reliability. For examples, the $CoSi_2$ films, 15 and 30 nm thick, with implantation near the $CoSi_2$/poly-Si interface and annealing at 800°C, or, with deeper implantation into poly-Si gates and annealing at 700 and 800°C can be employed. In addition, the 45 nm thick $CoSi_2$ films with implantation near the $CoSi_2$/poly-Si interface and annealing at 700°C can be used to lead to excellent gate oxide reliability. Those conditions are listed in Table II.

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Table II. The proposed process conditions for this scheme.

Implantation peak	$CoSi_2$ thickness		
	15 nm	30 nm	45 nm
Near $CoSi_2$/poly-Si interface (°C)	800	800, 900	700
Deeply into poly-Si gate (°C)	700, 800	700, 800	—

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Optimization of the Growth of CdTe Thin Films Formed by Electrochemical Atomic Layer Epitaxy in an Automated Deposition System

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ABSTRACT

This paper describes the deposition of CdTe thin films by electrochemical atomic layer epitaxy (ALE). ALE involves the formation of compounds an atomic layer at a time, using surface-limited reactions. That is, atomic layers of the elements making up a compound are deposited in a cycle, where each cycle produces a monolayer of the compound. In electrochemical ALE, the surface-limited reactions that produce the atomic layers are referred to as underpotential deposition (UPD). This article describes the dependence of the deposit structure, morphology and composition on a number of the steps in the deposition cycle. Separate optimized solutions and potentials are used to deposit each of the elements. Specifically, a variety of deposition and stripping potentials have been examined, resulting in a broad range of deposit compositions and morphologies. The dependence of the deposits on the potential used to form Cd atomic layers is a good example. If the potential was too positive, no CdTe deposits were formed, as no Cd was deposited, so there was nothing for Te UPD to form on. If the potentials were too far negative, bulk Cd began to deposit, and Cd-rich three-dimensional growth predominated. There was a 0.2 V plateau for the Cd deposition potential where stoichiometric films were deposited; however, the highest quality films were formed within a 0.1 V wide plateau, between −0.55 and −0.65 V. The optimal Te deposition potentials appear to be between −0.7 and −0.8 V. At more positive potentials, the Cd atomic-layers stripped, while at more negative potentials Te dendrites were formed and the surface roughened badly. Potentials of −1.2 V and below should be used for the Te stripping step, in order to remove all excess Te, above an atomic layer. If more positive potentials were used, some excess Te remained and three-dimensional growth resulted. Te stripping should be performed for at least 20 s to completely remove the excess Te. Neither substrate orientation, nor annealing to 300°C had much effect on the quality of the deposited films.

Introduction

Compound semiconductors are a critical constituent of optoelectronic devices.[1,2] Nanostructuring is becoming an increasingly important feature of such devices; solid-state blue lasers are a good example.[3] For most thin-film deposition methodologies, sufficient control over nanostructural dimensions is problematic, while atomic level control is becoming very desirable. To that end, atomic layer epitaxy (ALE) is being developed as a modification of vacuum-based techniques such as molecular beam epitaxy (MBE) and chemical vapor deposition (CVD).[4-7] ALE breaks up the deposition of each monolayer of a compound into a series of steps. The steps consist of the application of surface-limited reactions, where each reaction results in the formation of an atomic layer of one of the elements making up the compound. The series of steps can be used in a cycle to form a monolayer of the compound: this sequence is repeated the desired number of times to form a given thickness of deposit. Each step can be a point of control for the deposition process.

Work in this group has focused on developing an electrochemical analog of ALE.[8-15] Electrochemical techniques are desirable as they allow uniform deposition on irregular surfaces, at low temperatures with excellent selectivity and process control.[8,16-18] In addition, electrochemical techniques generally have simplified waste streams, as less dangerous or toxic materials are used relative to the precursors in many vacuum-based techniques. Electrochemical ALE (ECALE) makes use of well-known electrochemical sur-

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