# Field Inversion Generated in the CMOS Double-Metal Process Due to PETEOS and SOG Interactions

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***Abstract*—Severe field inversion has been observed in the circuits fabricated by the CMOS double metal process using PETEOS/inorganic SOG/PEOX as the inter-metal dielectrics and PEOX/PECVD nitride as the passivation layer. We have performed detailed studies to conclude that the field inversion is caused by the interaction between PETEOS and non-carbon-based SOG, triggered by the $H^+$ released from PECVD nitride during the sintering. No field inversion is observed when PEOX/inorganic SOG/PEOX is used as the inter-metal dielectrics. The effect of field inversion on the circuit yield is also discussed.**

## I. Introduction

SPIN-ON GLASS (SOG) sandwiched by either PECVD tetraethylorthosilicate (PETEOS) or PECVD silane-based oxide (PEOX) has been widely used as the inter-metal dielectrics in the CMOS double-metal process. The dielectric structure provides good planarization and dielectric isolation. However, it has been reported that carbon-based spin-on glass causes field inversion in CMOS circuits under certain process conditions [1]. The inorganic spin-on glass has been shown to be free of the field inversion problem [1]. In this paper, we report severe field inversion when the inorganic spin-on glass is used in the presence of PETEOS. We have performed systematic experiments to identify causes of the field inversion. The impact of field inversion on the circuit yield are also discussed.

## II. Experimental

The devices were fabricated using the conventional 1.0-$\mu$m CMOS process. The field oxide thickness was 7500 Å as-grown, and 4500 Å on finished wafers. The field isolation was enhanced by a $p^-$ field implant with a boron dose of $9 \times 10^{13}/cm^2$, and 150-keV energy. For comparison, four types of inter-metal dielectric schemes were fabricated, namely, PETEOS/SOG/PEOX, PEOX/SOG/PEOX, 10 000-Å PETEOS, and 10 000-Å PEOX. Here SOG material used is non-carbon-based. The bottom PETEOS or PEOX film was 3000 Å thick, while the top PEOX film was 5000 Å thick for the first two types of inter-metal dielectric schemes. The SOG was double-coated with total thickness of 2000 Å and was cured at 420°C. The passivation was formed by 5000-Å-thick PEOX deposition, followed by 7000-Å-thick PECVD nitride deposition. Sintering at 410°C in the 80% $N_2$/20% $H_2$ ambient was performed after the passivation via etch. For comparison, some wafers were sintered before PECVD nitride deposition.

A special field device, as shown in Fig. 1(a), was designed to evaluate the integrity of the inter-metal dielectrics. This test structure was similar to the one used in [1]. The source and drain of the field device formed a comb structure with polysilicon running perpendicular to the source and drain. Metal lines were running on the top of source and drain and contacting the diffusion areas through contact vias. This test structure actually consisted of two parallel field devices: one was along the cross section of line $AA'$, which has a polysilicon gate but no $n^+$ implants in the source and drain regions; the other was along the cross section of line $BB'$, which has $n^+$ implants in the source and drain regions, but no polysilicon gate. The field structure along cross section of line $BB'$ was very sensitive in detecting the amount of charges in the dielectric films deposited during backend processes. The channel length of the field device was 2.4 $\mu$m, and the width was 1200 $\mu$m. For comparison, a regular field device, as shown in Fig. 1(b), with 2.4-$\mu$m channel length and 20 $\mu$m channel width was also designed. In our experiments, we measured the threshold voltages of these two types of field devices to examine the isolation integrity of CMOS process.

## III. Results and Discussions

### A. General Observations

It has been known that the backend process can damage the MOS devices [1]–[4]. Many precautions are being taken to prevent damage, and many extra processes are

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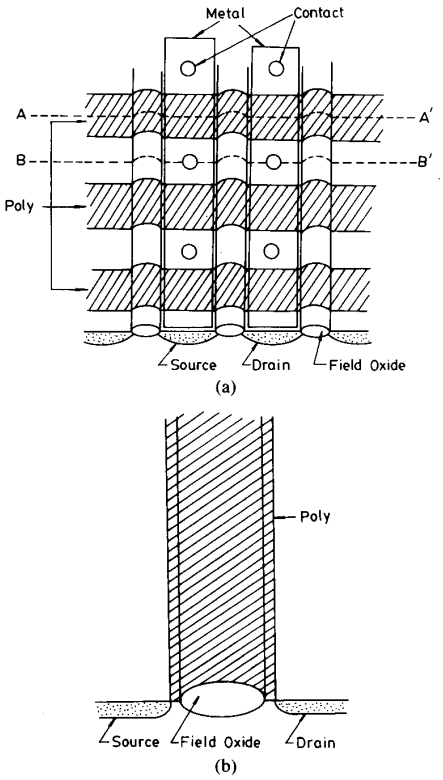


Fig. 1. (a) A special field device test structure consisting of two parallel field devices: one along the cross section of line $AA'$, which has a polysilicon gate but no $n^+$ implants in the source and drain regions; the other along the cross section of line $BB'$, which has $n^+$ implants in the source and drain regions, but no polysilicon gate. A regular field device is shown in (b).

used to anneal the damage in modern VLSI technologies. During the development of our 1.0-$\mu$m CMOS double-metal process, we have initially used silicate-based SOG sandwiched with PETEOS (i.e., PETEOS/SOG/PETEOS) as the inter-metal dielectrics. Very low threshold ($\sim$0 V) of n-type special field devices (as depicted in Fig. 1(a)) was routinely found. We have tried to replace the top PETEOS layer by PEOX (i.e., PETEOS/SOG/PEOX), and found the threshold voltage of n-type special field devices increases, though still low ($<$8 V). However, the p-type special field devices, the n- and p-type regular field devices (as depicted in Fig. 1(b)), and the n- and p-type thin-oxide devices behave normally, even when the n-type special field devices have field inversion problems. The field inversion can be suppressed by applying a back-gate bias. These observations are similar to those reported in [1]. The channel inversion is believed to be due to changes in the dielectric films above the field oxide where polysilicon is not present. The charging effects induced during the backend process can be blocked by the presence of polysilicon or metal-1 due to the shielding phenomena. This explains why normal thin oxide devices as well as regular field oxide devices can be obtained, even when there are charges generated during the backend process.

### B. Systematic Studies

In order to identify causes of the charging effects in dielectric films, we have performed the following systematic experiments. Fig. 2(a) shows the thresholds of n-type special field devices for 12 wafers with four splits of different intermetal dielectric schemes (i.e., 3 wafers in each split). From now on, the field threshold voltages indicate the threshold voltage of n-type special field devices, unless it is particularly specified. The wafers in the group using PETEOS/SOG/PEOX show field inversion, while wafers in groups using PEOX/SOG/PEOX, PEOX, and PETEOS do not show the field inversion problem. We also experience significant fluctuations in the field threshold voltage when there is field inversion. Our experiments confirm the reported results that inorganic SOG does not cause field inversion when sandwiched in PEOX material [1]. The field inversion occurs only when inorganic SOG is interfacing with PETEOS. The effect of carbon on the field inversion problem has been previously addressed by comparing the carbon-based and non-carbon-based SOG [1]. Since PETEOS is a carbon-based material, it may supply carbon to silicate-based SOG, and induce the reaction as described in [1].

The impacts of the field inversion on the chip yield for a particular ASIC chip design (a microcontroller chip, chip size $\sim$100 kmil$^2$) fabricated on the wafers used for Fig. 2(a) are shown in Fig. 2(b). This microcontroller chip design is so sensitive to field inversion that the yield is almost zero for wafers with PETEOS/SOG/PEOX as intermetal dielectrics. For other typical ASIC chip products, we have usually observed a yield loss between 10 and 20% due to field inversion based on our other experiments. In Fig. 2(b), the circuit yield for wafers using 10 000-Å PETEOS and 10 000-Å PEOX is also very low. From SEM cross sections, we found the low yield for these two cases is caused by metal opens and shorts due to lack of planarization.

To understand mechanisms of charge generation in dielectric films, we monitored the field threshold of various processing steps during the backend process, and the results are summarized in Fig. 3. For the PETEOS/SOG/PEOX inter-metal dielectric scheme, minor degradation of special field devices is shown at the measurement after the passivation via etch, and dramatic decrease in the field threshold is detected after sintering at 410°C in an 80% $N_2$/20% $H_2$ ambient. No degradation is found through the backend process for the PEOX/SOG/PEOX intermetal dielectric scheme. It has been shown that PECVD nitride can release $H^+$ during sintering [1]–[3]. The released $H^+$ diffuses into the bottom dielectric films, and triggers interaction between PETEOS and SOG. Combining experimental data in Figs. 2 and 3, we conclude that the charges are generated by the PETEOS and SOG interactions and the interaction is triggered by $H^+$ released from the PECVD nitride and diffused into the bottom films during the sintering process.

To further locate the existence of charges, we first remove the PECVD nitride film, measure the field thresh-

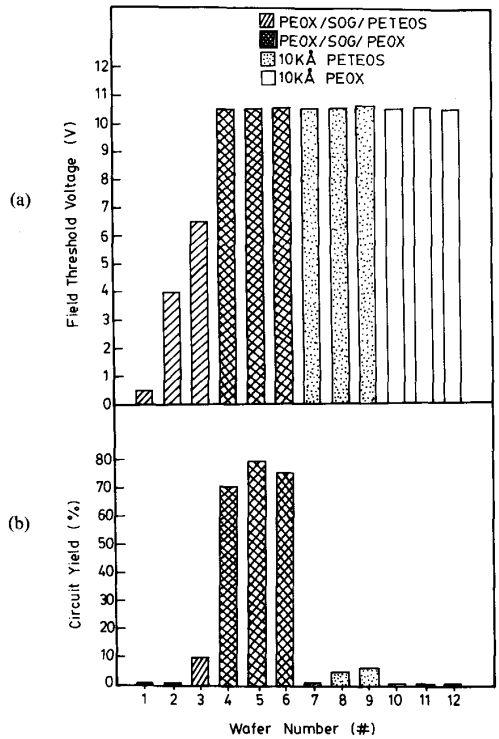


Fig. 2. (a) Field threshold voltages of field devices with four different inter-metal dielectric schemes. (b) The circuit yield of a given ASIC design fabricated on the same wafer the field threshold of which is shown in (a).

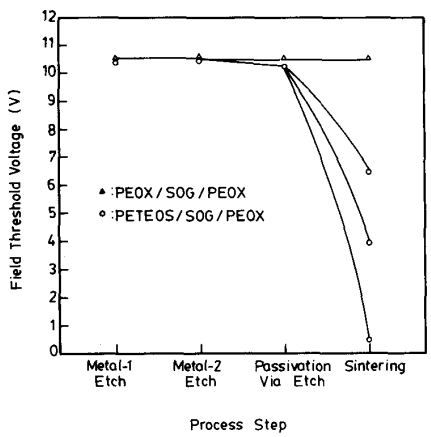


Fig. 3. Field threshold voltages measured in steps during the backend of line process for PETEOS/SOG/PEOX and PEOX/SOG/PEOX inter-metal dielectric schemes.

old, then remove the PETEOS/SOG/PEOX structure, and measure the field threshold again. Plasma dry etch is used to remove dielectric films, and sintering is performed after the films are removed to fix damage caused by plasma etch. Our experimental results show that the field threshold voltage slightly increases after PECVD nitride is removed, and the field threshold is completely recovered to the original value previously measured at metal-1 after the PETEOS/SOG/PEOX structure is removed. This experiment proves that the charges exist mainly in the PETEOS/SOG/PEOX inter-metal dielectric structure.

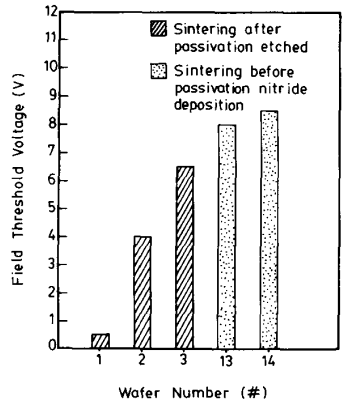


Fig. 4. Field threshold voltages for wafers with PETEOS/SOG/PEOX inter-metal dielectric schemes and with the sintering process performed after and before PECVD nitride deposition, respectively.

Since the interaction between PETEOS and SOG is triggered by the $H^+$ diffused from the top layer of PECVD nitride, we can prevent this interaction by performing the sintering process before, instead of after, the PECVD nitride deposition. By doing this, we improve the quality of underlying PEOX films to prevent the $H^+$ from diffusing down to the SOG and PETEOS films. Futhermore, the probability of $H^+$ released from PECVD nitride as well as the diffusion rate of $H^+$ are reduced by omitting the sintering temperature after the PECVD nitride deposition. Fig. 4 shows field threshold voltages for wafers subjected to the sintering process before and after the PECVD nitride deposition, respectively. Significant improvements in field threshold voltages are found when the sintering is performed before the PECVD nitride deposition. This is a typical example that process integration is as important as the individual process step in mordern VLSI techologies.

## IV. Summary

We have found severe field inversion caused by the backend process when the PETEOS/SOG/PEOX scheme is used as the inter-metal dielectrics, even if the SOG material is non-carbon-based. Systematic experiments have been conducted to identify causes of the degradation. No field inversion is found when PEOX/SOG/PEOX is used as the inter-metal dielectric. The field oxide device degrades slightly after the PECVD nitride deposition, and its field threshold voltage dramatically decreases after the sintering process. We have also performed experiments to find the location of charges. The charges are found to exist mainly in the PETEOS/SOG/PEOX inter-metal dielectric films. The field inversion problems can be improved by performing the sintering process before the deposition of PECVD nitride, instead of after. Based on our experimental results, we conclude that the field inversion is due to charges generated from the PETEOS and inorganic SOG interactions, which is possibly triggered by

$H^+$ released from PECVD nitride passivation layer during the sintering process.

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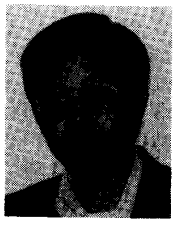

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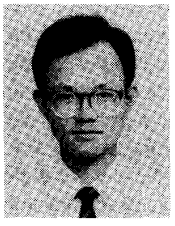

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Dr. Chang is a member of Phi Tau Phi, the American Electro-Magnetics Academy, the Chinese Institute of Electrical Engineers, the American Physical Society, and the Electrochemical Society. He has been elected an IEEE fellow for "his contribution to semiconductor devices development and to education."