Poly-Si Nanowire Nonvolatile Memory With Nanocrystal Indium–Gallium–Zinc–Oxide Charge-Trapping Layer

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***Abstract*—This letter introduces a polycrystalline silicon (poly-Si) thin-film nonvolatile memory (NVM) with a nanocrystal (NC) indium–gallium–zinc–oxide (IGZO) charge-trapping layer. Experimental results indicate that this NVM exhibits high and symmetric program/erase speeds through the Fowler–Nordheim tunneling mechanism. The memory window loss of the NVM with NC IGZO charge-trapping layer is 25% after 10^4 s at 85 °C due to deep quantum well, as well as high-density and deep trap sites in NC IGZO charge-trapping layer. Accordingly, a poly-Si thin-film transistor with NC IGZO charge-trapping layer is promising for NVM applications.**

***Index Terms*—Indium gallium zinc oxide (IGZO), nanocrystal (NC), nonvolatile memory (NVM), thin-film transistor (TFT).**

I. Introduction

As THE demand for information storage increases, the memory density required for electronic devices also increases. Flash memory is one kind of nonvolatile memory (NVM) that does not require a power supply to sustain information storage; it is also the essential component of portable electronics. Flash memory has been continued to scale for high-density applications. However, following Moore's law is becoming increasingly difficult because of process and device limitations. Hence, 3-D multilayer-stack memory based on polycrystalline silicon (poly-Si) thin-film transistors (TFTs) has been proposed to solve these problems [1]–[5].

Poly-Si TFTs also have attracted substantial attention because of their wide range of applications in active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light-emitting displays (AMOLEDs) [5], [6]. The primary appeal of the poly-Si TFTs in AMLCDs lies in greatly improved carrier mobility in the transistor channel, the ability to integrate pixel switching elements, and the ability to integrate the panel array, the peripheral driving circuit, and other functional components on a single glass substrate. Such poly-Si TFTs are thus ushering in the era of system-on-panel (SOP) technology [7]–[9]. Moreover, embedded high-density NVM is required for storing image and signal to realize SOP.

Recently, a new metal–oxide–semiconductor material, i.e., amorphous indium–gallium–zinc–oxide (IGZO) (a-IGZO), has been studied extensively because this thin film has uniform carrier mobility, flexibility, transparency, and low-temperature process. These characteristics make it become an outstanding candidate for numerous TFT applications, including flexible electronics, AMLCD, and AMOLED [10], [11]. In addition, the a-IGZO thin film as active layer and charge-trapping layer in NVMs has been explored to elucidate the potential usage in advanced applications [12]–[14]. However, these NVMs show poor Fowler–Nordheim (F–N) erasing characteristics. For the embedded NVM of SOP and 3-D high-density NAND Flash memory, this large bandgap material, IGZO, as the charge-trapping layer warrants further investigation.

Accordingly, in this work, poly-Si thin-film NVMs with the nanocrystal (NC) IGZO charge-trapping layer are fabricated. The transfer characteristics, program/erase (P/E) characteristics, and the data retention of the memory with the NC IGZO charge-trapping layer are addressed.

II. Device Structure and Fabricaion

The trigate poly-Si TFT NVM with an NC IGZO charge-trapping layer was fabricated by initially growing a 400-nm-thick silicon dioxide layer. A 50-nm-thick undoped amorphous-Si layer was deposited by low-pressure chemical-vapor deposition (LPCVD) at 550 °C and solid phase crystallized at 600 °C for 24 h in nitrogen ambient. The patterns of the active layer were defined as ten strips of multiple 45-nm nanowires (NWs). An 8.5-nm-thick thermal SiO_2 layer was grown as the tunneling oxide. Above the thermal SiO_2, a 10-nm-thick a-IGZO was deposited through dc sputtering in Ar/O_2 mixed gas at room temperature, and a 16.5-nm-thick SiO_2 was deposited as the blocking oxide by PECVD. The X-ray photoelectron spectroscopy analysis shows that the atomic percentages of In, Ga, Zn, and O are 19.48%, 8.48%, 22.62%, and 49.42%, respectively. An 80-nm-thick poly-Si layer was deposited as the gate electrode. Then, the self-aligned source, drain, and gate regions were implanted with 23-keV phosphorous ions at a dose of 5×10^{15} cm^{-2} and activated by rapid thermal annealing at 900 °C for 60 s in nitrogen

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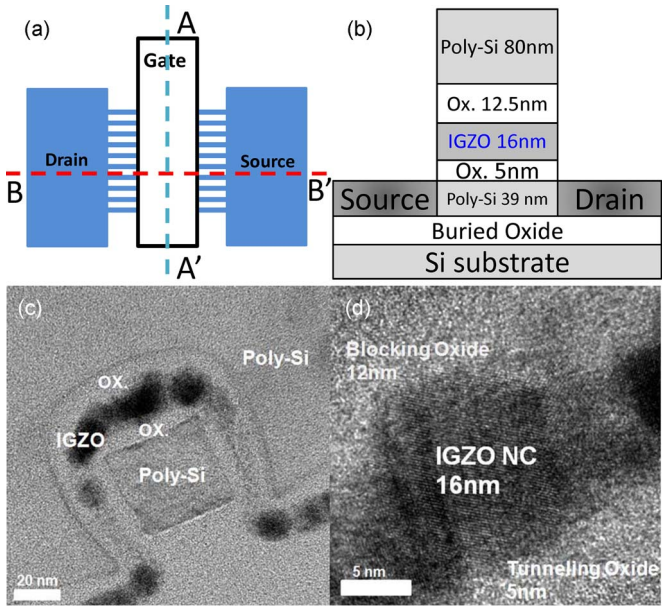

Fig. 1. (a) Top view of pi-gate TFT NVMs. (b) Cross-sectional view corresponding to (a) in the BB' direction. (c) TEM image of trigate structure with $NWs = 45$ nm and $SiO_2 = 5$nm/NC IGZO $= 16$ nm/$SiO_2 = 12.5$ nm stacked gate dielectric, which is the cross-sectional view in AA' direction. (d) Magnification of SiO_2/NC IGZO/SiO_2 stacked gate dielectric.

ambient. A 200-nm-thick SiO_2 passivation layer was deposited. Finally, a 300-nm-thick Al–Si–Cu metallization was performed and sintered at 400 °C in nitrogen ambient for 30 min. The NVMs with conventional top gate ($gate\ width = 1\ \mu$m) were also fabricated for comparison and demonstration.

III. Results and Discussion

Fig. 1(a) shows the top view of the pi-gate TFT NVM with an NC IGZO charge-trapping layer, and Fig. 1(b) shows the cross-sectional view of pi-gate NVMs in BB' direction. Fig. 1(c) shows the cross-sectional transmission electron microscopic (TEM) photograph of one NW of trigate NVM in AA' direction, and the poly-Si active layer of trigate device is surrounded by the stacked gate dielectric. The physical width of each NW is 45 nm, and the gate length is 0.7 μm. Fig. 1(d) shows the enlarged area of the SiO_2/NC IGZO/SiO_2 stacked dielectric. The physical thicknesses of tunneling oxide, charge-trapping layer, and blocking oxide are 5, 16, and 12.5 nm [Fig. 1(c)]. However, these thicknesses are not consistent with the measured thicknesses of these layers that are individually grown or deposited on the control wafers. The measured thicknesses are 8.5, 10, and 16.5 nm of SiO_2, IGZO, and SiO_2 thin films on the control wafer. The differences of the tunneling and blocking oxide thicknesses between device and control wafers are similar. This phenomenon may be explained by the diffusion of IGZO layer into SiO_2 layer during the rapid thermal annealing for implantation activation. Simultaneously, the IGZO thin film crystallizes and self-assembles to form the NCs with the diameter of around 16 nm.

Fig. 2 shows the normalized drain current ($I_d \times L/W$) versus gate voltage for trigate and conventional devices in fresh, programmed, and erased states. The devices are programmed at $V_{gs} = 11$ V for 1 s from the fresh state and erased at $V_{gs} = -11$ V for 1 s from the programmed state. The read condition of

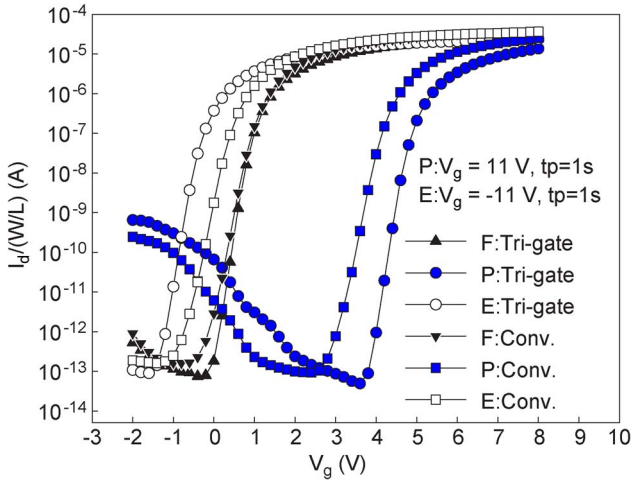

Fig. 2. I_d–V_g transfer characteristics of fresh trigate and conventional devices with an NC IGZO charge-trapping layer. Both devices are programmed at $V_{gs} = 11$ V for 1 s from the fresh state and erased at $V_{gs} = -11$ V for 1 s from the programmed state.

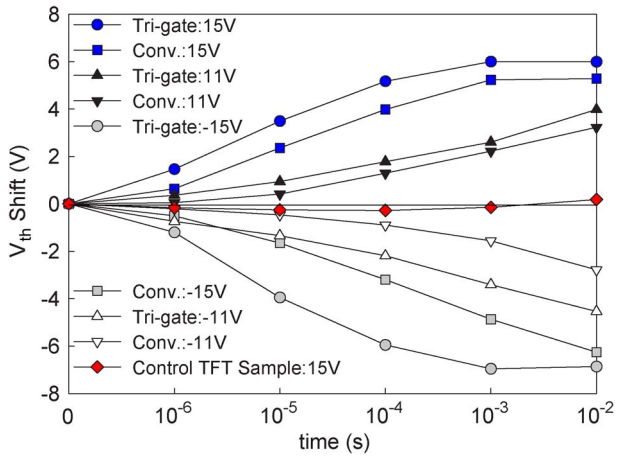

Fig. 3. P/E characteristics of trigate and conventional NVMs with an NC IGZO charge-trapping layer under F–N bias conditions. A control sample trigate TFT without IGZO layer is also compared.

I_{ds}–V_{gs} curves is $V_{ds} = 0.5$ V, and V_{gs} is swept from -2 to 8 V. The subthreshold slope of trigate and conventional devices are 195 and 210 mV/dec, respectively. The trigate device reveals better transistor characteristics due to superior gate control of trigate structure [3].

Fig. 3 shows the P/E characteristics of trigate and conventional devices. The programming operations use the F–N tunneling mechanism at $V_{gs} = 11$ and 15 V with grounded S/D from the erased state of $V_{th} = -1$ V. The erasing operations also use the F–N tunneling mechanism at $V_{gs} = -11$ and -15 V with the grounded S/D from the programmed state of $V_{th} = 4.4$ V. The results in Fig. 3 indicate that the trigate device has higher F–N P/E efficiency than that of conventional device because of corner effect [2], [3]. Both trigate and conventional devices exhibit high P/E speeds due to extra high density traps on large surface area of NCs. In addition, it is noteworthy that the erasing speed of the poly-Si memory with the IGZO charge-trapping layer is very fast. These characteristics totally differ from those of the previously studied NVMs which use a-IGZO as an active channel and a charge-trapping layer. The

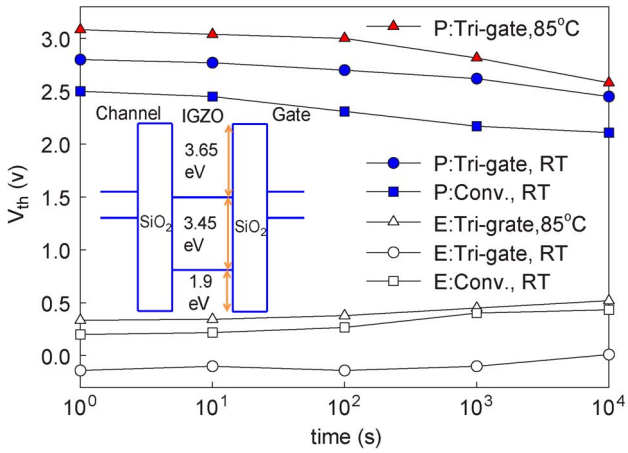

Fig. 4. Retention characteristics of trigate and conventional devices with an NC IGZO charge-trapping layer at room temperature (RT) and 85 °C. The $V_{\rm th}$ of fresh trigate device is 1 V, which net charge is nearly zero in the NC IGZO charge-trapping layer. The inset is the band diagram of poly-Si/SiO_2/IGZO/SiO_2/poly-Si stacked film.

NVMs with the a-IGZO channel exhibit very poor F–N erasing characteristics [12]–[14]. The IGZO thin film has ionic bond, and the conducting electrons originate from oxygen vacancies. Therefore, the a-IGZO thin film exhibits n-type conductivity and lack of holes [10]. In other words, in F–N erasing operation, much larger gate voltage is needed to form the hole inversion layer for supplying tunneling current in the a-IGZO channel. This shortage of holes in the a-IGZO active channel results in very slow F–N erasing characteristics. In addition, the stored electrons of IGZO charge-trapping layer are trapped under the conduction band at the programmed state, which also explains the extremely slow erasing speed [14], [15]. However, in this study, the active channel is undoped poly-Si thin film and much easier to form an inversion layer for supplying hole. This characteristic allows a high F–N erasing speed for NVM. For further demonstrating the charge storage capability of the NC IGZO charge-trapping layer, the programming characteristic of control sample, i.e., a trigate TFT ($W/L = 67$ nm $\times$ 10/1 μm) with single 26-nm *tetraethyl orthosilicate* oxide gate dielectric, is also presented, and it is the absence of $V_{\rm th}$ shift.

Fig. 4 shows the data retention of trigate and conventional devices measured at room temperature and 85 °C. The memory windows of trigate and conventional devices sustain 72% and 83%, respectively, after 10^4 s at room temperature. At 85 °C, the memory window of trigate device sustains 75% after 10^4 s. The conduction band difference between IGZO and SiO_2 is 3.65 eV, and the valence band difference is 1.9 eV [12]. As the NC IGZO charge-trapping layer sustains large amount of charges for data storage, these deep quantum wells suppress direct tunneling effect from the charge-trapping layer into the channel. Moreover, the stored charges in the deep trap sites of the NC IGZO charge-trapping layer can also help to prevent data loss [14], [15]. However, further optimizations for the thicknesses of tunneling oxide layer and a-IGZO thin film are necessary for better endurance and retention characteristics. Due to the diffusion of IGZO layer and volume-expansion-induced stress during growing thermal oxide at the corner [Fig. 1(c)], the thickness of tunneling oxide decreases to 3 nm at the corner. Hence, the tunneling oxide fails easily at high-voltage operations.

IV. Conclusion

A poly-Si thin-film Flash NVM with an NC IGZO charge-trapping layer has been presented. Experimental results indicate that memories with NC IGZO charge-trapping layer exhibits high and symmetric P/E characteristics by F–N tunneling current. The data retention is satisfactory for NVM applications due to deep quantum well and deep trap sites in the NC IGZO thin film. This investigation examines the feasibility of poly-Si thin-film NVM with NC IGZO charge-trapping layer on future AMLCD SOP and 3-D layer-to-layer stacked high-density NAND memory applications.

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