Characteristics of the Fluorinated High-k Inter-Poly Dielectrics

Chih-Ren Hsieh, Yung-Yu Chen, Kwung-Wen Lu, Gray Lin, and Jen-Chung Lou

***Abstract*—In this letter, the reliabilities and insulating characteristics of the fluorinated aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) inter-poly dielectric (IPD) are studied for the first time. Compared with the IPDs without fluorine incorporation, the results clearly indicate that fluorine incorporation process is effective to improve the insulating characteristics of both the Al_2O_3 and HfO_2 IPDs, mainly ascribed to the trap density reduction and the smooth interface. Although HfO_2 possesses higher dielectric constant to increase the gate coupling ratio, the results apparently indicate that the fluorine incorporation process is more effective to improve the dielectric characteristics of the Al_2O_3 IPD than the HfO_2 IPD.**

***Index Terms*—Al_2O_3, fluorine, HfO_2.**

I. Introduction

THE FLASH memory market has shown exponential increases, particularly in the area of mass storage application. In the coming decade, we will be required to provide flash technology that is compatible with the read/write speed of embedded dynamic random access memory and high nonvolatility. For the floating-gate flash memory, the inter-poly dielectric (IPD) requires a high breakdown voltage and a low leakage current to obtain better data retention [1], [2]. Incorporating alternative high dielectric constant (high-k) materials to replace current oxide/nitride/oxide (ONO) IPD of the floating-gate flash memories can be a way to increase the floating gate capacitance without extending the cell area and complicating the fabrication process while suppressing the charge loss [3], [4]. However, direct deposition of high-k dielectrics without interface treatments either on the polysilicon (Si) or on the Si substrate would inevitably result in a poor interface between the gate dielectrics and the poly-Si or between the gate dielectric and the Si substrate due to undesirable interface reoxidation [4], [5].

Recently, dielectric properties and device characteristics with fluorine incorporated high-k gate stacks have been studied comprehensively [6], [7]. Fluorine implantation prior to the gate dielectric deposition can widely distribute fluorine atoms within the high-k films, then recover interfacial dangling bonds and bulk oxygen vacancies during subsequent processes, which is useful to reduce gate leakage current and to improve dielectric reliabilities [8], [9]. Nevertheless, the effects of fluorine incorporation within the high-k dielectric, serving as the IPD of the floating-gate flash memory, are seldom investigated. In this study, for the first time, the reliability characteristics of the fluorinated high-k IPDs are studied in order to further enhance the dielectric insulating properties.

II. Experiment

In the experiment, the n^+-poly-Si/IPD/n^+-poly-Si capacitors were fabricated on 6-in p-type (100)-oriented silicon wafers. Then, a 200-nm poly-Si gate was deposited on the buffer oxide by a low-pressure chemical vapor deposition (LPCVD) system using SiH_4 gas at 620 °C and subsequently implanted with phosphorous at 5×10^{15} cm^{-2}, 20 keV to form the n^+ poly-Si bottom gate. Prior to the aluminum oxide (Al_2O_3) or hafnium oxide (HfO_2) dielectric deposition, the bottom gate was subjected to fluorine ion (F^+) implantation at 5×10^{13} cm^{-2}, 10 keV (defined as AlOF and HfOF in the figures, respectively). After conventional RCA cleaning and sequentially etching in diluted hydrofluoric acid to remove particles and native oxides, Al_2O_3 and HfO_2 IPDs were then deposited by metal-organic chemical vapor deposition with O_2 gas at 500 °C followed by postdeposition annealing at 900 °C and 600 °C in N_2 ambient for 30 s, respectively. Subsequently, a 200-nm n^+ poly-Si top gate was fabricated in the same way as the n^+ poly-Si bottom gate, followed by dopant activation with rapid thermal annealing at 950 °C in N_2 ambient for 30 s. After the gate stacks were patterned, the 500-nm TEOS oxide passivation and the Al metallization were defined.

The high-k IPDs without interface treatment (defined as AlO and HfO in the figures) were also fabricated to evaluate the impact of the fluorine incorporation. Scaled ONO IPD was used as a reference. The ONO IPD consists of a 1.5–2-nm thermally grown bottom oxide on the n^+ poly-Si bottom gate at 850 °C in an O_2/N_2 environment, a 4–9-nm LPCVD nitride layer deposited on top at 700 °C using SiH_2Cl_2 and NH_3 gases, and lastly, a 1–1.5-nm top oxide formed by wet oxidation of the nitride layer at 950 °C in an O_2/H_2 ambient. In addition, the insulating characteristic of the ONO IPD with equivalent oxide thickness (EOT) varying from 4–8 nm was extracted as the trend line shown in the figures. EOT was obtained from the high-frequency (100 kHz) capacitance–voltage measurement using a Hewlett-Packard (HP) 4284 LCR meter. The electrical properties and reliability characteristics of the inter-poly capacitors were measured using an HP4156C semiconductor

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TABLE I
EXTRACTED DIELECTRIC CONSTANT (k) OF THE HIGH-k IPDS

Al_2O_3 IPD	k	HfO_2 IPD	k
AlO	8.6	HfO	13.2
AlOF	9.0	HfOF	14.1

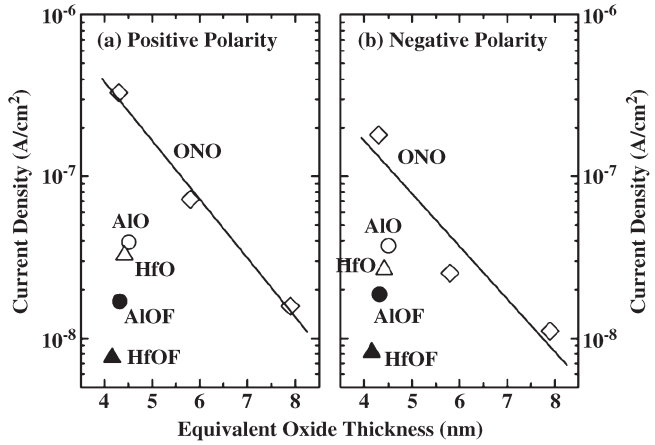

Fig. 1. Low-field (3 MV/cm) current density of the fluorinated high-k IPDs measured in (a) positive and (b) negative polarities.

parameter analyzer. The extracted k-value of the Al_2O_3 and HfO_2 IPDs was listed in Table I.

III. RESULTS AND DISCUSSIONS

Fig. 1 plots the leakage current density at a relatively low electric field (3 MV/cm) for the fluorinated high-k IPDs measured in (a) positive and (b) negative polarities in order to simulate the bias condition during data retention and to examine the charge loss. Compared with the ONO IPD, both high-k IPDs without interface treatment (AlO and HfO) can obviously reduce leakage current density in both polarities at the same EOT due to physically thicker thickness. Fluorine incorporation can further reduce the leakage current greater than one order of magnitude. Since a critical issue in the design criteria of the stacked-gate flash memory is eliminating the leakage path between the floating gate and the control gate to sustain charge retention, flash memory with high-k IPD is expected to significantly suppress charge loss more effectively than ONO IPD.

Breakdown voltage comparison between high-k IPDs and ONO IPD is shown in Fig. 2. Compared with ONO IPD in both polarities at similar EOT, the improvement of breakdown voltage for Al_2O_3 IPD without fluorine incorporation can be larger than 3 V, whereas the breakdown voltage for fluorinated Al_2O_3 IPD can be further increased to larger than 4 V. However, fluorine implantation process is ineffective in increasing the breakdown voltage of the HfO_2 IPD.

Directly deposited HfO_2 IPD without interface treatment exhibits extremely poor charge-to-breakdown ($Q_{\rm BD}$) value than ONO IPD, as shown in Fig. 3. Although the result indicates that HfO_2 IPD with fluorine incorporation can increase the $Q_{\rm BD}$, the extracted $Q_{\rm BD}$ of the fluorinated HfO_2 IPD seems too small to be implemented. On the other hand, Al_2O_3 IPD can obviously increase the $Q_{\rm BD}$. Fluorine incorporation within the Al_2O_3 IPD can further improve the $Q_{\rm BD}$ in both polarities. The 63% failure

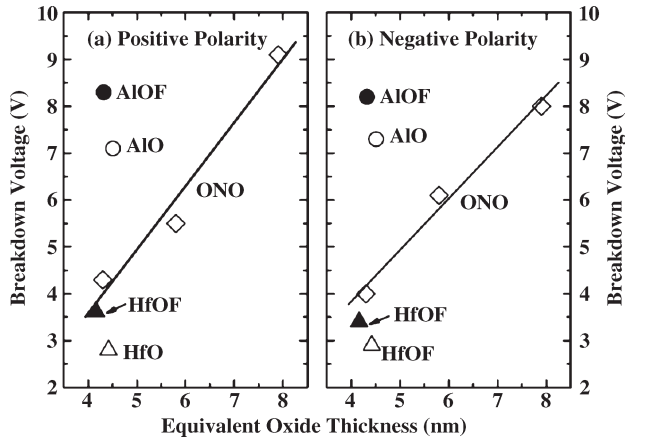

Fig. 2. Breakdown voltage comparison of the fluorinated high-k IPDs measured in (a) positive and (b) negative polarities.

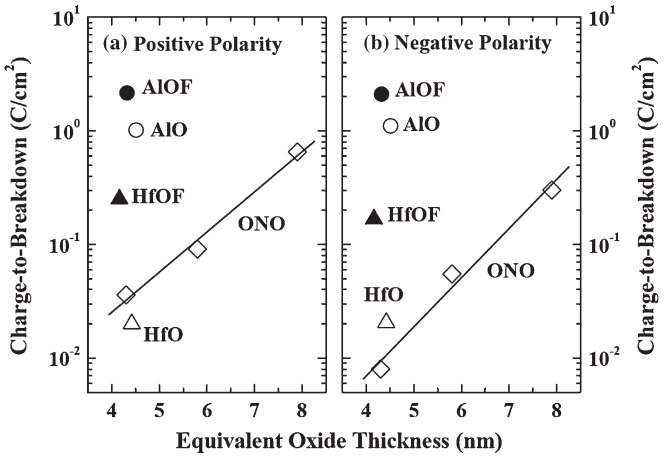

Fig. 3. Comparison of 63% charge-to-breakdown failure rate of the fluorinated high-k IPDs under constant voltage stress in (a) positive and (b) negative polarities.

$Q_{\rm BD}$ of the fluorinated Al_2O_3 IPD is larger than 2.1 C/cm^2 in both polarities, which is much higher than the $Q_{\rm BD}$ of the fluorinated HfO_2 IPD.

Since the slope of the Weibull distribution is an important factor in reliability calculation to extrapolate lifespan to different percentiles, the Weibull slope (β) of the $Q_{\rm BD}$ distribution is further extracted to examine the dielectric reliability as shown in Fig. 4. Obviously, Al_2O_3 IPD exhibits much higher Weibull slope than HfO_2 and ONO IPD in both polarities. Fluorine incorporation can be used to further tighten up the Weibull slope of the Al_2O_3 IPD. Since higher and symmetric device characteristics can contribute to further IPD scaling, the results clearly demonstrate that the fluorinated Al_2O_3 IPD is more effective to promote the device performance of the stacked-gate flash memory.

The apparent dielectric characteristics improvement of the fluorinated Al_2O_3 IPD can be partially ascribed to the diminishing of the dangling bonds and the oxygen vacancies with fluorine atoms [6], [9]. Fluorine incorporation is effective to replace low-k oxygen vacancies (vacuum) by the fluorine atoms [9] and results in higher dielectric constant as shown in Table I. For the Al_2O_3 IPD with fluorine incorporation, binding energy

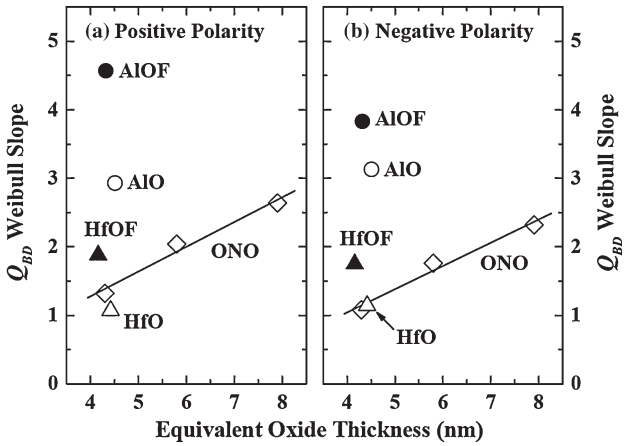

Fig. 4. Weibull slope of the charge-to-breakdown ($Q_{\rm BD}$) distribution for the fluorinated high-k IPDs under (a) positive and (b) negative stresses.

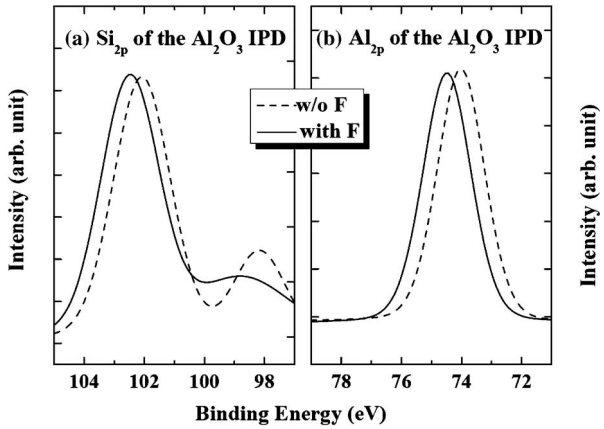

Fig. 5. XPS spectrum of the (a) Si_{2p} and (b) Al_{2p} signals for the fluorinated Al_2O_3 IPD.

increment which is larger than 0.5 eV is obtained for both the Si and the Al signals as shown in Fig. 5. The results clearly indicate that fluorine incorporation is effective to terminate the bulk oxygen vacancies and the interface dangling bonds, which will create stronger Al–F and Si–F bonds within the fluorinated Al_2O_3 IPD, respectively. Higher Si and Hf binding energy is also detected for the HfO_2 IPD with fluorine incorporation, which forms stronger Hf–F and Si–F bonds within the fluorinated HfO_2 IPD (not shown).

Moreover, the fluorinated high-k IPDs obviously reveal polarity-dependent properties. The dielectrics stressed in positive polarity (electron injection from the poly-Si bottom gate) clearly exhibit superior dielectric characteristics than those stressed in negative polarity (electron injection from the poly-Si top gate) as shown in Figs. 1–4. The polarity-dependent dielectric properties of the fluorinated high-k IPDs can be hypothetically explained by the surface roughness of the bottom gate and the top gate. Fluorine implantation prior to the high-k dielectrics deposition is believed to form hydrophobic Si–F bonds during subsequent high-temperature dielectric deposition and annealing, which is beneficial to the reduction of the interfacial reoxidation and interface roughness [9]–[11]. This also results in higher dielectric constant as shown in Table I. A smoother interface is helpful in reducing the localized field, which can also suppress trap density generation [4]. In consequence, less trap density generation and smooth interface at the bottom gate will inevitably contribute to superior dielectric characteristics when the fluorinated high-k IPDs are stressed in positive polarity.

IV. Conclusion

The leakage current density, breakdown voltage, $Q_{\rm BD}$, and Weibull slope have been compared between the fluorinated high-k IPDs and ONO IPD in this letter. Fluorine incorporation process can be used to further improve the insulating characteristics of both high-k IPDs. Moreover, fluorinated Al_2O_3 IPD clearly indicates the best dielectric characteristics at similar EOT. Fluorination of the Al_2O_3 IPD can promote the IPD characteristics more effectively than the fluorination of the HfO_2 IPD. The results undoubtedly demonstrate that the fluorine incorporation process possesses higher potential to be implemented for future stacked-gate flash memory application due to the superior insulating properties.

References

[1] C. Cobianu, O. Popa, and D. Dascalu, "On the electrical conduction in the interpolysilicon dielectric layers," *IEEE Electron Device Lett.*, vol. 14, no. 5, pp. 213–215, May 1993.

[2] T. One, T. Mori, E. Ajioka, and T. Takayashiki, "Studies of thin poly-Si oxides for E and E2PROM," in *IEDM Tech. Dig.*, 1985, pp. 380–383.

[3] D. Wellekens, P. Blomme, B. Govoreanu, J. D. Vos, L. Haspeslagh, J. V. Houdt, D. P. Brunco, and K. V. D. Zanden, " Al_2O_3 based flash interpoly dielectrics: A comparative retention study," in *Proc. Solid-State Device Res. Conf.*, 2006, pp. 238–241.

[4] Y. Y. Chen, C. H. Chien, and J. C. Lou, "Characteristics of the inter-poly Al_2O_3 dielectrics on NH_3-nitrided bottom poly-Si for next-generation flash memories," *Jpn. J. Appl. Phys.*, vol. 44, no. 4A, pp. 1704–1710, Apr. 2005.

[5] S. C. Chen, Y. Y. Chen, Y. T. Chang, J. C. Lou, K. T. Kin, and C. H. Chien, "Improvements of ozone surface treatment on the electrical characteristics and reliability in HfO_2 gate stacks," *Microelectron. Eng.*, vol. 84, no. 9/10, pp. 1898–1901, Sep./Oct. 2007.

[6] H.-H. Tseng, P. J. Tobin, S. Kalpat, J. K. Schaeffer, M. E. Ramon, L. R. C. Fonseca, Z. X. Jiang, R. I. Hegde, D. H. Triyoso, and S. Semavedam, "Defect passivation with fluorine and interface engineering for Hf-based high-k/metal gate stack device reliability and performance enhancement," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3267–3275, Dec. 2007.

[7] C. R. Hsieh, Y. Y. Chen, and J. C. Lou, "Effect of fluorinated silicate glass passivation layer on electrical characteristics and dielectric reliabilities for the HfO_2/SiON gate stacked nMOSFET," *Microelectron. Eng.*, vol. 87, no. 11, pp. 2241–2246, Nov. 2010.

[8] H.-S. Jung, S. K. Han, H. Lim, Y.-S. Kim, M. J. Kim, M. Y. Yu, C.-K. Lee, M. S. Lee, Y.-S. You, Y. Chung, S. Kim, H. S. Baik, J.-H. Lee, N.-I. Lee, and H.-K. Kang, "Dual high-k gate dielectric technology using selective AlOx etch (SAE) process with nitrogen and fluorine incorporation," in *VLSI Symp. Tech. Dig.*, 2006, pp. 162–163.

[9] M. Inoue, S. Tsujikawa, M. Mizutani, K. Nomura, T. Hayashi, K. Shiga, J. Yugami, J. Tsuchimoto, Y. Ohno, and M. Yoneda, "Fluorine incorporation into HfSiON dielectric for Vth control and its impact on reliability for poly-Si gate pFET," in *IEDM Tech. Dig.*, 2005, pp. 413–416.

[10] R. A. Haring and M. Liehr, "Reactivity of a fluorine passivated silicon surface," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 10, no. 4, pp. 802–805, Jul./Aug. 1992.

[11] C. S. Lai, W. C. Wu, T. S. Chao, J. H. Chen, J. C. Wang, L. L. Tay, and N. Rowell, "Suppression of interfacial reaction for HfO_2 on silicon by pre- CF_4 plasma treatment," *Appl. Phys. Lett.*, vol. 89, no. 7, p. 072 904, Aug. 2006.