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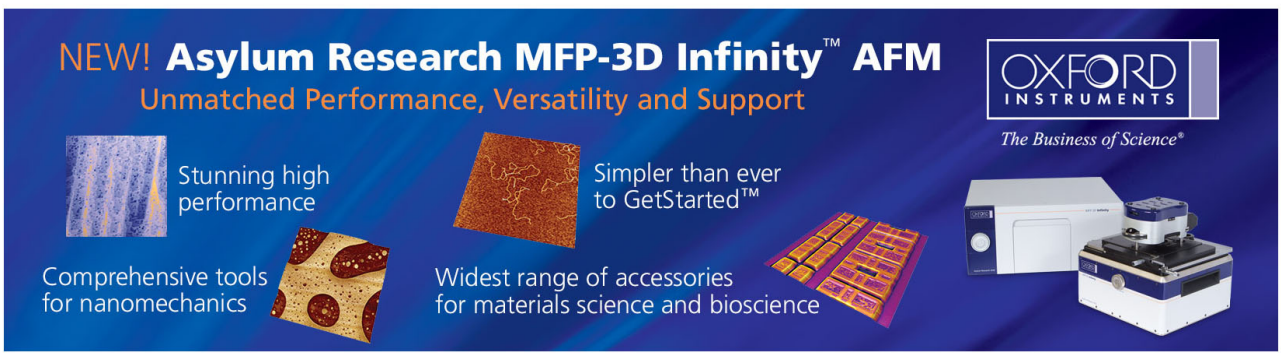

Polymer space-charge-limited transistor as a solid-state vacuum tube triode

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We report the construction of a polymer space-charge-limited transistor (SCLT), a solid-state version of vacuum tube triode. The SCLT achieves a high on/off ratio of 3×10^5 at a low operation voltage of 1.5 V by using high quality insulators both above and below the grid base electrode. Applying a greater bias to the base increases the barrier potential, and turns off the channel current, without introducing a large parasitic leakage current. Simulation result verifies the influence of base bias on channel potential distribution. The output current density is 1.7 mA/cm^2 with current gain greater than 1000. © *2010 American Institute of Physics*. [doi:10.1063/1.3513334]

Since the late 19th century, scientists have researched technologies that provide electronic switch and signal amplifier. The vacuum tube is a triode with a hot cathode, plate anode, and a controlling grid inside an evacuated glass tube. Since its patent in 1906, the vacuum tube became a dominant technology until the rise of the transistor, at around 1960. Yet even today, vacuum tubes survive in specialist areas, including high-power applications, audio amplifiers, and in military applications due to its resistance to electromagnetic pulse. Aside from these practical applications, the vacuum tube is elegant in both structure and operation principle. It is thus interesting to ask whether the vacuum tube concept can see a revival in this era of solid-state electronics, and once again prove its unique advantages.

Attempts during the 1950s and 1960s, to build vacuum tubes using inorganic semiconductors, proved unsuccessful because of difficulties with the dopant diffusion process in forming the grid structure.[1–3] Several reports, since the 1990s, describe research into intrinsic organic semiconductor designs that deliver vacuum tube functionality.[4,5] Fabrication of the grid, by deposition through a shadow mask, with openings on the micron-scale, results in poor current density and on/off ratio.[4] Improvements in grid design, using high-density nanometer scale openings increased output current density to greater than 1 mA/cm^2,[6–8] sufficient for most applications. The difficulty regarding the on/off ratio of solid-state vacuum tubes lies in the large spatial overlap between the grid and collector electrode. In an early solid-state device design,[7] the on/off ratio was only 10^2; recently we raised it to 10^4 by introducing an insulator to surround the grid.[9] A key challenge to the development of a solid-state version of the vacuum tube is to raise the on/off ratio to around 10^5, this being the generally accepted ratio required for practical applications.[10] For example, in the switching transistor for a sensor array with 1000 lines, the current readout is the sum of the currents for one line in the on-state, and 999 lines in the off state. The latter must be one order of magnitude smaller than the range of variation of the former, which is usually ten times. The transistor on-current must therefore be at least 10^5 times larger than the off-current.[10] In this study, we attained an on/off ratio of 3×10^5 by simply increasing the thickness of the insulator between the emitter and the grid. The greater thickness allows a wider range of grid potentials able to modulate the collector current before breakdown occurs. With this final improvement, the solid-state vacuum tube offers superior performance features compared to its field-effect transistor counterpart, with lower voltage, higher output current, and comparable on/off ratio.

We named our solid-state version of the vacuum tube triode a "polymer space-charge-limited transistor" (SCLT). Figure 1(a) shows a schematic diagram of the device and Fig. 1(b) is a scanning electron microscopy (SEM) image of the openings form at sites without Al. In operation, the holes are injected into organic semiconductor by the emitter, and are collected by the collector. The emitter-collector diode's space-charge-limited current (SCLC) is modulated by a metal base electrode embedded within the semiconductor. The voltages applied to the collector and base, determine a potential barrier between the emitter and collector. The SCLT on and off states are determined by whether carriers encounter a high or low potential barrier. Simulation for the proposed SCLT device were carried out with Silvaco TCAD ATLAS software. Simulation parameters are given in Ref. 11. Figure 1(d) shows a simulated potential distribution at the central vertical channel when collector-to-emitter voltage (V_{CE}) is –1.5 V and base-to-emitter voltage (V_{BE}) varies from 2.5 to –2.5 V. The figure describes a strong bias effect on potential distribution. A more positive V_{BE} leads to a higher potential barrier to turn off the channel current. A simulated channel current density J_{CE} versus V_{BE} plot, for V_{CE} equal to –1.5 V reveals that, in the absence of all parasitic leakage, the device on/off current ratio could be greater than nine orders of magnitude.

Figure 1(c) depicts origins of the SCLT off-current. At a fixed negative V_{CE}, the output collector current density (J_C) is the sum of J_{C1} and J_{C2}. J_{C1} is the current density from emitter to collector, J_{C2} is the leakage current density from base to collector, and J_3 is the leakage current between base and emitter. The arrows indicate the direction of current.

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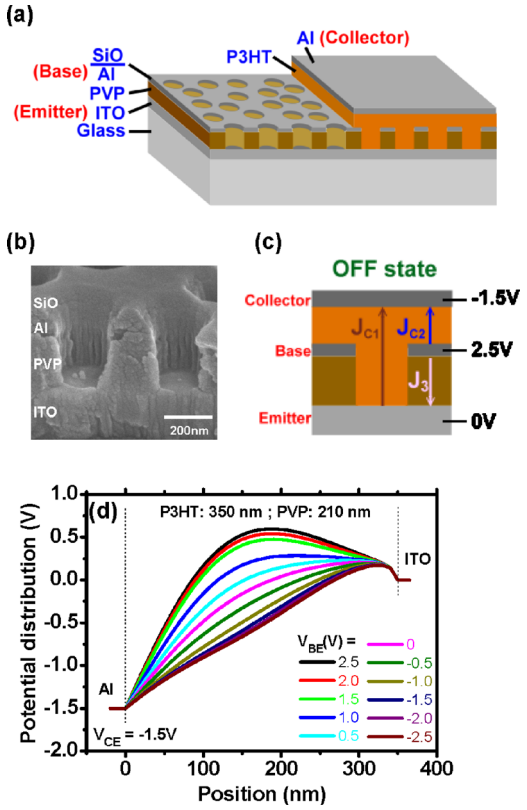

FIG. 1. (Color online) (a) Schematic diagram of SCLT device structure. (b) SEM image of openings formed at sites without Al grid prior to spin coating with P3HT. The white scale bar indicates 200 nm. (c) Three current sources in SCLT. J_{C1} is the current density from emitter to collector, J_{C2} is the leakage current density from grid to collector, and J_3 is the leakage current density between emitter and collector. (d) A simulated potential distribution at the central vertical channel. Higher base-bias leads to a higher potential barrier.

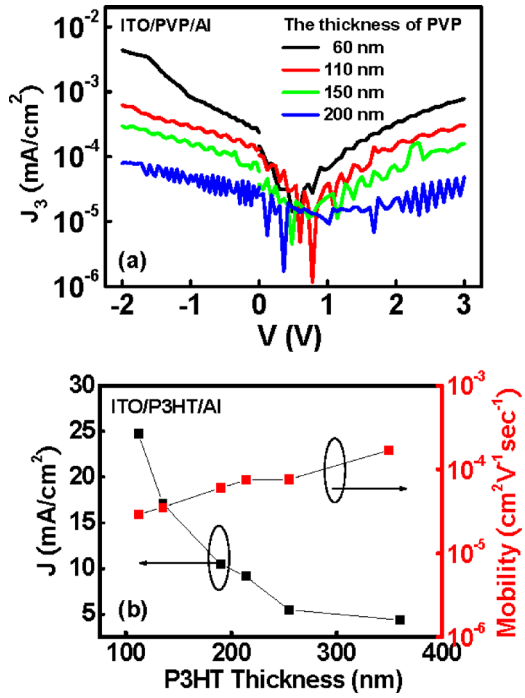

FIG. 2. (Color online) (a) *J-V* characteristics of insulating PVP layer of various thicknesses. The device structure is ITO/PVP/Al. (b) Current density at 2.5 V for diodes with various P3HT thicknesses. The device structure is ITO/P3HT/Al. Carrier mobility of each diode was obtained from the SCLC.

Tuning the V_{BE} from negative to positive suppresses J_{C1}, however, J_{C2} and J_3 both increase, since the voltage drop across the base and collector (V_{BC}), and V_{BE} are increased. The minimum of J_C is reached as J_{C2} becomes comparable to J_{C1}. Hence, in order to maximize the on/off ratio, while keeping the current gain high, ways to reduce J_{C2} and J_3 must be found. We added a 50 nm insulating SiO layer above the base electrode, and increased the thickness of the PVP insulating layer below the base electrode to 210 nm. We demonstrate a polymer vertical transistor with enhanced insulating properties of the insulating layers, which allows a high V_{BE} and makes a high on/off ratio of 3×10^5 possible.

The SCLT was fabricated on indium tin oxide (ITO) glass substrate which was plasma cleaned with 150 W O_2 plasma for 30 min to smooth the substrate. A 210 nm thick layer of cross-linkable PVP was spin coated onto the ITO substrate, and then cross-linked at 200 °C for 60 min under an inert atmosphere, and using methylated poly(melamine-co-formaldehyde) (Aldrich, Mw ~ 511) as a cross-linking agent. The PVP surface was made hydrophilic by 50 W O_2 plasma treatment, and then submerged into 210 nm diameter positively charged polystyrene (PS) spheres (Merck, K6-020) in dilute ethanol solution (0.8 wt % PS) for three minutes. The PS spheres adsorbed to the PVP surface to serve as the shadow mask. The substrate was then transferred to a beaker of boiling isopropanol solution for 10 s, to form two-dimensional colloidal arrays, and immediately blown dry in a stream of nitrogen gas. A 40 nm thick layer of Al, and 50 nm layer of SiO were deposited atop the PVP layer, to form the metal base electrode and upper insulator, respectively. After removing the PS spheres with adhesive tape (Scotch, 3M), PVP material at sites without Al coverage was removed by O_2 plasma treatment at 150 W for 13 min. In a glove box, a 350 nm poly(3-hexylthiophene) (P3HT) layer was spin coated onto the substrate from 4.5 wt % chlorobenzene solution. Finally, the aluminum collector material was deposited to complete the SCLT with a 1 mm^2 active area.

Figure 2(a) shows insulating properties of PVP layers of various thicknesses. The 210 nm PVP device exhibited lower leakage current density than the 60 nm device. The enhanced insulating properties of 210 nm PVP allow the emitter-base diode to sustain higher bias without breakdown. In order to improve the SCLT characteristics, the P3HT layer should be no thinner than the upper surface of the base, and depressions in the P3HT surface should not be observable in SEM images above the base opening sites.[12] Since we formed a 210 nm PVP layer, the P3HT layer must be thicker than 210 nm. Thus, we fabricated diodes in the ITO/P3HT/Al structure with various P3HT thicknesses, in order to understand the diode characteristics. The current densities of these diodes were recorded with 2.5 V applied on ITO emitter, and carrier mobility's were deduced from the currents follow SCLC. As shown in Fig. 2(b), current density decreases with increasing P3HT thickness, however, carrier mobility increases with increasing P3HT thickness. This phenomenon was also observed in small molecule organic diodes.[13,14] The authors concluded that the organic thin film's low mobility originated from an interfacial trap state, and molecular arrangement on the surface. In our case, since P3HT is known to be sensitive to surface conditions, the molecular orientation condition in the region close to the ITO must differ from

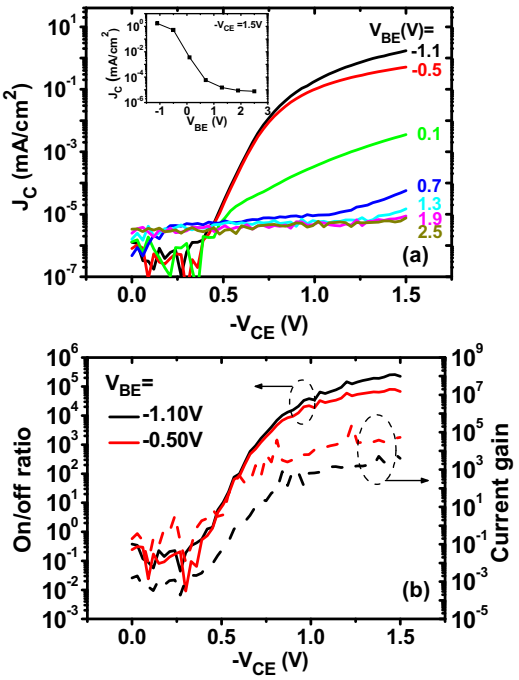

FIG. 3. (Color online) (a) J_C as a function of V_{CE} under various V_{BE} values. The inset shows the transfer characteristics of SCLT for V_{CE}=–1.5 V. (b) On/off ratio and current gain as a function of V_{CE}.

that of the bulk far away from the ITO. The influence of interfacial conditions on the diode characteristics is becomes weaker as the thickness of P3HT increases, and hence the mobility of P3HT increases with increasing thickness.

Figure 3 shows SCLT transistor characteristics. The inset of Fig. 3(a) shows the transfer characteristics of SCLT as determined from Fig. 3(a). The ITO emitter was grounded and the Al collector was negatively biased at V_{CE}. If V_{CE} equal to –1.5 V, then when V_{BE} is –1.1 V, the SCLT is in the on state, and J_C is 1.71 mA/cm^2. When V_{BE} is +2.5 V, J_C is suppressed and the SCLT is in the off state. The base current density (J_B) is in the order of 10^{-4}–10^{-5} mA/cm^2. Figure 3(b) shows on/off ratio and current gain of SCLT as functions of V_{CE}. The on/off ratio is obtained by dividing J_C (V_{BE} at –1.1 or –0.5 V) by J_C (V_{BE} at 2.5 V). The current gain is obtained by dividing J_C by J_B when V_{BE} is –1.1 or –0.5 V. As V_{CE} is –1.5 V, the maximum on/off ratio of 3×10^5 is achieved, and the current gain is still greater than 1000. This on/off ratio is larger than our previous work,[8,10] and is the highest value so far reported for polymer vertical transistors. Since the transistor on current is in the same order as in our previous report, the improved on/off ratio must arise from the reduced off current, which may come from two sources. One is that applying a more positive V_{BE} voltage to the base can improve the on/off ratio. Using high quality insulators both above and below the grid base electrode is the key factor to enhancing the on/off ratio. The other is that the ratio of emitter-to-base thickness to the opening diameter is greater than that used in our previous work. Better grid control is obtainable with a higher ratio.

We integrated a second SCLT in series with a load resistor (R_L=10 MΩ), to demonstrate a resistive-load inverter operating at low supply voltages as shown in Fig. 4. The V_{DD}

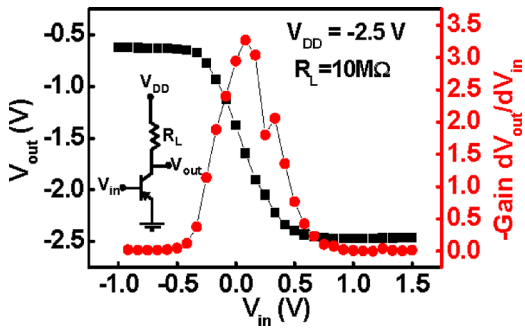

FIG. 4. (Color online) Transfer characteristics and gain of the inverter at V_{DD} of –2.5 V. The load resistance is 10 MΩ. The inset shows the schematic inverter circuit.

was fixed at –2.5 V while input voltage (V_{in}) was varied from –1 to 1.5 V. When V_{in} was 1.5 V, the SCLT is in the off state, the effective resistance from emitter to collector (R_{EC}) is high, and hence the output voltage (V_{out}) should approach V_{DD}. By contrast, when V_{in} is –1 V, the SCLT is in the on state, R_{EC} is low, and hence the V_{out} should approach zero. However, V_{out} is not close to 0.0 V when the SCLT is turned on. Increasing the output current when SCLT is in the on state can solve the problem. The absolute value of voltage gain is 3.3, higher than in our previous report.

In summary, we report the fabrication and operation of a SCLT with high on/off ratio and low operation voltage. By improving the insulator characteristics, a greater V_{BE} bias at the base is possible for suppression of the off current. The demonstration of an inverter application illustrated a possible application for organic electronics devices with low power consumption.

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[11]The SCLT characteristics simulation is made based on the device structure shown in Fig. 1(c). Insulator surrounds the grid is used to make the model more realistic. The thickness of PVP, Al grid, and P3HT are 200 nm, 40 nm, and 350 nm, respectively. The opening diameter is 210 nm. The highest occupied molecular orbital and lowest unoccupied molecular orbital levels of P3HT are 5.2 and 3.0 eV. The work function of emitter and collector are 5.2 and 4.3 eV. The hole mobility and electron mobility are 10^{-5} and 10^{-6} cm^2/V s.
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