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Highly scaled charge-trapping layer of ZrON nonvolatile memory device with good retention

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We have fabricated the TaN–[SiO_2–$LaAlO_3$]–ZrON–[$LaAlO_3$–SiO_2]–Si charge-trapping flash device with highly scaled 3.6 nm equivalent-Si_3N_4-thickness. This device shows large 4.9 V initial memory window, and good retention of 3.4 V ten-year extrapolated retention window at 85 °C, under very fast 100 μs and low ±16 V program/erase. These excellent results were achieved using deep traps formed in ZrON trapping layer by As^+ implantation that was significantly better than those of control device without ion implantation. © *2010 American Institute of Physics*. [doi:10.1063/1.3522890]

As listed in *International Technology Roadmap for Semiconductors*,[1] the metal-oxide-nitride-oxide-Si (MONOS) charge-trapping flash (CTF) devices[1–15] have high potential to replace the poly-Si floating-gate flash memory for future generation nonvolatile memory (NVM) due to the discrete charge-trapping property and simpler planar process. Nevertheless, one fundamental drawback for CTF device is the distributed trap energy in Si_3N_4 (Ref. 11) as compared with the deep 3.15 eV energy in poly-Si floating-gate memory, where charge stored in shallower traps may escape and degrade the retention characteristics.[12–15] Such degraded retention is one of the major challenges in fewer electrons stored in highly scaled NVM device.[1] Although improved retention can be achieved by increasing tunnel oxide thickness, this is traded off the intolerable slow erase time (10–100 ms).

One method to improve the retention is to use a deep conduction band energy (E_C) high-κ trapping layer.[12–16] Significant retention improvement has been realized by using high-κ Al(Ga)N in the MONOS CTF that was also listed in ITRS as a key technology for CTF.[1] To further lower the program/erase (P/E) voltage, higher κ HfON trapping layer MONOS has been fabricated,[14] but the shortcoming is the lower trapping efficiency in HfON with a smaller memory window.[14] To improve the memory window, dual trapping-layer HfON–Si_3N_4 CTF was used,[15] but adding the lower κ Si_3N_4 limits further down-scaling the equivalent-nitride thickness (ENT). However, scaling ENT to 3–4 nm is needed for future CTF NVM.[1] Alternatively, lower trapping energy can also be reached by forming nanocrystal in CTF using ion implantation.[17–20] In this paper we have used both higher-κ deep-E_C ZrON and As^+ implantation to improve the CTF performance. At a 3.6 nm ENT trapping layer, this device has an initial 4.9 V memory window and good retention of 3.4 V extrapolated ten-year retention window at 85 °C, under fast 100 μs and low ±16 V P/E. This is the thinnest ENT CTF device that meets ITRS scaling target to tenth nanometer.[1]

The TaN–[SiO_2–$LaAlO_3$]–ZrON–[$LaAlO_3$–SiO_2]–Si devices were fabricated on standard 6 in. *p*-type Si wafers. The double tunnel oxide layers of 2.5 nm thermal SiO_2 were grown on Si substrates and 2.5 nm $LaAlO_3$ was deposited by physical vapor deposition (PVD). Then the 18 nm ZrON charge trapping layer was deposited by reactive PVD under mixed O_2 and N_2. The As^+-implantation into ZrON was applied at 3 keV, 5×10^{15} cm^{-2} dose, and 60° titled angle, which was followed by 950 °C and 1 s rapid thermal annealing (RTA). It was reported that the memory window increases with increasing ion-implanted dose.[20] The As^+-implant condition of 5×10^{15} cm^{-2} and 3 keV dose were chosen to reach both the highest possible dose for manufacture and the lowest energy for the thinnest ENT. Next, 8 nm $LaAlO_3$ was deposited by PVD and 6 nm SiO_2 was deposited by chemical vapor deposition of tetraethyl orthosilicate [$Si(C_2H_5O)_4$] to form the double blocking layers. Finally, 200 nm TaN was deposited by PVD, followed by gate definition, self-aligned 25 keV As^+ implantation at 5×10^{15} cm^{-2} dose, and 900 °C RTA to activate the dopant at source-drain region. The flatband voltage (V_{FB}) was obtained from the measured *C-V* data and quantum-mechanical *C-V* simulation.[21] The threshold voltage (V_{th}) was determined from the interception of gate voltage (V_g) to zero drain current (I_d) of linear I_d-V_g curve.

Figure 1 compares *C-V* hysteresis of ZrON CTF devices with and without the As^+ implantation. Larger *C-V* hysteresis window of 8.1 V was obtained in As^+-implanted CTF than

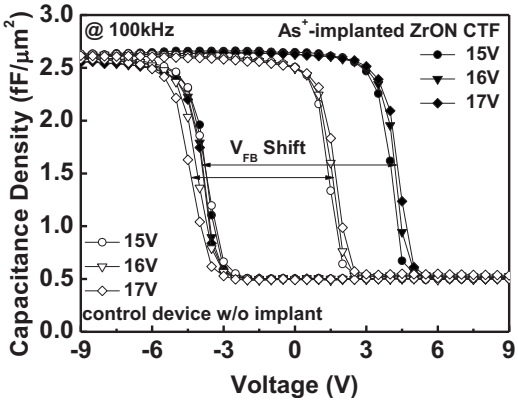

FIG. 1. *C-V* hysteresis of ZrON CTF devices with and without As^+ implantation.

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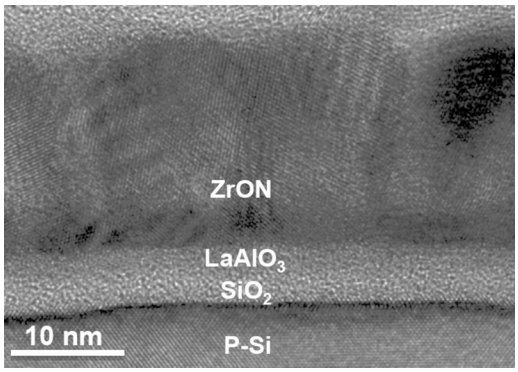
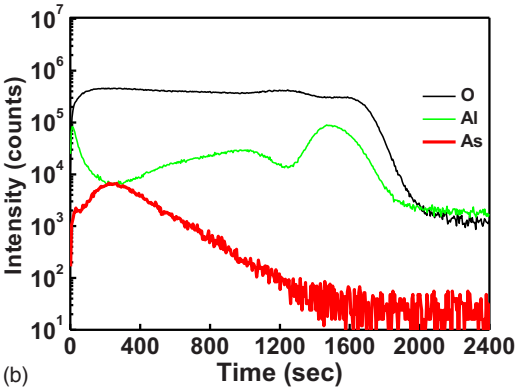


(a)



(b)

FIG. 2. (Color online) (a). Cross-sectional TEM and (b) SIMS of ZrON–[$LaAlO_3$–SiO_2]–Si structure with As^+ implantation.

the 5.7 V of control device under ±16 V sweep and close capacitance density of ~2.6 fF/μm^2 for both devices. Since the area of *C-V* curve is the charge ($Q=CV$), the increase of V_{FB} indicates that the As^+-implanted ZrON has higher trap density for electron storage. The larger hysteresis window by As^+ implantation may be due to the forming deep energy levels in ZrON trapping layer that exists even after 950 °C RTA. From the frequency-dependent *C-V* measurements, the V_{FB} shift (ΔV_{FB}) is independent on frequencies at 10–700 kHz. Thus, the hysteresis memory window is only from the ZrON trapping layer rather than the interface states between tunnel oxide and Si.

Figures 2(a) and 2(b) show the cross-sectional transmission electron microscopy (TEM) and secondary ion-mass spectroscopy (SIMS) of ZrON–[$LaAlO_3$–SiO_2]–Si structure with As^+ implantation. The polygrains were found in ZrON after 950 °C RTA that leads to the higher κ value[22,23] with As^+ implant. From the measured 18 nm ZrON thickness by TEM, an ENT of 3.6 nm was obtained from the ENT $=\kappa_{Si3N4}/\kappa_{ZrON}\times t_{ZrON}$, where the κ_{Si3N4}, κ_{ZrON}, and t_{ZrON} are the dielectric constant of Si_3N_4, dielectric constant of ZrON, and the thickness of ZrON, respectively. The concentration of implanted As decreases rapidly before entering the double tunnel layer of $LaAlO_3$-SiO_2. Such low energy tilted-angle As^+ implantation is important to reduce the damage to tunnel oxide layer.

Figure 3 shows the x-ray diffraction (XRD) spectra of ZrON–[$LaAlO_3$–SiO_2]–Si structure with and without As^+ implantation. The strong diffraction peaks indicate the good ZrON crystallinity that is important to provide higher κ ~35 (Refs. 22 and 23) with a smaller ENT of 3.6 nm. Besides, extra weak As peaks were also found in As^+-implanted

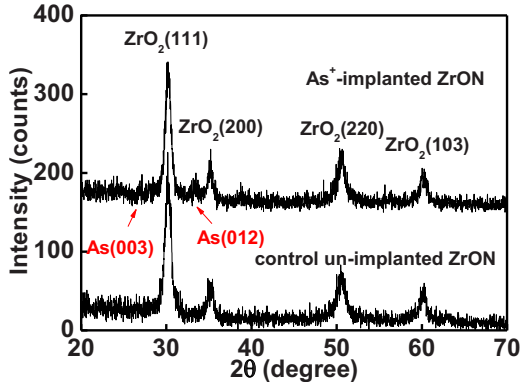


FIG. 3. (Color online) XRD of ZrON–[$LaAlO_3$–SiO_2]–Si structure with and without As^+ implantation.

and 950 °C-annealed ZrON, with the same angles of clustered As-dots in As-rich GaAs.[24] This suggests the possibility to form the deep energy levels in ZrON due to large As work-function of 5.1 eV,[25] which also explains the larger hysteresis shown in Fig. 1.

Data retention is one of the most importance parameters for NVM. Figure 4 shows the retention characteristics at 85 °C. Under ±16 V and 100 μs P/E, the As^+-implanted ZrON devices have a larger initial memory window of 4.9 V than the 2.9 V data of control device without As^+ implantation, suggesting the higher trap density in As^+-implanted ZrON trapping layer. The very fast 100 μs P/E speed is due to the additional conduction and valance band discontinuity (ΔE_C and ΔE_V) between $LaAlO_3$ and SiO_2, for easier electron and hole tunneling during program and erase, respectively. Still large ten-year extrapolated memory window of 3.4 V was obtained for As^+-implanted ZrON CTF device and better than that of control device. The good retention is due to the physically thicker double $LaAlO_3$–SiO_2 for carrier confinement, while the ΔE_C and ΔE_V in $LaAlO_3/SiO_2$ improve the program and erase speed. This large ten-year retention window with a small 3.6 nm ENT trapping layer also allows multilevel cell storage at 85 °C.[15]

In summary, we have used both higher κ ZrON and As^+ implantation to improve the device performance of MONOS CTF device. At record smallest 3.6 nm ENT, large 4.9 V initial memory window and good retention of 3.4 V ten-year extrapolated window at 85 °C were measured in this CTF

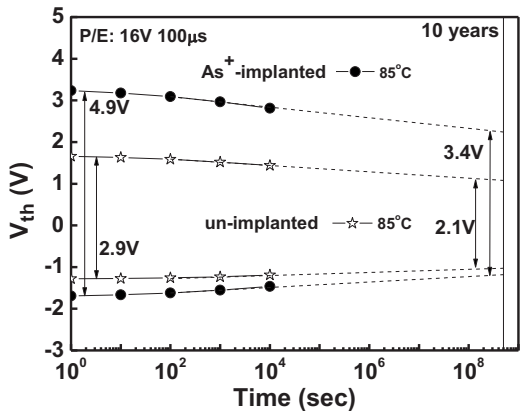


FIG. 4. Retention characteristics of ZrON MONOS CTF devices at 85 °C with and without As^+ implantation.

device, under very fast 100 μs speed and low P/E voltage of $\pm$16 V.

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