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The investigation of charge loss mechanism in a two-bit wrapped-gate nitride storage nonvolatile memory

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The charge loss mechanism of a two-bit wrapped-gate nitride storage nonvolatile memory is investigated. From retention measurements, it was shown that both vertical and lateral charge loss coexist. As a result of the misalignment of carriers, the lateral charge loss was caused by the hole accumulation near the junction and migrating toward the channel. By using a scaling of the word-gate length or a substrate-transient hot hole erase scheme, the charge loss in the lateral direction can be suppressed. Also, from the retention test, the latter scheme, substrate-transient hot hole (STHH), has a window independent of the word-gate length, which is better for the device scaling.
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Silicon-oxide-nitride-oxide-silicon (SONOS) flash memory is one of the most mature nitride-storage technologies, which allows one-bit/cell or two-bit/cell operation by using channel-hot-electron (CHE) injection programming and band-to-band hot-hole (BBHH) injection erasing.[1,2] However, the conventional SONOS flash memory has some disadvantages such as low programming efficiency, high power consumption, and high programming drain voltage, etc.

Another important issue related to the SONOS cell is the charge loss with time, the data retention. Two major models have been reported to explain the retention mechanisms. The first model is the vertical charge loss through bottom oxide, since the bottom oxide is strongly degraded during successive P/E stresses.[3–6] The trapped electrons in the nitride storage can escape through Frankel–Pool tunneling and trap-assist-tunneling to the substrate. The second model explains the charge loss through the lateral redistribution of holes because of a misalignment.[6–9] After long term P/E cycles, a large amount of holes accumulation near the junction, the holes might spread out and migrate into the channel before recombining with the programmed electron through thermal activation. In recent years, a SONOS-type memory cell with wrapped gate was demonstrated,[10,11] which is feasible for high density, high speed, and low power consumption. By utilizing source-side-injection (SSI) programming, the wrapped-gate SONOS can achieve hundred times better efficiency than CHE ones.[10,11] However, none has been studied on the reliability issues of such device, especially the data retention. With the specific structure of wrapped-gate SONOS, we can take the advantage to suppress the misalignment of charge distribution. The mechanism of this approach will be proposed.

Figure 1 shows the device structure and the simulation result by using SYNOPSYS SENTAURUS TCAD (technology computer aided design) software.[12] The device has a control gate wrapped by the ONO layer and then a word gate is grown on the top. A nitride-cap layer (300 Å) was grown on top of the control gate and with a tunnel oxide (65 Å) at the bottom. From the TEM cross-section, the experimental devices have ONO layer thickness, with 65 Å bottom oxide, 60 Å nitride, and 80 Å top oxide. The ONO-layer was cutoff by the self-alignment process at the edge of the source/drain, and the oxide thickness between word gate and the source/drain region is about 500 Å. The gate width is about 0.2 μm, and the channel length is 0.18 μm under the control-gate and with three different splits of 0.10, 0.12, and 0.13 μm for the word-gate length, L_{WG}. It was shown that the gap region has the largest electric potential drop and forms a largest lateral electric field. Therefore, the electron will get sufficient energy in the gap region, inducing impact ionization to achieve programming operation. The programming charge should be injected to the right (left) side of the word-gate between the gap and the drain (source). The programming and erasing condition are shown in Table I.

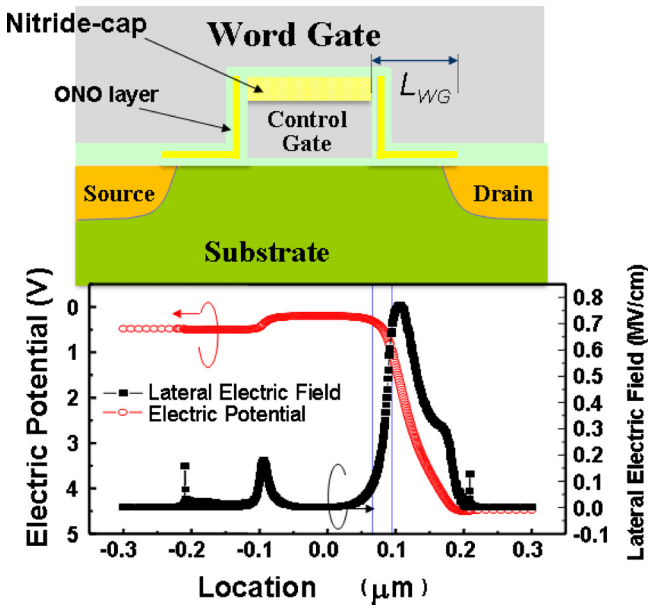

FIG. 1. (Color online) The device structure and the simulation results of the electric potential and lateral electric field under the programming conditions, V_G=10 V, V_{CG}=1 V, V_D=4 V, and V_B=0 V.

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TABLE I. The programming and erasing bias conditions used in this work.

Schemes	V_S	V_D (V)	V_G (V)	V_{CG} (V)	V_B (V)	Time
Program (SSI)	0	4	10	1	0	4 μs
Erase (BBHH)	Floating	6	−5	0	0	1 ms
Erase (STHH)	Floating	Floating	Floating	0	10	1 μs

Figure 2(a) shows the endurance by using SSI programming and band-to-band hot hole (BBHH) injection erasing operations. The erased state threshold voltage rolls up with the increasing number of P/E cycles. For a shorter word-gate length, the programmed electrons will be more close to the junction and holes being injected from the channel which will be more easily to recombine with these electrons. In comparison, for long word-gate length, the misalignment becomes worse since holes will be accumulated near the junction, repulsing the next hole injection and creating the electron accumulation in the channel so as to raise the erase state threshold voltage as shown in Fig. 2(a). The retention experiment, charge loss at 85 °C baking, is shown in Fig. 2(b). Since the program and erase operations are all the same for the three devices, we can assume that the bottom oxide of the three devices are equally damaged, that is, the vertical charge loss are almost the same for all three devices. Hence, the charge loss difference comes from the *lateral direction*. It was found that both the vertical and lateral charge loss coexist no matter what the word-gate length was used. At the programmed state, the accumulated holes migrate into the channel and cause a decrease in threshold voltage while at the erased state, it caused an increase in the threshold voltage. These came from the misalignment of electrons and holes as well as the migration of holes into the channel.

To solve the aforementioned misalignment issues, a substrate-transient hot hole (STHH) injection[13] erasing scheme has been proposed. Figure 3(a) shows the STHH erase set-up and the applying pulse is given in Fig. 3(b). During STHH erasing, the gate is grounded; the source and drain are kept floating while a pulse was applied to the substrate. From T_1 to T_2, source and drain are kept floating while a positive bias (V_{top}) is applied to the bulk, where source or drain-substrate junction capacitance is charged first (the junction is forward biased). As time goes from T_2 to T_3, the substrate bias immediately comes back to V_{base} while the floating drain cannot catch up but slowly recovered to the initial bias condition. Therefore, a large band bending occurs

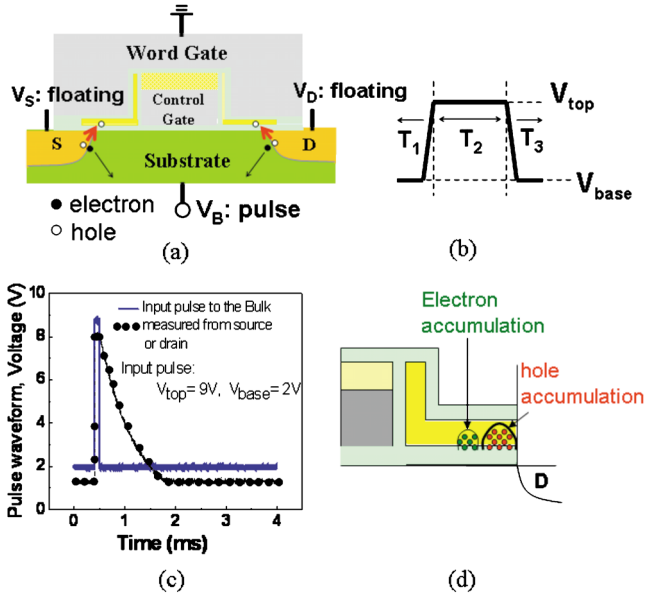

FIG. 3. (Color online) (a) The schematic set-up of the operating connections and (b) the input pulse waveform applying to the bulk, V_B. (c) The measured waveform (circles) from the source or drain terminal, under the applying pulse (solid line). (d) The respective locations of the injected electrons and holes under the word-gate region and near the drain, where the ONO storage layer is underneath the word-gate.

and generates hot holes to achieve erasing operation. The output (circles) is measured from the drain or source, in which the voltage difference of the input pulse to the bulk and the n+source/drain is the contact potential, V_{bi} (around 0.5 to 0.6 V) between the p-n+junctions. Also, in this figure, a change in the base voltage, V_{base}, the discharging transient will reach to the V_{base} value. Although the applied pulse width can be very short, microsecond or less, the real erasing time is the time for floating drain moving from $V_{top}-V_{bi}$ to $V_{base}-V_{bi}$, in a few minisecond, Fig. 3(c).

Based on the plot in Fig. 3(d), the holes are localized near the drain while electrons are located more close to the channel as a result of the programming and erasing schemes used. To show the efficacy of STHH injection of holes, Fig. 4 shows the endurance and the retention loss at 85 °C bake by using SSI programming and STHH erasing operation. The threshold voltages of the erase states are almost the same even after 10^4 P/E cycles. It reveals that less electron and hole accumulates in the channel and near the junction. Because the location of the hole profile generated by STHH is more deeply into the channel than BBHH, the holes can

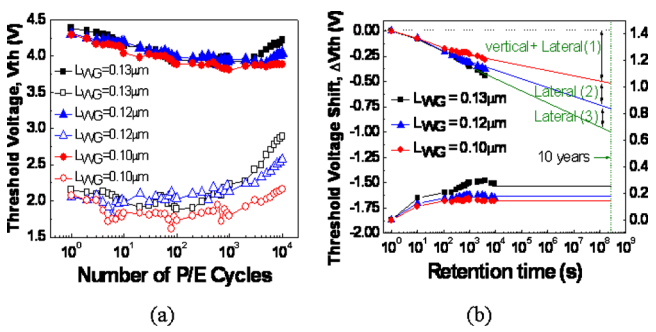

FIG. 2. (Color online) (a) The endurance and (b) the retention loss at 85 °C baking of the wrapped-gate device after 10^4 P/E cycles by using SSI programming and BBHH erasing with bias conditions listed in Table I.

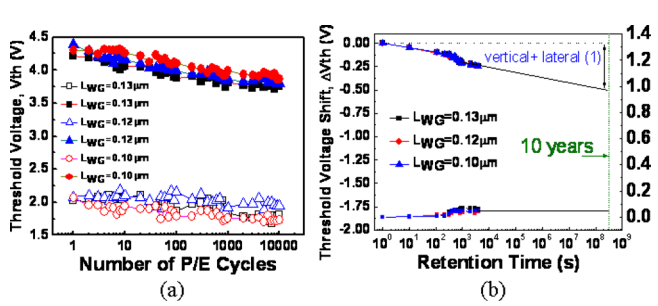

FIG. 4. (Color online) (a) The endurance and (b) the retention tests at 85 °C baking temperature of the wrapped-gate device after 10^4 P/E cycles by using SSI programming and STHH erasing with bias conditions listed in Table I.

completely eliminate the programmed electrons far from the junction and lead to better alignment of electrons and holes. Figure 4(b) shows that the retention loss is independent of the programming gate length which can be assumed that no accumulation holes and electrons were observed. Therefore, it inhibits the charge loss through the lateral direction, and the vertical charge loss is mainly caused by the cycling-induced traps after long term P/E cycles. Furthermore, the predicted 10-year lifetime retention test shows that window closure is much better by the using of STHH scheme.

In conclusion, the charge loss in a wrapped-gate SONOS cell includes both lateral and vertical directions. The vertical charge loss is mainly determined by the generated interface traps while the lateral charge loss is caused by the misalignment between electron and hole accumulations during P/E cycling. For the two-bit wrapped-gate SONOS, by altering the word-gate length to a suitable length, the lateral direction loss can be moderately improved. Besides, by utilizing SSI programming and STHH erasing schemes, proposed in this paper, a complete elimination of the misalignment along the lateral direction can be achieved which results in a better window closure for the ten year life-time test.

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