Statistical Simulation of Static Noise Margin Variability in Static Random Access Memory

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***Abstract*—In this paper, we examine the impact of random-dopant-fluctuation (RDF), process-variation-effect (PVE), and workfunction-fluctuation (WKF), on 16-nm-gate metal-oxide-semiconductor field-effect-transistor (MOSFET) static random access memory (SRAM) cells. For planar MOSFETs with a threshold voltage ($V_{\rm th}$) of 140 mV, the nominal static noise margin (SNM) of six-transistor (6T)-SRAM with unitary cell ratio (CR) is only 20 mV; and the normalized SNM fluctuations (SNM) induced by RDF, PVE, and WKF are 80%, 31%, and 48%, respectively, which may damage SRAM's operation. Two improvement approaches are further implemented; first, eight-transistor (8T)-SRAM and 6T-SRAM with increased CR are examined. Compared with the conventional 6T-SRAM, under the same $V_{\rm th}$, the SNM of 8T-SRAM is enlarged to 233 mV and the corresponding RDF, PVE, and WKF-induced SNM are reduced to 9.5%, 6.4%, and 7%, respectively, at a cost of 30% extra chip area. Without increasing chip area, device with raised $V_{\rm th}$, doping profile engineering and using silicon-on-insulator fin-type field-effect transistors (SOI FinFETs) are further advanced. The 6T SOI FinFETs SRAM exhibits the smallest σSNM, with merely 5.3%, 1.2%, and 2.3%, resulting from RDF, PVE, and WKF, respectively, where the value of SNM is equal to 125 mV.**

***Index Terms*—Eight-transistor (8T), electrical characteristic, fin-type field-effect transistors (FinFET), fluctuation, metal-oxide-semiconductor field-effect-transistor (MOSFET), planar, process variation, random dopant, silicon-on-insulator (SOI), six-transistor (6T), static noise margin (SNM), static random access memory (SRAM), workfunction fluctuation.**

I. Introduction

THE MINIMUM feature size of metal-oxide-semiconductor field-effect transistors (MOSFETs) has been rapidly scaled down, the threshold voltage ($V_{\rm th}$) fluctuation is decided and becomes crucial for the design window and manufacturing yield of ultralarge-scale integration circuits [1]–[4]. Fluctuations of short-channel effects (SCEs) resulting from process-variation-induced gate-length deviation and line-edge roughness are growing worse due to serious SCEs when the dimension of device is further scaled [5], [6]. Second, the random nature of discrete dopants results in significantly random fluctuation. Such random-dopant-induced fluctuations are unpredictable due to the number and location of dopant atoms in the channel region; fluctuation-related issues in devices and circuits including suppression technologies have been studied [5], [7]–[16]. Among these suppression technologies, high-κ/metal gate technologies are known useful for device scaling and fluctuation reduction. However, the usage of metals as gate electrode introduces another variation source due to the dependence of workfunction on the orientation of metal grains [17], [18]. The sources of variation above limit the performance, yield, and functionality due to significant component mismatch in area constrained circuits, such as static random access memory (SRAM). Generally, a SRAM cell is operated in three different states: standby, write, and read; owing to the cell is most vulnerable to noise during read operation [3], [4], the stability of a SRAM cell is often related to the static noise margin (SNM). The SNM is defined as the maximum dc noise voltage tolerance to avoid the cell state been flipped during a read access [4]. Recent studies have been reported on the effect of random-dopant-induced characteristic fluctuation in SRAM circuits using compact modeling approach [1]–[4], [19], [20]. Unfortunately, such approach does not take the random-dopant-position-induced fluctuation [21] and the metal grain orientations into consideration yet, which may lead to sizeable difference in estimation device and SRAM characteristics. Thus, a unified simulation analysis including the three aforementioned variations may provide interesting engineering findings for SRAM fabrication.

In this paper, an experimentally validated 3-D "atomistic" coupled device-circuit simulation approach is employed to analyze the process-variation, random-dopant, and workfunction-variation-induced characteristic fluctuations in 16-nm-gate six-transistor (6T) and eight-transistor (8T)-SRAM circuits [22]. Based on the statistically generated large-scale 'atomistic' doping profile, 3-D device simulation is performed by solving a set of 3-D drift-diffusion equations with quantum corrections by the density gradient method under our parallel computing system [23], [24].

To consider more rich physical insight of device and pursue the best accuracy in estimation of the characteristic fluctuation in SRAM circuit, a coupled device-circuit simulation [7], [9],

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[21], [25] is performed. The impact of intrinsic parameter fluctuation consisting of random-dopant-fluctuation (RDF), process-variation-effect (PVE), and workfunction-fluctuation (WKF) and associated suppression approaches are investigated under this analyzing scenario. Notably, the accuracy of developed technique has been quantitatively verified in the experimentally measured characteristics of sub-20-nm devices [10].

This paper is organized as follows. In Section II, we state the analyzing technique for studying the effect of aforementioned intrinsic parameter fluctuations on characteristics of device and SRAM circuit. In Section III, we first examine the impacts of intrinsic parameter fluctuations on SRAM cells. Then, suppression approaches, based upon the circuit and device viewpoints, are implemented to examine the associated stabilities. Finally, we draw conclusions and suggest future work of this paper.

II. Simulation Methodology

The nominal channel doping concentration of the studied n-type MOSFET (NMOS) devices is with $1.48 \times 10^{18}\text{cm}^{-3}$ in this paper; we note that the nominal channel doping concentration was empirically adopted from experimental data [10]. They have a SiO_2 gate-oxide thickness of 1.2 nm and a TiN gate with workfunction of 4.4 eV. To estimate RDF-induced characteristic fluctuation starting from 65-nm-gate devices, we first consider the randomness of the number and position of discrete channel dopants. 12 500 dopants are randomly generated in a large cube (325 nm × 325 nm × 80 nm), in which the equivalent doping concentration is $1.48 \times 10^{18}\text{cm}^{-3}$, which is rounded off to the 2nd decimal place of $1.4793 \times 10^{18}\text{cm}^{-3}$, as shown in Fig. 1(a). The large cube is then partitioned into 125 sub-cubes of (65 nm × 65 nm × 16 nm). The number of dopants may vary from 70 to 130, where the average number is 100, as shown in Fig. 1(b) and (c), respectively. These sub-cubes are equivalently mapped into the device channel for the 3-D "atomistic" device simulation with discrete dopants, as shown in Fig. 1(d). Similarly, we can generate the sets of discrete dopant cases for the 32-nm and 16-nm-gate transistors as shown in Fig. 1(e) and (f), respectively. In Fig. 1(g), we apply the statistical approach to evaluate the effect of PVE, in which the magnitude of the gate length deviation and the line edge roughness mainly follows the projections of the ITRS roadmap [26]. The three-sigma (3σ) of the process-variation-induced gate length deviation and line edge roughness is 1.5 nm and 4.3 nm for the 16-nm and 65-nm devices, respectively. The V_{th} roll-off is adopted to estimate the PVE-induced V_{th} fluctuation. For WKF, considering the size of metal grains and the gate area of the devices, the device gate area is composed of a small number of grains as shown in Fig. 1(h). Since each grain orientation has different workfunction, the gate workfunction is modeled as a probabilistic distribution rather than a deterministic value. Therefore, a statistically sound Monte-Carlo approach is advanced for examining such distribution. The gate area is partitioned into several parts according to the average grain size. The gate areas are (65 nm × 65 nm), (32 nm × 32 nm), and (16 nm × 16 nm) for 65-nm, 32-nm, and 16-nm gate planar devices, respectively. Then, the grain orientation of each part and total gate workfunction are estimated based on the properties of used metals, as shown in Fig. 1(i) [18]. Notably, in "atomistic" device simulation, the resolution of individual charges within a conventional drift-diffusion simulation using a fine mesh creates problems associated with singularities in the Coulomb potential [27], [28]. The potential becomes too steep with fine mesh, and therefore, the majority carriers are nonphysically trapped by ionized impurities, and the mobile carrier density is reduced. Thus, the density-gradient approximation is used to handle discrete charges by properly introducing related quantum–mechanical effects, and coupled with Poisson equation as well as electron-hole current continuity equations [29], [30].

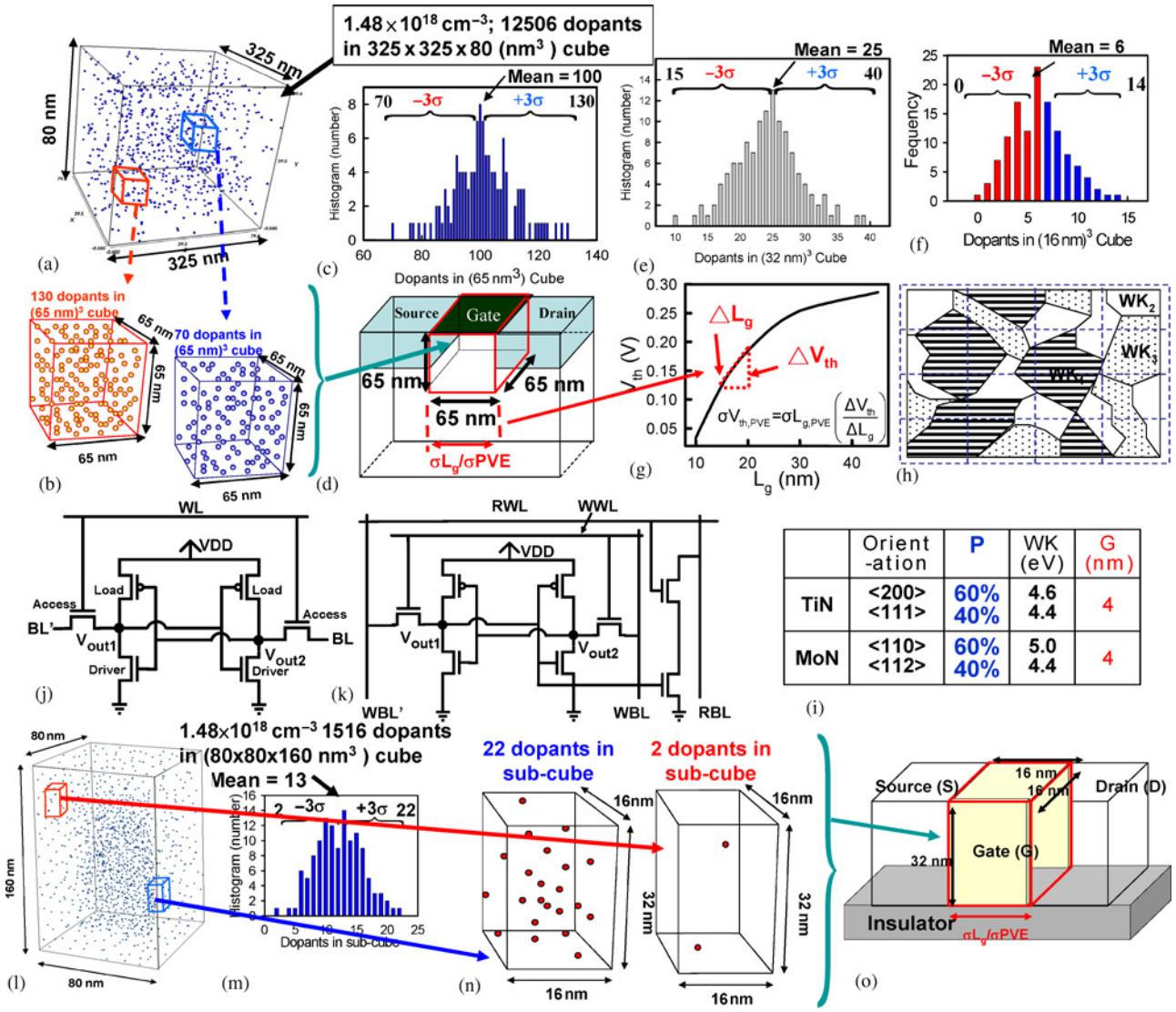
Fig. 1(j) and (k) illustrates the explored 6T and 8T-SRAM cells, respectively. All cell ratios [CR, $\text{CR} = ((W/L)_{\text{driver\_transistor}})/((W/L)_{\text{access\_transistor}})$] of the SRAM cells in this paper are first set as unitary. The applied voltages of 16 nm and 65 nm devices are 1.0 V and 1.2 V, respectively, according to the projections of the ITRS roadmap [26]. Due to the nominal value of the SNM with different device setting are different, the absolute value of SNM fluctuation is here normalized for a fair comparison purpose. We use the normalized SNM fluctuation (σ_{SNM}) to assess the transfer characteristic fluctuation of SRAM. All physical models and accuracy of such large-scale simulation approach are quantitatively calibrated by experimentally measured results [10]. Similarly, we do generate discrete-dopant-fluctuated cases for p-type MOSFET (PMOS) through the flow of Fig. 1(a)–(f). Then, we randomly select those fluctuated NMOS and PMOS devices for the following examinations. In order to estimate SRAM characteristics with ultrasmall nanoscale transistors, instead of compact model approach [1]–[4], [19], [20], a device-circuit coupled simulation [7], [9], [21] is employed. The characteristics of devices of SRAM circuit are first estimated by solving the 3-D device transport equations, and are used as initial guesses in the successively coupled device-circuit simulation. The SRAMs circuit nodal equations are formulated, according to the current and voltage conservation laws, and directly coupled to the 3-D device transport equations (in the form of a large matrix containing the circuit and device equations), which are solved simultaneously to obtain the circuit characteristics [7], [9], [21].

III. Results and Discussion

In this section, the intrinsic-parameter-induced characteristic fluctuations of NMOS and PMOS, from 65 nm to 16 nm, in 6T-SRAM cells are first explored. Then, we discuss the transfer characteristic including its stability for the tested SRAM cells. Fluctuation suppression techniques based on circuits and device viewpoints are presented and discussed.

A. Intrinsic Parameter Fluctuations

Fig. 2 shows the RDF, PVE, and WKF-induced V_{th} fluctuations of 65-nm, 32-nm, and 16-nm-gate NMOSs. The roll-off of the nominal threshold voltage follows the gate length decreased, where the nominal V_{th} for 16-nm, 32-nm, and 65-nm-gate devices are 140 mV, 220 mV, and 280 mV,



	Orient -ation	P	WK (eV)	G (nm)
TiN	<200> <111>	60% 40%	4.6 4.4	4
MoN	<110> <112>	60% 40%	5.0 4.4	4

Fig. 1. (a) Discrete dopants randomly distributed in the large cube with the average concentration of $1.48 \times 10^{18}\text{cm}^{-3}$. (b) and (c) There are 12 506 dopants within the cube, for 65-nm-gate devices, dopants may vary from 70 to 130 (average = 100), within its sub-cubes of 65 nm × 65 nm × 16 nm. (d) Sub-cubes are equivalently mapped into channel region for discrete dopant simulation as shown in MOSFET. (e) Dopants may vary from 10 to 40 (average = 25) for 32-nm-gate devices and (f) 0 to 14 (average = 6) for 16-nm-gate devices. (g) V_{th} roll-off characteristics is applied to estimate the process-variation-effect-induced V_{th} fluctuation, where the gate length variation follows the projections of the International Technology Roadmap for Semiconductors (ITRS). (h) Gate area is partitioned into several parts according to the properties of metal material as shown in (i), workfunction of each part is assumed to be a random value to estimate workfunction-induced fluctuation. The schematics of (j) 6T and (k) 8T-SRAM cells. (l) Similarly, discrete dopants randomly distribute in a large cuboid, then partition into sub-cubes of 16 nm × 16 nm × 32 nm, dopants may vary from [(m) and (n)] 2 to 23 (average = 13). (o) The sub-cubes are equivalently mapped into channel region of SOI FinFET.

respectively. Be assuming the statistical independency of the fluctuation variables, the total V_{th} fluctuation ($\sigma V_{\text{th,total}}$) could be approximated by

$$\left(\sigma V_{\text{th,total}}\right)^2 \approx \left(\sigma V_{\text{th,RDF}}\right)^2 + \left(\sigma V_{\text{th,PVE}}\right)^2 + \left(\sigma V_{\text{th,WKF}}\right)^2 \quad (1)$$

where $\sigma V_{\text{th,RDF}}$, $\sigma V_{\text{th,PVE}}$, and $\sigma V_{\text{th,WKF}}$ are RDF, PVE, and WKF-induced threshold voltage fluctuations, respectively. As the gate length scales from 65 nm to 16 nm, the total V_{th} fluctuation increases significantly from 18 mV to 68 mV. The V_{th} fluctuation of 16 nm MOSFET is around 4× larger than that of 65 nm, which follows the trend of the analytical model

$$\sigma V_{\text{th,RDF}} = 3.19 \times 10^{-8} \frac{t_{\text{ox}} N_A^{0.401}}{\sqrt{WL}} \quad (2)$$

where t_{ox} is the thickness of gate oxide, W and L are the width and length of transistor [21]. Additionally, as shown in Fig. 2, the RDF dominates the total V_{th} fluctuation in the explored device dimensions, which may result in critical issue of stability. Fig. 3 shows the static transfer characteristics of 65 nm planar SRAM cells, where the dashed lines represent intrinsic-parameter-fluctuated curves, and the solid line stands for the nominal curve. The nominal SNM for the 65 nm planar MOSFET SRAM is 138 mV. Since the RDF induces the largest

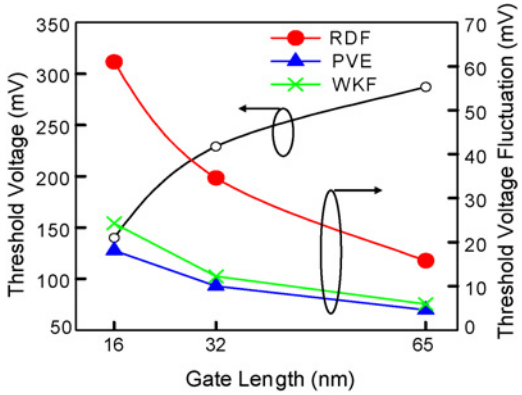


Fig. 2. Plot of V_{th} and V_{th} fluctuations induced by RDF, PVE, and WKF for different gate lengths of NMOS devices.

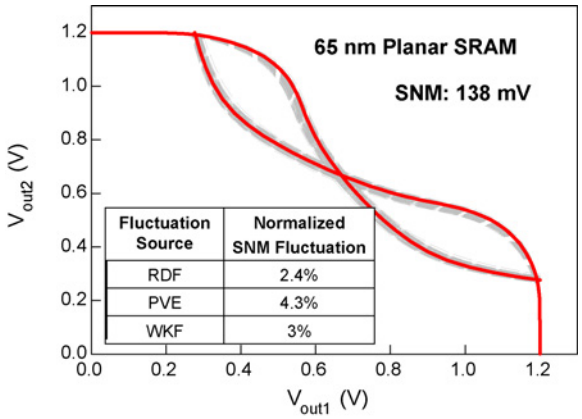


Fig. 3. Nominal and fluctuated static transfer characteristic curves of 65 nm planar 6T-SRAM cells. The inset shows the normalized SNM fluctuations induced by RDF, PVE, and WKF, respectively.

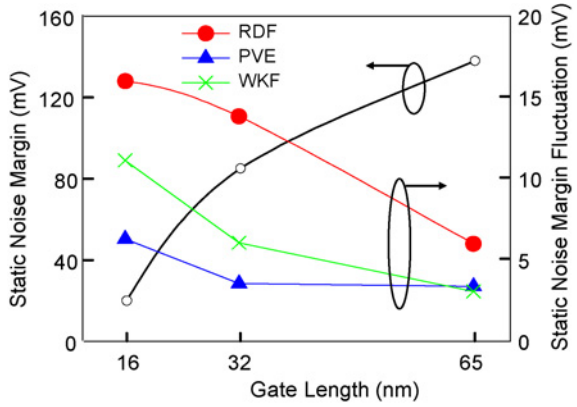


Fig. 4. Plot of SNM and SNM fluctuations that are induced by RDF, PVE, and WKF for different gate lengths of SRAM cells.

variability in the threshold voltage, the s_{SNM} of SRAM is dominated by RDF. The RDF, PVE, and WKF-induced σ_{SNM} are also summarized in inset of Fig. 3, the σ_{SNM} induced by RDF, PVE, and WKF are 4.3%, 3%, and 2.4%, respectively. Fig. 4 shows the roll-off characteristic of SNM and the SNM fluctuation of SRAM cells with different device gate length. As the gate length scales from 65 nm to 16 nm, the SNM decreases significantly from 138 mV to 20 mV. Notably, in calculating the SNM fluctuation, once a SRAM cell is destructive read, its SNM is set then as zero. Among fluctuations, the RDF is the most critical issue in improving stability of SRAM. Fig. 5 summarized the normalized SNM fluctuations for 65-nm, 32-nm, and 16-nm-gate SRAM. As the gate length of device, scaling from 65 nm to 16 nm, the RDF-induced σ_{SNM} increases from 4.3% to 80% which strongly depends on the dimension of transistors. Although shrinking device size can increase the density of memory, the decreased SNM and increased SNM fluctuation are crucial issues for SRAM with such small devices.

Since the SNM of 6T-SRAM, for device with V_{th} = 140 mV and unitary CR, is 20 mV with 80%, 31%, and 48% normalized SNM fluctuations induced by RDF, PVE, and WKF, respectively, which could not ensure correct operation of SRAM, different characteristic improvement approaches, from circuit and device viewpoints, are thus examined for the 16-nm-gate SRAM cells.

B. Circuit Level Improvement

Besides conventional 6T architecture, the main purpose of 8T-SRAM is to eliminate the impact of bit line to stored data during read operation by separating the data retention and data output elements. Unlike the 6T-SRAM, the access transistors of 8T-SRAM are turned off when data reading and the data will be gathered through the additional two transistors. This mechanism can avoid direct flow between the bit line and the stored data and then increase the noise margin. Fig. 6(a) shows the static transfer characteristics of 8T-SRAM cells of RDF-fluctuated cases, where the V_{th} of device is 140 mV. Due to the separation of data access element, the influence of bit-line is reduced; and thus the nominal SNM is increased to 233 mV. The RDF-induced SNM fluctuation is 22 mV, which is merely within 10% variation. The value of SNM is 12 times larger than that of conventional 6T-SRAM cell and the RDF-induced σ_{SNM} is suppressed by a factor of 8.4. We note that the 8T-SRAM can enlarge the SNM and reduce σ_{SNM}, but the chip area is increased by 30%. We further conduct, as shown in Fig. 6(b), the comparison of the SNM and σ_{SNM} for both the 8T-SRAM and the conventional 6T-SRAM with CR = 2. Similar to the 8T-SRAM, the 6T-SRAM with CR = 2 also requires 30% extra chip area. Nevertheless, as shown in Fig. 6(b), the SNM of 6T-SRAM with CR = 2 is 84 mV and RDF, PVE, and WKF-induced SNM fluctuations are about 20%, 13%, and 16%, respectively. Due to the functional limitation during read operation, the extra requirement of chip area, by increasing CR of the 6T-SRAM, does not bring significant improvement in a cost-effective manner, compared with the 8T-SRAM.

C. Device Level Improvement

Fig. 7 shows the static transfer curve of the 16-nm-gate planar 6T-SRAM with V_{th} = 350 mV. The SNM is increased to 92 mV and the normalized SNM fluctuations that induced by RDF, PVE, and WKF are reduced to 41%, 18%, and 29%, respectively. Since the σ_{SNM} are still too large to ensure the accurate operation of the SRAM cell, to further

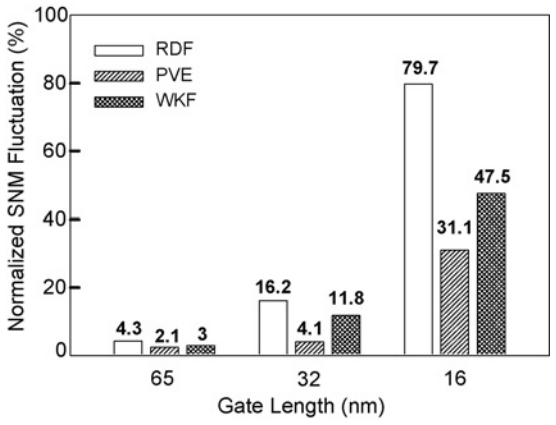


Fig. 5. RDF, PVE, and WKF-induced normalized SNM fluctuations for 16 nm to 65 nm planar MOSFET SRAM cells.

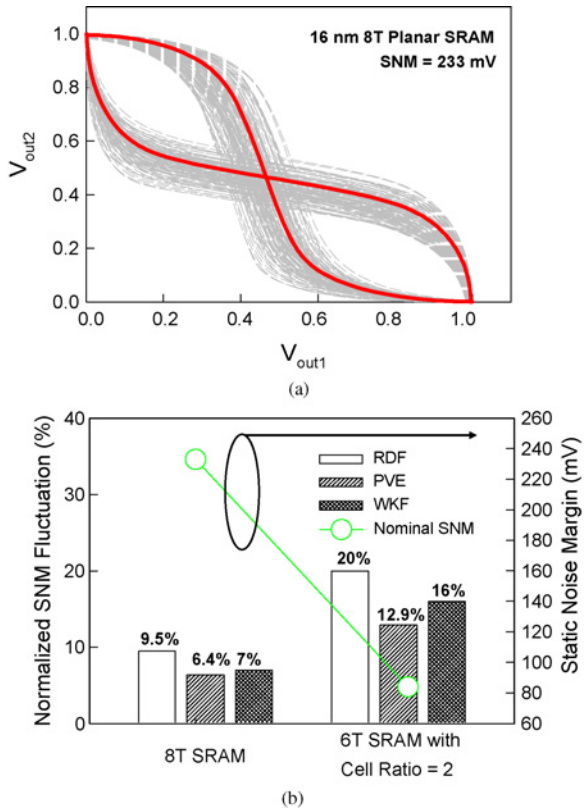


Fig. 6. (a) Static transfer characteristics of planar 8T-SRAM cells. (b) Comparison of characteristic fluctuations between the 8T-SRAM and the 6T-SRAM with a CR of two.

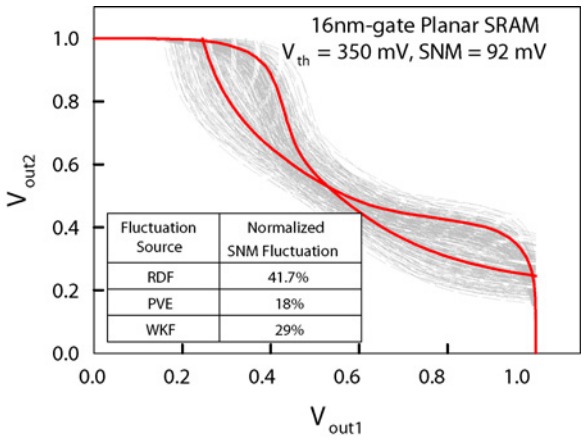


Fig. 7. Static transfer characteristics of improved 6T-SRAM cells, the threshold voltage of devices were raised to 350 mV.

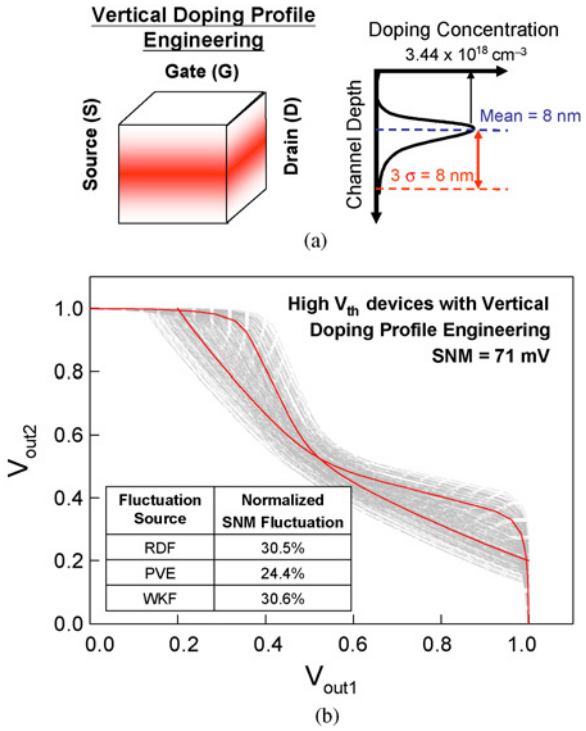


Fig. 8. (a) Illustration of the vertical doping profile from the surface to substrate which follows a normal distribution. (b) Normalized RDF, PVE, and WKF-induced fluctuations for 16-nm planar SRAM with high-V_{th} devices using the vertical doping profile.

suppress the RDF-induced SNM fluctuation, vertical doping profile engineering, as shown in Fig. 8(a) is implemented to reduce the RDF-induced characteristic fluctuation. The aim of vertical doping profile engineering is to control fewer dopants near the current conducting path to suppress RDF-induced characteristic fluctuations. Fig. 8(b) shows the static transfer characteristics of 16 nm planar SRAM with high-V_{th} devices using vertical doping profile. The result shows that vertical doping profile engineering can further suppress RDF-induced σ_{SNM} from 41.7% to 30.5%; however, it also suffers from more serious SCEs, which reduces the value of SNM to 71 mV. Additionally, the PVE-induced σ_{SNM} is increased from 18% to 24.4%.

Though the usage of high-V_{th} and vertical doping profile engineering can enlarge the SNM and reduce σ_{SNM}. The increased V_{th} also reduce the write noise margin and slow down the operation speed. Therefore, based on the same layout area as 16-nm-gate planar MOSFETs, 16-nm-gate silicon-on-insulator fin-type field-effect transistors (SOI FinFETs) with an aspect ratio (defined by the fin height/the fin width) of two is then adopted to replace the planar MOSFETs to examine the associated fluctuation resistivity against intrinsic parameter fluctuation. Without loss of generality, the equivalent doping

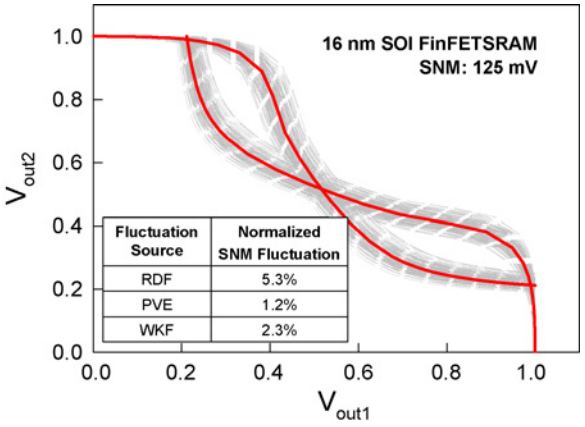


Fig. 9. Nominal and fluctuated static transfer characteristic curves of 16-nm SOI FinFET SRAM cells.

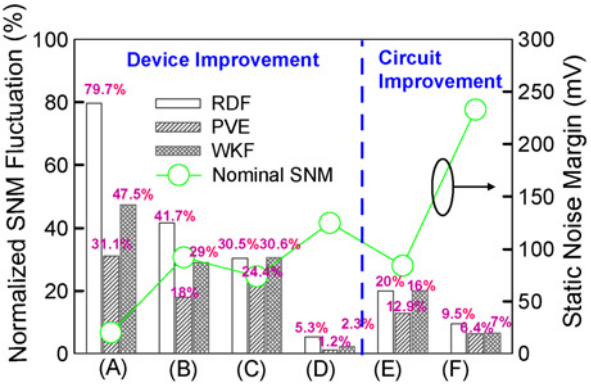


Fig. 10. Summary of intrinsic-parameter-induced normalized SNM fluctuation and nominal SNM for different improvement techniques. (a)–(c) Planar 6T-SRAM with (a) CR = 1, (b) raised V_{th}, and (c) both raised V_{th} and doping-profile-engineering. (d) 6T SOI FinFET SRAM. (e) Planar 6T-SRAM with CR = 2. (f) Planar 8T-SRAM.

concentration is equal to $1.48 \times 10^{18}\text{cm}^{-3}$. Thus, 1516 dopants are generated in a large cube (80 nm × 80 nm × 160 nm) and partitioned into sub-cubes (16 nm × 16 nm × 32 nm), as shown in Fig. 1(l) and (n), respectively. The number of dopants in a sub-cube may vary from 2 to 24, and the average is 13, as shown in Fig. 1(m). These sub-cubes are equivalently mapped into the 16-nm-gate SOI FinFET, as shown in Fig. 1(o). To compare the device characteristics on a fair basis, the nominal threshold voltages of SOI FinFETs are calibrated to 140 mV, which is the same threshold voltage as in the original cases. The RDF, PVE, and WKF-induced threshold voltage fluctuations are 42.2 mV, 8.3 mV, and 17 mV, in which the threshold voltage fluctuations are suppressed, compared with the original device. The improved channel controllability reduces the effects of RDF, PVE, and WKF; similarly, the RDF-induced variation still plays the major source in device characteristic fluctuations. Fig. 9 shows the static transfer characteristics of the 16 nm SOI FinFET SRAM cell, where dashed lines illustrated fluctuated curves and the solid line is the nominal curve. The nominal SNM is 125 mV and RDF, PVE, and WKF-induced fluctuations are aggressively suppressed to 5.2%, 1.2%, and 2.3%, respectively. The improved nominal SNM is due to the SOI-FinFETs having larger transconductance than that of planar MOSFETs under the same V_{th}. A relation between transconductance and SNM [3] is given by

$$\text{SNM} \propto \sqrt{1 - \frac{I_{\text{nx}}}{g_{\text{m,pmos}}}} - \frac{I_{\text{ax}}}{g_{\text{m,nmos}}} \tag{3}$$

where the I_{nx} is the saturation drain current of the driver transistor and I_{ax} is the saturation drain current of the access transistor. Consequently, the SNM increases when the transconductance increases. Therefore, even the SOI FinFETs is with a low-threshold voltage, 140 mV, as planar MOSFETs, the large transconductance still can provide sufficiently large SNM for circuit operation.

As shown in Fig. 10, we compare the aforementioned improvement techniques, based upon the device and circuit viewpoints, in which (a)–(c) represents the planar 6T-SRAM cells with (a) CR = 1, (b) raised V_{th}, and (c) raised V_{th} case with doping-profile-engineering. Fig. 10(d) is the 6T SOI FinFET SRAM, Fig. 10(e) is planar 6T-SRAM with CR = 2 and Fig. 10(f) is planar 8T-SRAM. Fig. 10(e) and (f) are developed from the circuit design viewpoint, in which 30% extra chip area are required. The 8T-SRAM exhibits interesting SNM and σ_{SNM} because of the turn-off of the access transistors in 8T-SRAM when data reading. For planar MOSFETs with V_{th} = 140 mV, the SNM could be enlarged to 233 mV and the σ_{SNM} is reduced to 9.5%. The circuit improvement approach can provide large SNM and is without changing the fabrication process. Therefore, 8T architecture could be considered for SRAM design with a compromise between performance and chip density. To keep a minimal chip area comparable with the conventional planar 6T-SRAM, the design approach from device engineering has to be developed. By adjusting the V_{th} to 350 mV, the SNM of the planar 6T-SRAM can be enhanced to 92 mV with 41.7% σ_{SNM}. Using doping profile engineering can further reduce the RDF-induced σ_{SNM} to 30.5%. However, the SNM is reduced to 71 mV because of the serious SCEs. To have a large SNM with sufficient small σ_{SNM}, the explored SOI FinFETs 6T-SRAM exhibits a sufficiently large SNM (125 mV) with 5.4% σ_{SNM}.

IV. Conclusion

In this paper, an experimentally validated 3-D "atomistic" coupled device-circuit simulation approach has been advanced to investigate the dependence of intrinsic parameter fluctuations in nanoscale SRAM cell. The roll-off characteristics of 6T-SRAM from 65-nm to 16-nm-gate have been examined, in which the domination source of variation, RDF, has been found. Additionally, the reduced SNM from 138 mV to 20 mV and enlarged SNM fluctuation from 4% to 80% implies the importance of suppression RDF fluctuation in SRAM circuit. To improve the reduced SNM and large σ_{SNM} in 16-nm-gate 6T-SRAM, approaches proposed from circuit and device design were presented. From the time-to-market viewpoint, the circuit-level improvement of 8T-SRAM could be considered at a cost of 30% extra chip area. To further increase the chip density, the device engineering is necessary. The techniques

of raise of device V_{th} and doping profile engineering can increase SNM and reduce σ_{SNM}, respectively. However, there is a trade-off between these two techniques because of the degraded speed and serious short channel effects, respectively. Hence, based on the same layout area, the use of SOI FinFETs in 6T-SRAM has been further examined. The SNM of 6T SOI FinFETs SRAM is 125 mV and the normalized SNM fluctuation induced by RDF, PVE, and WKF are suppressed significantly to 5.4%, 1.2%, and 2.3%, respectively. We are currently deriving closed form equations of the aforementioned fluctuations for circuit simulation of large size of SRAM cells.

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