Microelectronic Engineering 87 (2010) 2253–2257

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Improvement on the noise performance of InAs-based HEMTs with gate sinking technology

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ARTICLE INFO

Article history:
Received 26 September 2009
Received in revised form 22 January 2010
Accepted 21 February 2010
Available online 26 February 2010

Keywords:
Buried gate
High-electron mobility transistor (HEMT)
InAs
InGaAs

ABSTRACT

Improvement on the RF and noise performance for 80 nm InAs/$In_{0.7}Ga_{0.3}As$ high-electron mobility transistor (HEMT) through gate sinking technology is presented. After gate sinking at 250 °C for 3 min, the device exhibited a high transconductance of 1900 mS/mm at a drain bias of 0.5 V with 1066 mA/mm drain–source saturation current. A current-gain cutoff frequency (f_T) of 113 GHz and a maximum oscillation frequency (f_{max}) of 110 GHz were achieved at extremely low drain bias of 0.1 V. The 0.08 × 40 μm^2 device with gate sinking demonstrated 0.82 dB minimum noise figure and 14 dB associated gain at 17 GHz with only 1.14 mW DC power consumption. Significant improvement in RF and noise performance was mainly attributed to the reduction of gate-to-channel distance together with the parasitic source resistance through gate sinking technology.

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1. Introduction

Ultra-low power, high performance low noise amplifiers are critical components for many commercial and military system applications such as wireless LANs, space-based radars, mobile millimeter-wave communications and handheld imagers [1–3]. In addition to noise figure and gain, low DC power consumption is always desired for large-scale array applications since prime power is limited in such systems.

Among all the possible technologies to meet the stringent system requirements, antimonide-based compound semiconductor (ABCS) InAs/AlSb high-electron mobility transistors (HEMTs) are promising because of the very high-electron mobility and peak velocity [4]. Nevertheless, the ability of ABCS HEMTs operating at low drain bias has been successfully demonstrated [4]. Besides ABCS HEMTs, high indium content InP-based InAs/$In_{1-x}Ga_xAs$ composite channel HEMTs featuring high sheet electron densities has been attractive [5–7]. Research effort has been devoted to the reduction of the gate-to-channel distance and optimum design of epitaxial structure for performance improvement [8]. Recently, world-record f_T of 628 GHz was reported using 30 nm InAs/$In_{0.53}Ga_{0.47}As$ channel HEMTs [9].

High-electron mobility and conductivity are essential for devices to maintain excellent RF performance with extreme low DC power consumption [10,11]. Additionally, gate-recess structure plays a critical role in the high-frequency and noise performance for such devices. In general, the transconductance (g_m) of the device is mainly influenced by the gate-to-channel distance, and the reduction of which can effectively increase the f_T due to the enhancement of average electron velocity underneath the gate electrode.

Another key factor that may have impact on the device performance is the shape of the recessed region since it directly affects the corresponding parasitic resistances (R_s and R_d) and capacitances (C_{GS} and C_{GD}). Furthermore, such shape also modulates the electric field in the channel. Shinohara et al. [12] reported the f_T value of 547 GHz in 30 nm-gate pseudomorphic HEMTs by means of multilayer cap structure to reduce parasitic source and drain resistances. Matsuzaki et al. [13] have employed tiered-edge ohmic structure and low-k benzocyclobutene passivation to effectively minimize parasitic gate capacitance and achieve relatively high g_m and f_T values. Although the results seemed promising, yet relatively complicated fabrication processes were involved. As for the noise figure, reduction of the gate length (L_g) and parasitic resistances is the key to achieve extremely low noise figure of the devices. While reduction of gate length seems to be a good approach, limitation of such approach lies mainly in the degradation on performance caused by the short-channel effect. Thus, care must be taken in obtaining the optimum physical parameters of devices for such applications [6].

Pt-based gate sinking technology has been widely applied in the fabrication of HEMTs since it provides a possible solution which enables vertical scaling of gate-to-channel distance without increasing the access resistance. Meanwhile, the short-channel effect can also be minimized through proper adjustment of the

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doi:10.1016/j.mee.2010.02.012

length of side recess [14]. Another advantage of using Pt-based structure is the relatively larger Schottky barrier height which in turn suppresses gate leakage currents. Thus, superior device performance can be achieved through a very simple and straightforward fabrication process with optimal epitaxial structure.

In this paper, fabrication and complete characterization of 80 nm InAs/$In_{0.7}Ga_{0.3}As$ composite channel HEMTs using Pt-buried gate technique are presented. Major device figure of merits including g_m, f_T, and minimum noise figure (NF_{min}) are compared against the devices without gate sinking for the first time. Measurement results revealed that the devices with gate sinking achieved higher g_m and f_T with lower NF_{min} at extremely low DC power consumption levels. Comparison of the device performance against state-of-the-art ABCS HEMTs with equivalent gate length has also been made. The excellent performance has made InP-based InAs HEMT technology a potential candidate for future low-power high-frequency applications.

2. Device fabrication

The HEMT structure used $In_xAl_{1-x}As$ as the buffer layer and was grown by molecular beam epitaxy (MBE) method on a 2-in InP substrate. The epitaxial structure of the device is shown in Fig. 1. A 50-Å InAs channel layer with 20-Å $In_{0.7}Ga_{0.3}As$ upper sub-channel and 30-Å $In_{0.7}Ga_{0.3}As$ lower sub-channel was grown on top of the 500-nm-thick InAlAs buffer layer. The $In_{0.7}Ga_{0.3}As$ sub-channels were applied to enhance the electron confinement in the thin InAs layer and improve the electron transport properties [15]. On top of the channel, the HEMT layers consist of a 40-Å-thick InAlAs spacer, a Si-δ-doping with 5×10^{12} cm^{-2}, a 10-nm-thick InAlAs barrier, a 4-nm-thick InP etching stop, and a 35-nm-thick InGaAs cap layer with 2×10^{18} cm^{-3} Si-doping. The two-dimensional electron gas (2DEG) density and electron mobility of the as-grown material were measured to be 4.34×10^{12} cm^{-2} and 12,000 cm^2/V s at room temperature, respectively.

For the device fabrication, the active area of the device was isolated by wet etching. The ohmic contacts were formed with 3-μm source–drain spacing by evaporating Au/Ge/Ni/Au on heavily doped *n*-InGaAs cap layer and then alloyed at 250 °C for 25 s to attain low contact resistance (R_c). The T-shaped gate was processed using the 50-kV JEOL electron beam lithography system (JBX 6000 FS) with trilayer e-beam resist. Succinic acid/H_2O_2/NH_4OH solution was used for gate recess, and then, Pt (12 nm)/Ti (60 nm)/Pt (80 nm)/Au (180 nm) were deposited as Schottky gate metal and lifted off by ZDMAC to form the 80-nm T-shaped gate. A 100-nm-thick silicon nitride was deposited as a passivation layer by plasma-enhanced chemical vapor deposition at 250 °C for 10 min. Finally, thermal annealing at 250 °C for 3 min in forming gas ambient was carried out for gate sinking to further recess the channel. The contact resistance was 0.032 Ω mm after gate-sinking process, which remained almost unchanged as compared with that of 0.021 Ω mm before annealing. The estimated gate-to-channel distance after gate sinking was 8 nm.

3. Device performance

Fig. 2 shows the DC *I–V* characteristics of the 2 × 20 μm devices with and without gate sinking. A very high drain current density of 1066 mA/mm for device with gate sinking was achieved compared to that of 789 mA/mm for device without gate sinking at V_{DS} = 0.5 V. This high current is mainly due to the superior electron mobility in the composite channel and the non-degrading performance of the ohmic contact during gate annealing. A shift in threshold voltage from −0.94 V for device (without sinking) to −0.82 V for device (with sinking) was observed. Meanwhile, the gate–drain breakdown voltage ($V_{DG,BR}$) decreased from 3.6 V (without sinking) to 2.4 V (with sinking), which is mainly due to the reduction in the Schottky barrier thickness after the gate-sinking process.

The transconductance g_m plotted as a function of V_{GS} for devices with and without gate sinking is shown in Fig. 3a. As is observed, the peak g_m value increased from 1430 ms/mm (without sinking) to 1900 ms/mm (with sinking) under the same drain bias (V_{DS}) of 0.5 V. The increase is mainly due to the sinking of Pt atoms into the InP etching stop layer which in turn shifted the gate metal front closer to the two-dimensional electron gas channel. Fig. 3b shows g_m as a function of V_{GS} for devices with gate sinking under various drain biases. It is obvious that nice peak g_m values are maintained at very low drain biases. Care must be taken in the biasing of such devices with very small energy bandgap since impact ionization phenomenon would occur at high drain bias level which in turn causes serious performance degradation.

For characterization of RF performance, the *S* parameters of the device were measured from 5 to 80 GHz using on-wafer probing system with HP8510XF network analyzer. Standard load-reflection–reflection-match (LRRM) calibration method was adopted to calibrate the measurement system and the reference planes of cal-

Cap	n In_xGaAs, x = 0.53
Etch stop layer	InP
Barrier	i In_xAlAs, x = 0.52
δ doping	Si
Barrier	i In_xAlAs, x = 0.52
Channel	In_xGaAs, x = 0.7
Channel	InAs
Channel	In_xGaAs, x = 0.7
Buffer	i In_xAlAs, x = 0.52
2 Inch S. I. InP Substrate	

Fig. 1. The epitaxial structure of the 80 nm InAs/$In_{0.7}Ga_{0.3}As$ HEMT device.

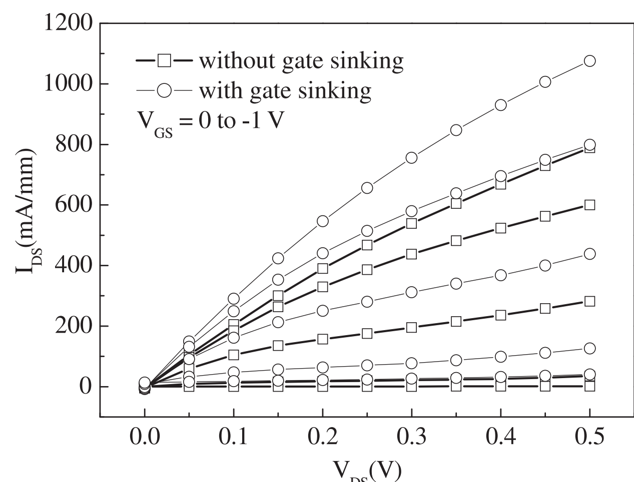

Fig. 2. DC *I–V* characteristics of the devices with and without gate sinking.

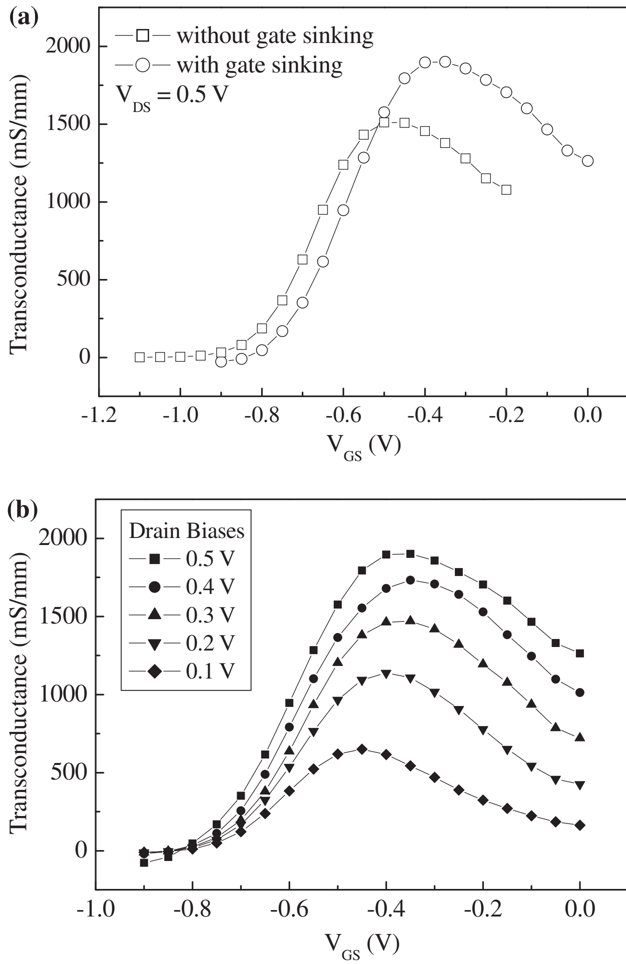

Fig. 3. (a) The transconductance g_m plotted as a function of V_{GS} for devices with and without gate sinking; the peak g_m value increased from 1430 ms/mm for device without gate sinking to 1900 ms/mm for that with gate sinking, both measured at 0.5 V drain bias. (b) g_m plotted as a function of V_{GS} for devices with gate sinking under various drain biases.

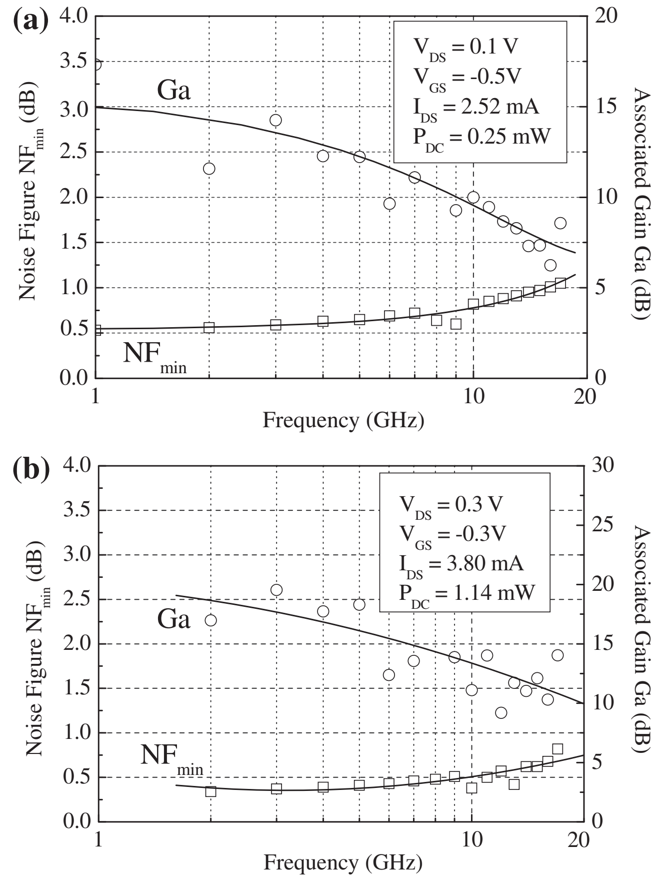

Fig. 4. Measured minimum noise figures ($NF_{\min}$) and the associated gain for (a) V_{DS} = 0.1 V and V_{GS} = −0.5 V; and (b) V_{DS} = 0.3 V and V_{GS} = −0.3 V.

ibration were set at the tips of the probes. The parasitic effect (mainly capacitive) due to the probing pads have been carefully removed from the measured S parameters using the same method as in Ref. [16] and the equivalent circuit model in Ref. [17]. The capacitance at the gate–source end was extracted to be 15.2 fF, whereas that at the gate–drain end was about 10.6 fF. A very high current-gain cutoff frequency f_T of 250 GHz and the maximum oscillation frequency $f_{\max}$ of 214 GHz were obtained for device with sinking as compared with that of f_T = 215 GHz and $f_{\max}$ = 190 GHz for the device without sinking when biased at 0.3 V V_{DS}. Additionally, a reasonable $f_T/f_{\max}$ of 113/110 GHz was achieved at 0.1 V V_{DS} with a corresponding total DC power consumptions of 0.35 mW (8 mW/mm). Such superior performance was mainly due to the reduced gate-to-channel distance by the gate-sinking process. The reduction of gate-to-channel distance tends to suppress the short-channel effect and enhances the overshooting in electron velocity. Furthermore, such reduction also suppresses the formation of surface traps which leads to the reduced parasitic resistance [14,18]. Table 1 summarizes the extracted intrinsic parameters for devices with and without gate sinking at the same drain bias of 0.3 V. The gate biases were set to be −0.4 V (without sinking) and −0.3 V (with sinking), corresponding to the occurrence of peak g_m. The noise performance at different drain biases is shown in Fig. 4a and b with the frequency ranging from 1 to 17 GHz. The measured minimum noise figure ($NF_{\min}$) at 17 GHz was 0.82 and 1.05 dB for V_{DS} = 0.3 and 0.1 V, respectively. The corresponding associated gain (G_a) was measured to be 14 dB for V_{DS} = 0.3 V and 8.6 dB for V_{DS} = 0.1 V, respectively. The optimum source gamma was recorded to be 0.64∠10.4°. Fig. 5 shows the measured minimum noise figure as a function of gate bias at 16 GHz under drain bias of 0.1 V. Clearly a minimum value at V_{GS} = −0.5 V was achieved corresponding to the optimum bias point yielding to peak g_m. To further investigate the effect of gate sinking on the noise performance, semi-empirical equation given by Fukui [19] is adopted which relates the minimum noise figure to the device parameters as;

$$NF_{\min} = 1 + k \cdot (f/f_T) \cdot \sqrt{g_m \cdot (R_g + R_S)} \quad (1)$$

Table 1
Summary of device performance with and without gate sinking Biased at V_{DS} = 0.3 V.

Gate sinking	R_S (Ω mm)	Intrinsic $g_{m,\max}$ (ms/mm)	C_{GS} (fF/mm)	C_{GS} (fF/mm)	f_T (GHz)	$f_{\max}$ (GHz)
Yes	0.102	1752	560	514	250	210
No	0.166	1500	562	560	215	190

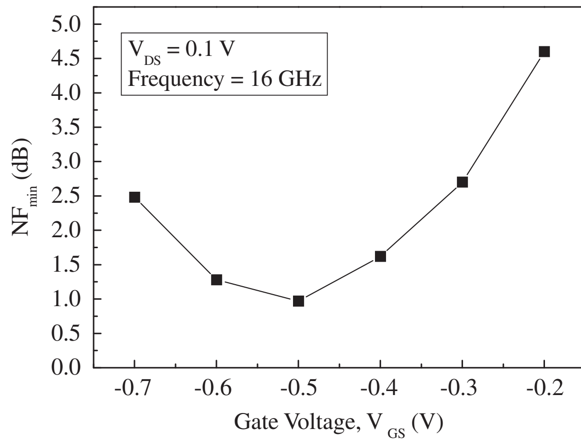

Fig. 5. Measured minimum noise figure at 16 GHz as a function of the gate bias under 0.1 V V_{DS}.

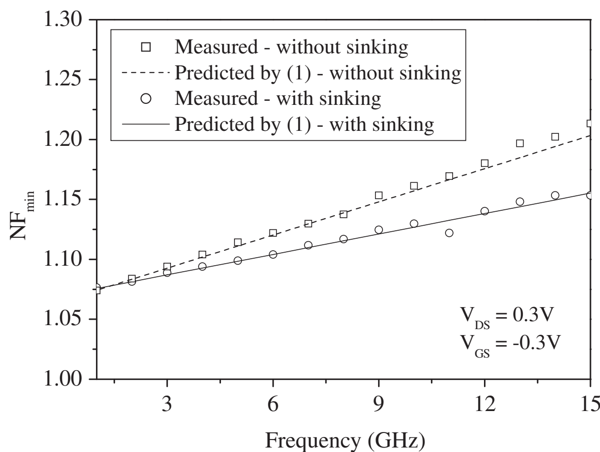

Fig. 6. Measured minimum noise figure as a function of frequency for devices with and without gate sinking at 0.3 V drain bias. Predicted NF_{min} using the extracted intrinsic device parameters listed in Table 1 with (1) for both devices are also included.

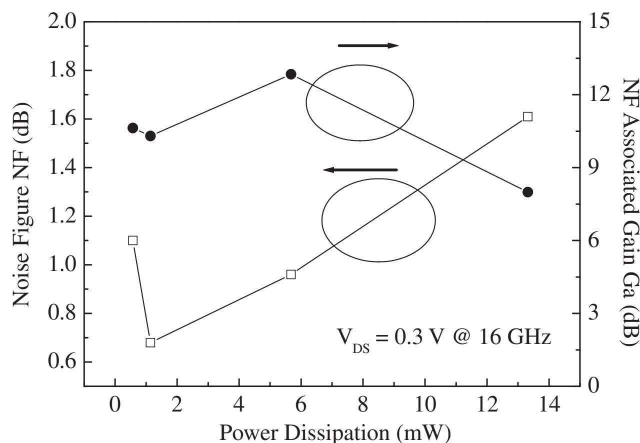

Fig. 7. Measured minimum noise figure and associated gain as functions of the total DC power dissipation for the 2 × 20 μm device with gate sinking at 16 GHz.

where k is a fitting factor representing the quality of channel materials. Fig. 6 shows the measured minimum noise figure as a function of frequency for devices with and without gate sinking at 0.3 V drain bias. Predicted NF_{min} using the extracted intrinsic device parameters listed in Table 1 with (1) for both devices are also included in the same plot. Note that the fitting factor k in (1) for both cases have been set to be the same value as 2.5 which makes great sense since the channel materials for both cases are exactly the same. The improvement in noise figure through gate sinking technology is quite obvious and is even more pronounced at high frequencies. Apparently the improvement in noise figure for devices with gate sinking is mainly attributed to the increase of f_T with contribution from the reduction of the source resistance as well. Fig. 7 shows the measured minimum noise figure and associated gain as functions of the total DC power dissipation for the 2 × 20 μm device with gate sinking at 16 GHz with 0.3 V drain bias. With reasonable gain performance, it is obvious that devices with gate sinking are well suitable for ultra-low power low noise applications at high frequencies.

4. Summary

InAs/$In_{0.7}Ga_{0.3}As$ HEMTs (80 nm) using Pt gate sinking were characterized for ultra-low power low noise applications. Comparisons have been made against the devices without gate sinking. While the epitaxial structure of the device was optimized, the reduction of gate-to-channel distance and R_s was achieved from gate-sinking process. The device exhibited very high drain current density of 1066 mA/mm and maximum g_m of 1900 ms/mm at V_{DS} = 0.5 V. Excellent f_T (f_{max}) up to 113 GHz (110 GHz) at V_{DS} = 0.1 V was achieved. Meanwhile, very low NF_{min} of 1.05 dB and associated gain of 8.6 dB at 17 GHz were achieved at 0.1 V drain bias. Moreover, the devices also exhibited reasonable power and linearity performances characterized at microwave frequencies. These superior performances have made such devices well suitable for future ultra-low power/high-frequency low noise applications.

Acknowledgement

The authors acknowledge the financial support from the National Science Council of the Republic of China (Taiwan) under Grant Nos. NSC-97-2221-E-003-115-070 and NSC-98-2221-E-003-115-069.

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