Capacitor-Less Design of Power-Rail ESD Clamp Circuit With Adjustable Holding Voltage for On-Chip ESD Protection

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***Abstract*—The *RC*-based power-rail ESD clamp circuit with the n-channel metal-oxide-semiconductor (NMOS) transistor drawn in the layout style of big field-effect transistor (BigFET) has been utilized to effectively enhance the ESD robustness of CMOS ICs. In this work, a new ESD-transient detection circuit without using the capacitor has been proposed and verified in a 65 nm 1.2 V CMOS process. The layout area of the new ESD-transient detection circuit can be greatly reduced by more than 54%, as compared to the traditional *RC*-based ESD-transient detection circuit realized with capacitor. From the experimental results, the new proposed ESD-transient detection circuit with adjustable holding voltage can achieve long enough turn-on duration under the ESD stress condition, as well as better immunity against mistrigger and transient-induced latch-on event under the fast power-on and transient noise conditions.**

***Index Terms*—Big field-effect transistor (BigFET), electrostatic discharge (ESD), holding voltage, power-rail ESD clamp circuit.**

I. Introduction

With the continuously scaled-down CMOS technology, electrostatic discharge (ESD) protection has become the major concern of reliability for integrated circuits (ICs) in nanoscale CMOS technology. The nanoscale device with thinner gate oxide and shallower diffusion junction depth seriously degraded the ESD robustness of ICs and raised the difficulty of ESD protection design for ICs implemented in nanoscale CMOS technology [1], [2]. In order to sustain the required ESD robustness, such as 2 kV in human-body-model (HBM) [3] and 200 V in machine-model (MM) [4], the power-rail ESD clamp circuit is an important element to achieve whole-chip ESD protection for ICs [5], [6]. The power-rail ESD clamp circuit is vital for ESD protection under V_{DD}-to-V_{SS} (or V_{SS}-to-V_{DD}) ESD stress, as well as different ESD stress conditions from the input/output to V_{DD}/V_{SS}, including positive-to-V_{SS} (PS) mode, negative-to-V_{SS} (NS) mode, positive-to-V_{DD} (PD) mode, and negative-to-V_{DD} (ND) mode, which are illustrated in Fig. 1(a) and (b). Therefore, the power-rail ESD clamp circuit can provide efficient protection to the internal circuits of IC products.

In advanced nanoscale CMOS technology, the ESD clamp device drawn in the layout style of big field-effect transistor (BigFET) had demonstrated excellent ESD protection performance [7]–[12]. In these power-rail ESD clamp circuits, the ESD clamp devices can discharge a large ESD current by the inversion channel layer without snapback operation of the parasitic BJT [13]–[16]. The typical power-rail ESD clamp circuit, which was shown in Fig. 2 with *RC*-based ESD-transient detection circuit and a controlling circuit, commands the ESD clamp device to turn on under ESD stress conditions and to turn off under normal circuit operation conditions. Practically, there are two different circuit skills, the *RC*-delay technique [7]–[10] and the capacitance-coupling design [11], [12], to realize the ESD-transient detection circuit in the power-rail ESD clamp circuit. The turn-on duration of the ESD clamp nMOS transistor is mainly controlled by the *RC*-time constant of the *RC*-based ESD-transient detection circuit [7]–[10]. Consequently, the *RC*-time constant would be designed large enough about several hundreds nanosecond to keep the ESD clamp nMOS transistor at "ON" state under the ESD stress condition. However, the extended *RC*-time constant of the ESD-transient detection circuit suffers not only the larger layout area from the resistance and capacitance but also the mistriggering of the ESD clamp nMOS transistor under fast-power-on application [8].

In previous studies [7], [8], [11], [12], they demonstrated the power-rail ESD clamp circuits with feedback circuit methods to extend the turn-on duration by using a small *RC*-time constant. However, the feedback circuit designs would suffer the latch-on issue under the fast power-on or the electrical fast transient (EFT) conditions [17]. Moreover, some circuit designs, such as on-time control circuits [7] and multi-*RC*-triggered circuits [9], had also been used to extend the turn-on duration without the latch-on issue. However, those previous circuits are more complicated with large silicon layout area including the requested resistances and capacitances in the ESD-transient detection circuits.

In this work, a new capacitor-less ESD-transient detection circuit, which is combined with the parasitic capacitance of the ESD clamp nMOS transistor drawn in BigFET layout style, has been proposed and verified in 65 nm 1.2 V CMOS technology.

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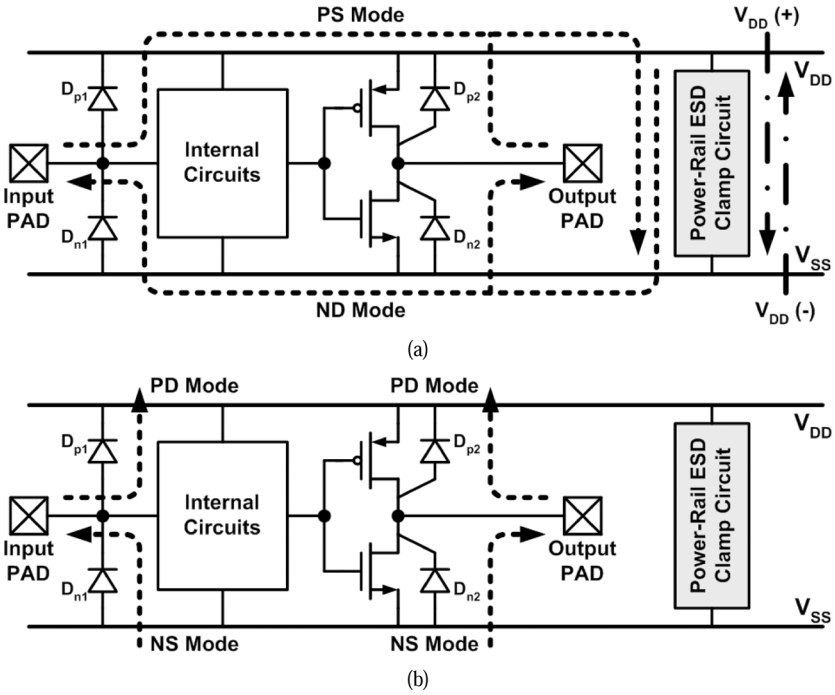


Fig. 1. Typical on-chip ESD protection design with active power-rail ESD clamp circuit under (a) PS mode/ND mode, and (b) PD mode/NS mode, ESD stress conditions.

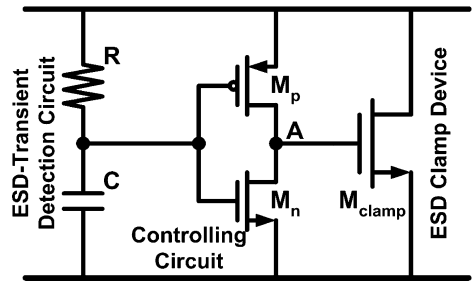


Fig. 2. Typical implementation of the *RC*-based power-rail ESD clamp circuit with ESD-transient detection circuit, controlling circuit, and ESD clamp device.

This new design adopts the feedback circuit in cascode structure to achieve desired function for controlling the ESD clamp nMOS transistor. According to the experimental measured results, the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit has revealed a much better performance than that in the traditional *RC*-based power-rail ESD clamp circuit.

II. Capacitor-Less Power-Rail ESD Clamp Circuit

A. New Proposed ESD-Transient Detection Circuit

The capacitor-less ESD-transient detection circuits with different number of diodes in series are illustrated in Fig. 3. The proposed power-rail ESD clamp circuit in Fig. 3(a) consists of the ESD-transient detection circuit with feedback technique, which are realized by two transistors ($M_{\rm n}$ and $M_{\rm p}$) and two resistances ($R_{\rm n}$ and $R_{\rm p}$), and the ESD clamp nMOS transistor ($M_{\rm clamp}$) drawn in BigFET layout style. These two resistances are realized by N-well resistance with shallow trench isolation (STI). In Fig. 3(a), the gate terminal of ESD clamp nMOS transistor is linked to the output of the ESD-transient detection circuit. The circuit is connected in a cascode structure ($R_{\rm n}$ with $M_{\rm n}$, and $M_{\rm p}$ with $R_{\rm p}$) to construct the ESD-transient detection circuit with positive-feedback mechanism, which can command the ESD clamp nMOS transistor at "ON" or "OFF" state.

To overcome the transient-induced latch-on issue, the ESD-transient detection circuit is added with one or two diodes in series to adjust its holding voltage, as shown in Fig. 3(b) and (c), respectively. The anode of the diode is connected to the gate terminal of $M_{\rm p}$ transistor, and its cathode is connected to the drain terminal of $M_{\rm n}$ transistor. With such a modification, the holding voltage of the power-rail ESD clamp circuit can be adjusted by the number of added diodes.

Verified in the testchip, the ESD clamp nMOS transistor is drawn in BigFET layout style without silicide blocking in a 65 nm 1.2 V CMOS process. Compared with the power-rail ESD clamp circuit with the traditional *RC*-based ESD-transient detection circuit, the layout area of the new proposed ESD-transient detection circuit is much smaller, as illustrated in Fig. 4(a) to (d). The dimension of $M_{\rm clamp}$ in all circuits verified in the silicon testchip is kept the same of 2000 μm/0.1 μm. According to the layout area of the new proposed power-rail ESD clamp circuits, the cell height of the whole power-rail ESD clamp circuit is reduced by 30%, and the layout area of the ESD-transient detection circuit is reduced by 54.5%.

B. Operation Principles

The most important feature of the new proposed power-rail ESD clamp circuit is no need of additional capacitor. Because the ESD clamp nMOS transistor is drawn in BigFET layout style without silicide blocking, a large gate-to-drain, gate-to-source,

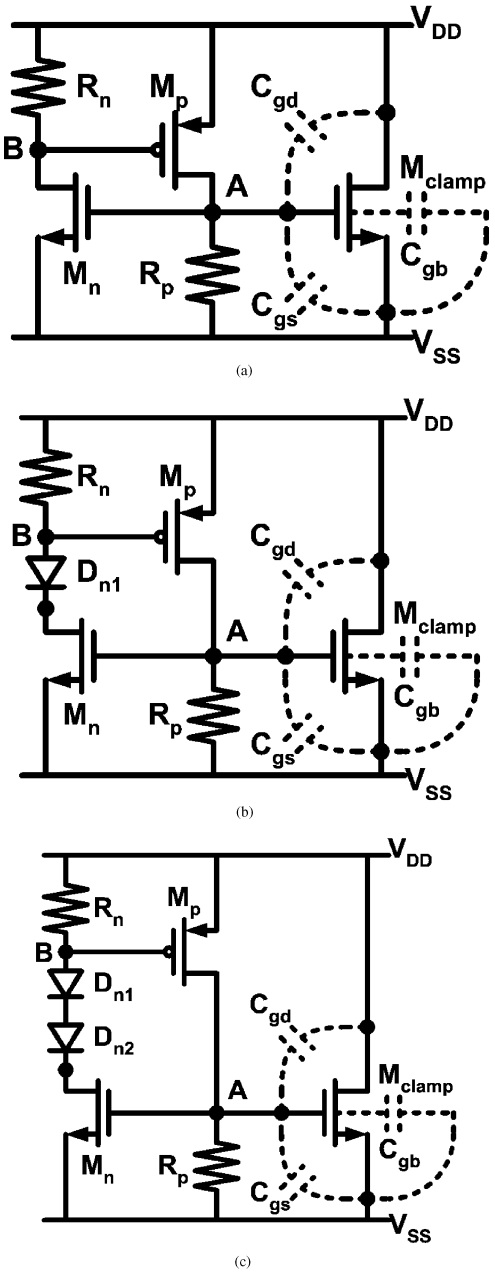


Fig. 3. Power-rail ESD clamp circuits with the new proposed ESD-transient detection circuit. There are (a) zero diode, (b) one diode, and (c) two diodes used in the ESD-transient detection circuit, respectively.

and gate-to-body parasitic capacitances ($\mathrm{C_{gd}}$, $\mathrm{C_{gs}}$, and $\mathrm{C_{gb}}$) essentially exist in the ESD clamp nMOS transistor. Sufficiently utilizing these parasitic capacitances with the resistance (R_{p}) to realize capacitance-coupling mechanism, no additional capacitor is needed in this design. In Fig. 3(a), during the positive V_{DD}-to-V_{SS} ESD stress condition, the voltage of node A will be simultaneously elevated toward a positive voltage through the coupling effect from the parasitic capacitances of the ESD clamp nMOS transistor. The elevated voltage of node A can not hold for a long time because the resistance (R_{p}) connected to V_{SS} would pull down the voltage of node A. Therefore, the nMOS transistor (M_{n}) is designed to immediately start the ESD-transient detection circuit with positive feedback mechanism when the voltage of node A is elevated. The turned-on nMOS transistor (M_{n}) makes the voltage of node B low enough to turn on the pMOS transistor (M_{p}) due to the voltage drop on the resistor (R_{n}). Therefore, the feedback loop of the ESD-transient detection circuit is started entirely, and the voltage of node A is continuously elevated to the voltage level at V_{DD} line by the turned-on pMOS transistor (M_{p}) during the ESD stress transition. Finally, the ESD clamp nMOS transistor is turned on to discharge ESD current. A 3 V voltage pulse with a rise time of 5 ns was applied to the V_{DD} node while the V_{SS} node was grounded to simulate the fast-rising edge of the HBM ESD event, as illustrated in Fig. 5. The simulation results clearly demonstrate that the voltage at node A can be elevated to the voltage level at V_{DD}. However, the voltage at node A in the *RC*-based power-rail ESD clamp circuit is elevated to the voltage level higher than the threshold voltage of ∼0.58 V for only the first period of ∼300 ns. The design parameters, including the device sizes of each transistor and resistor, are listed in Table I. On the other hand, the parasitic drain-substrate diode in the ESD clamp nMOS transistor can provide a low impedance path under the negative V_{DD}-to-V_{SS} ESD stress.

With the proposed power-rail ESD clamp circuit in Fig. 3, the gain (G) of the coupling effect composed of $\mathrm{C_{gd}}$, $\mathrm{C_{gs}}$, $\mathrm{C_{gb}}$, and R_{p} can be expressed as

$$G = \frac{V_A}{V_{\mathrm{DD}}} = \left| \frac{\left(\frac{1}{R_{\mathrm{p}}} + j\omega(C_{\mathrm{gs}} + C_{\mathrm{gb}})\right)^{-1}}{\frac{1}{j\omega C_{\mathrm{gd}}} + \left(\frac{1}{R_{\mathrm{p}}} + j\omega(C_{\mathrm{gs}} + C_{\mathrm{gb}})\right)^{-1}} \right|. \quad (1)$$

According to the design parameters of the proposed power-rail ESD clamp circuit, the gain with $\mathrm{C_{gd}} \fallingdotseq \mathrm{C_{gs}} = 0.43$ pF, $\mathrm{C_{gb}} = 0.39$ pF, $R_{\mathrm{p}} = 20$ kΩ, and signal frequency of 50 MHz derived from 5 ns fast-rising edge of the voltage pulse, would be 0.34. Therefore, the voltage of node A is determined by the gain of the coupling structure. As shown in Fig. 6, the coupling voltage at node A is exactly equal to 0.34 $\mathrm{V_{DD}}$ before the ESD-transient detection circuit is turned on. When the subthreshold current of the M_{n} can produce enough voltage drop on R_{n} to further turn on the M_{p}, the voltage at node A would be elevated quickly to the voltage level at V_{DD}. In Fig. 6, it can be observed that the voltage of node A is elevated to 0.41 V and then raised quickly because the ESD-transient detection circuit is turned on. Consequently, the ESD clamp nMOS transistor is turned on by the ESD-transient detection circuit with positive feedback mechanism. The gain expression in (1) of the coupling structure has been successfully verified by the simulation.

According to (1), the most critical device is the R_{p} to quickly drive the M_{n} into subthreshold region during the pulse rising period. Therefore, the R_{p} is chosen to be 20 kΩ to make the gain of the coupling structure and the layout area of R_{p} optimal. The resistance R_{n} of 40 kΩ is determined to produce enough voltage drop on R_{n} to further turn on the M_{p} as long as there is subthreshold current of a few tens micro-ampere flowing through the R_{n}. Consequently, the ESD-transient detection circuit with positive feedback mechanism can be successfully initiated.

According to the design window of the ESD protection circuit for avoiding the latch-on issue, the holding voltage (V_{h}) of the ESD protection circuit is an important index to exceed the

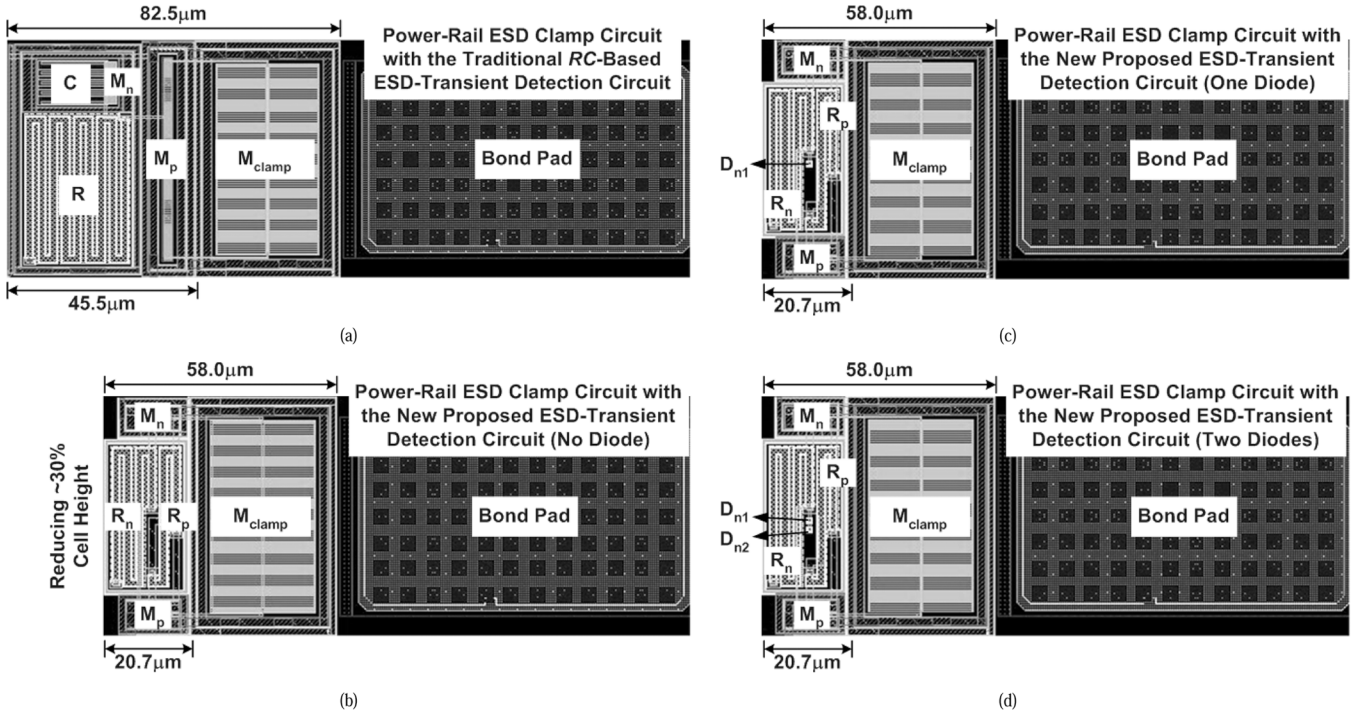


Fig. 4. Comparison on the layout areas among the four power-rail ESD clamp circuits. The $M_{\rm clamp}$ is drawn in a BigFET layout style with the same $\rm W/L = 2000\ \mu m/0.1\ \mu m$, which is triggered by (a) the traditional *RC*-based ESD-transient detection circuit, (b) the proposed ESD-transient detection circuit with no diode, (c) the proposed ESD-transient detection circuit with one diode, and (d) the proposed ESD-transient detection circuit with two diodes.

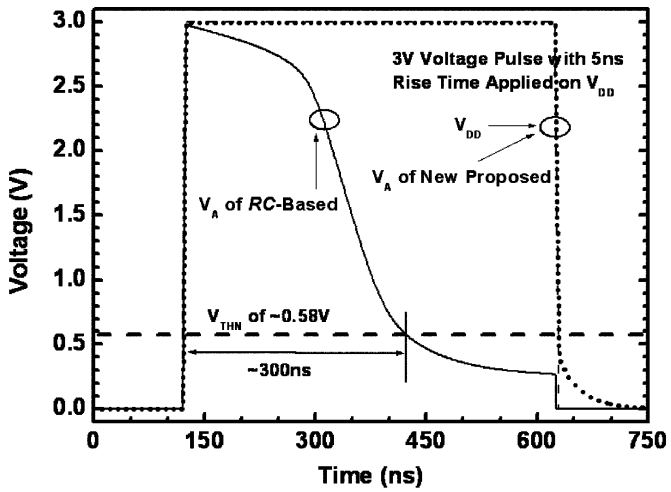


Fig. 5. ESD-like simulation results of the voltage at the gate terminal of the ESD clamp nMOS transistor controlled by the *RC*-based and the new proposed ESD-transient detection circuit.

normal circuit operation voltage $V_{\rm DD}$. The holding voltage of the proposed power-rail ESD clamp circuit can be indicated as

$$V_h = V_{\rm ds(M_n)} + nV_{\rm ON(Diode)} + V_{\rm gs(M_p)} = V_{\rm ds(M_n)}\big|_{I_{\rm ds}=V_{\rm THP}/R_{\rm n}} + nV_{\rm ON(Diode)} + V_{\rm THP} \quad (2)$$

where n and $V_{\rm ON}$ are the number and the turn-on voltage of the diode, respectively. For the pMOS threshold voltage of 0.58 V and $R_{\rm n}$ resistance of 40 kΩ, the $\rm I_{ds}$ current flowing through the $M_{\rm n}$ transistor is only about 14.5 μA. Based on the device parameters and simulation results, the $V_{\rm ds}$ of $M_{\rm n}$ transistor is only a few milli-volt and the $V_{\rm ON}$ of diode is about 0.67 V. Therefore, the $V_{\rm h}$ in the expression (2) can be re-expressed as below due to minor $V_{\rm ds}$ compared to $V_{\rm ON}$ and $V_{\rm THP}$.

$$V_h \approx nV_{\rm ON(Diode)} + V_{\rm THP} \quad (3)$$

For the new proposed power-rail ESD clamp circuit in Fig. 3(a), the $V_{\rm h}$ would be only 0.58 V due to zero diode in the ESD-transient detection circuit. It would be a high risk to apply the structure in Fig. 3(a) to the circuit with 1.2 V operation voltage. However, the $V_{\rm h}$ can be theoretically adjusted to 1.25 V and 1.92 V for the new proposed structures in Fig. 3(b) and (c), respectively. By adding the diodes in the ESD-transient detection circuit, the new proposed power-rail ESD clamp circuit with adjustable holding voltage can be safely applied to protect any internal circuits from the transient-induced latch-on event.

Under the normal $V_{\rm DD}$ power-on condition, the gain of the coupling structure is 1.35×10^{-5} for a 1.2 V power-on voltage pulse with a rise time of 1 ms. Such a slow-rising power-on voltage will not induce a high enough coupling voltage at node A to initiate the ESD-transient detection circuit. When the power-on voltage pulse has a rise time of 100 ns, the gain of the coupling structure is only 0.13, which is also too small to initiate the ESD-transient detection circuit. Even though the power-rail ESD clamp circuit encounters a fast-rising power-on voltage with the order of nanoseconds, the voltage level of node A and node B can be kept at ground and $V_{\rm DD}$, respectively, due to the design with adjustable holding voltage. Therefore, the new proposed power-rail ESD clamp circuit can have excellent immunity against mistrigger under the fast power-on conditions.

TABLE I
DESIGN PARAMETERS OF THE POWER-RAIL ESD CLAMP CIRCUITS

Design Parameters	*RC*-Based ESD Clamp Circuit	New Proposed ESD Clamp Circuit
Capacitor	64 μm / 2 μm (W/L)	none
Resistor (Ω)	R = 113k	R_n = 40k ; R_p = 20k
PMOS Transistor (M_p)	184 μm / 60 nm	24 μm / 60 nm
NMOS Transistor (M_n)	36 μm / 60 nm	12 μm / 60 nm
ESD Clamp NMOS Transistor (M_{clamp})	2000 μm / 100 nm	2000 μm / 100 nm
Diode (D_n)	none	0.057 μm^2

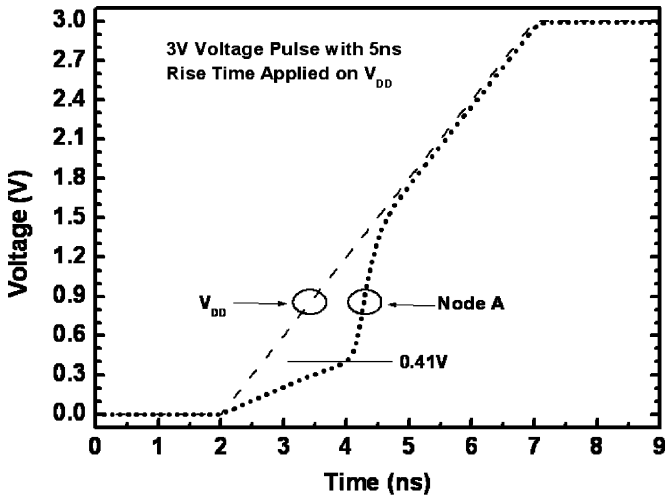


Fig. 6. The simulation results of the voltage transient on $V_{\rm DD}$ and node A for new proposed power-rail ESD clamp circuit. The 3 V ESD-like voltage pulse with 5 ns rise time is applied on $V_{\rm DD}$.

III. EXPERIMENTAL RESULTS

The testchips of power-rail ESD clamp circuits with the traditional *RC*-based and the new proposed ESD-transient detection circuits have been fabricated in a 65 nm 1.2 V CMOS process, as shown in Fig. 7(a) and (b). These circuits are prepared for DC *I–V* measurement, transmission line pulsing (TLP) measurement, turn-on verification measurement, and transient-induced latch-up (TLU) measurement.

A. DC I–V Measurement

The DC *I–V* characteristics of the power-rail ESD clamp circuits are measured by HP4155 from 0 V to 1.2 V with the voltage step of 10 mV. The leakage currents of the power-rail ESD clamp circuits at 1.2 V normal $V_{\rm DD}$ operation voltage can be observed clearly in Fig. 8. The leakage current of the *RC*-based power-rail ESD clamp circuit is 86.9 nA. However, the new proposed power-rail ESD clamp circuits have the leakage currents of the range from 50.2 nA to 55.3 nA, and the leakage current of the ESD clamp nMOS transistor ($M_{\rm clamp}$) is about 49.2 nA. This implies that the leakage currents of the *RC*-based and the new proposed ESD-transient detection circuits are 37.7 nA and 6.1 nA, respectively. The leakage current of the new proposed ESD-transient detection circuit is extremely reduced by 83.8% because the device sizes of $M_{\rm n}$ and $M_{\rm p}$ transistors are greatly shrunk. Therefore, the new proposed power-rail ESD clamp circuit with lower leakage current is more adequate for the portable product applications, which strongly demand the low standby current.

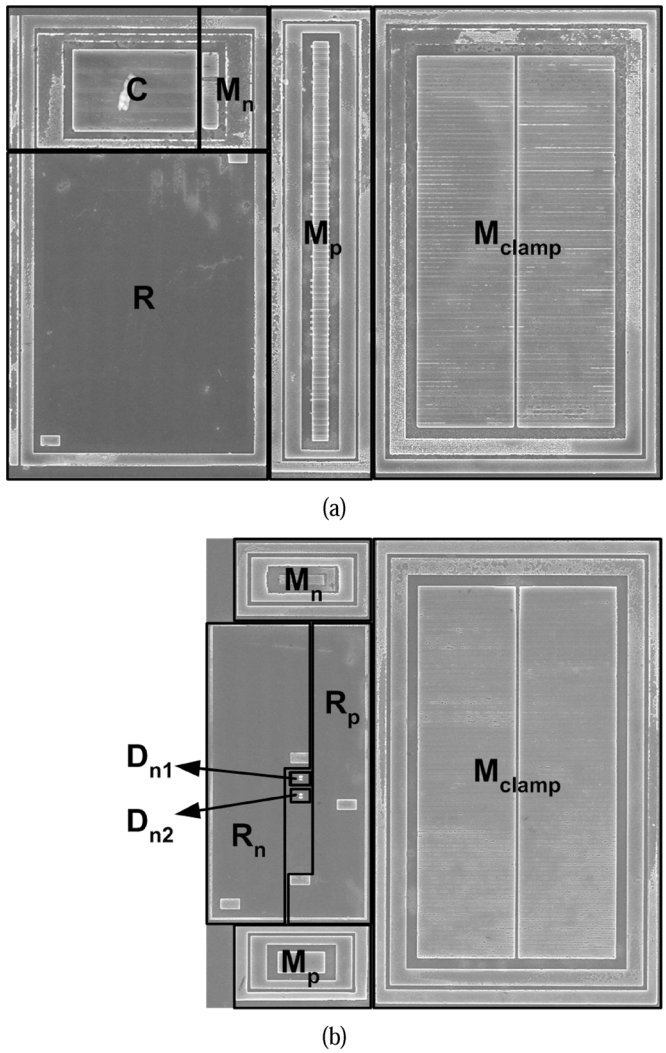


Fig. 7. Chip microphotographs of the fabricated power-rail ESD clamp circuit, realized with (a) the traditional *RC*-based ESD-transient detection circuit and (b) the proposed ESD-transient detection circuit with two diodes.

B. Transmission Line Pulsing (TLP) Measurement and ESD Robustness

In order to investigate the circuit behavior during high ESD current stress, transmission line pulsing (TLP) generator with a pulse width of 100 ns and a rise time of ∼2 ns is used to measure the *RC*-based and the new proposed power-rail ESD clamp circuits [18]. The measured results, as illustrated in Fig. 9(a), demonstrate that there are no obvious differences among the curves at the voltage level higher than 4 V because the ESD clamp nMOS transistors in all power-rail ESD clamp circuits are drawn with the same device dimension and layout style. The

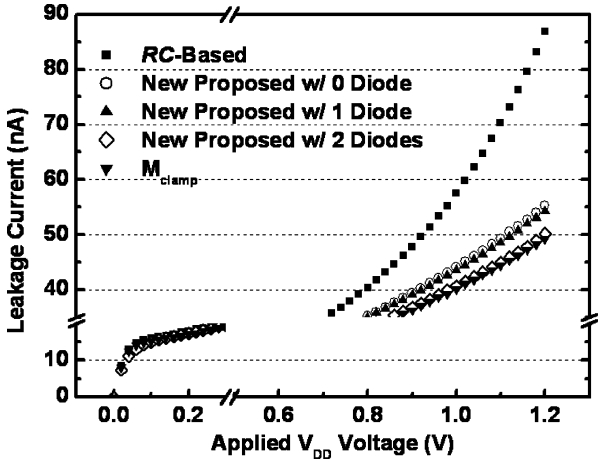


Fig. 8. The measured DC *I–V* curves of the *RC*-based power-rail ESD clamp circuit, the new proposed power-rail ESD clamp circuits, and the single ESD clamp nMOS transistor ($M_{\rm clamp}$).

second breakdown currents ($\rm It_2$) of these four power-rail ESD clamp circuits are all around 5.44 A.

The holding voltages ($V_{\rm h}$) of the new proposed ESD-transient detection circuits with zero, one, and two diodes are 0.51 V, 1.22 V, and 1.95 V, respectively, in Fig. 9(b). These measured $V_{\rm h}$ are very close to the theoretical $V_{\rm h}$ of 0.58 V, 1.25 V, and 1.92 V calculated in Section II-B. The adjustable holding voltage by modifying the number of diodes in the ESD-transient detection circuit has been successfully verified by the TLP *I–V* measurement.

Table II shows the HBM [3] and MM [4] ESD robustness of these four power-rail ESD clamp circuits. The HBM and MM ESD robustness of all power-rail ESD clamp circuits are over 8 kV and 450 V, respectively. It is obvious that the characteristics ($\rm It_2$, HBM, and MM ESD levels) of all power-rail ESD clamp circuits are the same due to the same device dimension and layout style of the ESD clamp nMOS transistors.

C. Turn-On Verification

In order to observe the turn-on efficiency of the power-rail ESD clamp circuits, a 3 V ESD-transient-like voltage pulse with 5 ns rise time is applied to the $V_{\rm DD}$ power line with the grounded $V_{\rm SS}$. The voltage pulse with a rise time of 5 ns is utilized to simulate the fast-rising edge of the HBM ESD event [3]. The ESD-transient-like voltage pulse will be coupled to the gate terminal of the $M_{\rm n}$ transistor in the proposed ESD-transient detection circuit, and then the proposed ESD-transient detection circuit with positive feedback mechanism will be started up. Consequently, the $M_{\rm clamp}$ transistor is triggered on. The turn-on verifications of the voltage waveform on $V_{\rm DD}$ power line under ESD-like stress condition are shown in Fig. 10(a).

In Fig. 10(a), the voltage waveform of the *RC*-based design rises as the time is increased. On the contrary, the voltage waveforms of the new proposed designs can be clamped to a specific voltage level during the whole pulse width due to the positive feedback mechanism of the ESD-transient detection circuit. Therefore, the new proposed ESD-transient detection circuit can efficiently extend the turn-on duration of the ESD clamp nMOS transistor under ESD stress conditions.

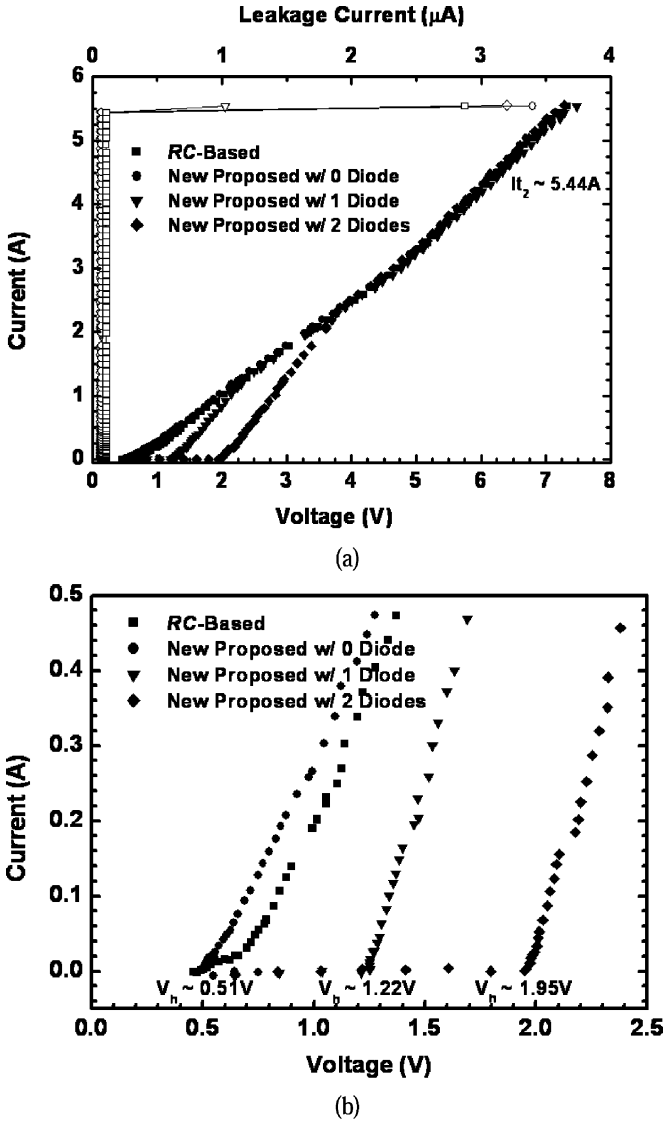


Fig. 9. TLP measured *I–V* curves of (a) the power-rail ESD clamp circuits with the *RC*-based, the new proposed ESD-transient detection circuit, and (b) the zoom-in illustration for the holding voltages ($V_{\rm h}$).

For power-on condition, the voltage usually has a rise time in the order of milliseconds. According to this feature, the coupling voltage at node A is not enough to start up the ESD-transient detection circuit, and the ESD clamp nMOS transistor will be kept at "OFF" state. However, some previous studies [7]–[10], [17] have demonstrated that the power-rail ESD clamp circuits with *RC*-based ESD-transient detection circuits and feedback mechanism were easily mistriggered into the latch-on state under the fast power-on condition. The new proposed power-rail ESD clamp circuits have been applied with 1.2 V voltage pulse with 25 ns rise time to investigate their immunity against mistrigger, as shown in Fig. 10(b). The voltage waveforms of the new proposed power-rail ESD clamp circuits are not degraded under the fast power-on condition. Even though the rise time of fast power-on voltage is shorter than 25 ns, the new proposed power-rail ESD clamp circuits with adjustable holding voltage can still perform high immunity against mistrigger. On the contrary, the *RC*-based power-rail ESD clamp circuit dramatically suffered

TABLE II
MEASURED RESULTS OF SECOND BREAKDOWN CURRENT AND ESD LEVELS OF FOUR POWER-RAIL ESD CLAMP CIRCUITS

Power-Rail ESD Clamp Circuits	It_2 (A)	HBM Level (kV)	MM Level (V)
Traditional *RC*-Based	5.44	> 8	450
New Proposed with 0 Diode	5.44	> 8	450
New Proposed with 1 Diode	5.44	> 8	450
New Proposed with 2 Diodes	5.44	> 8	450

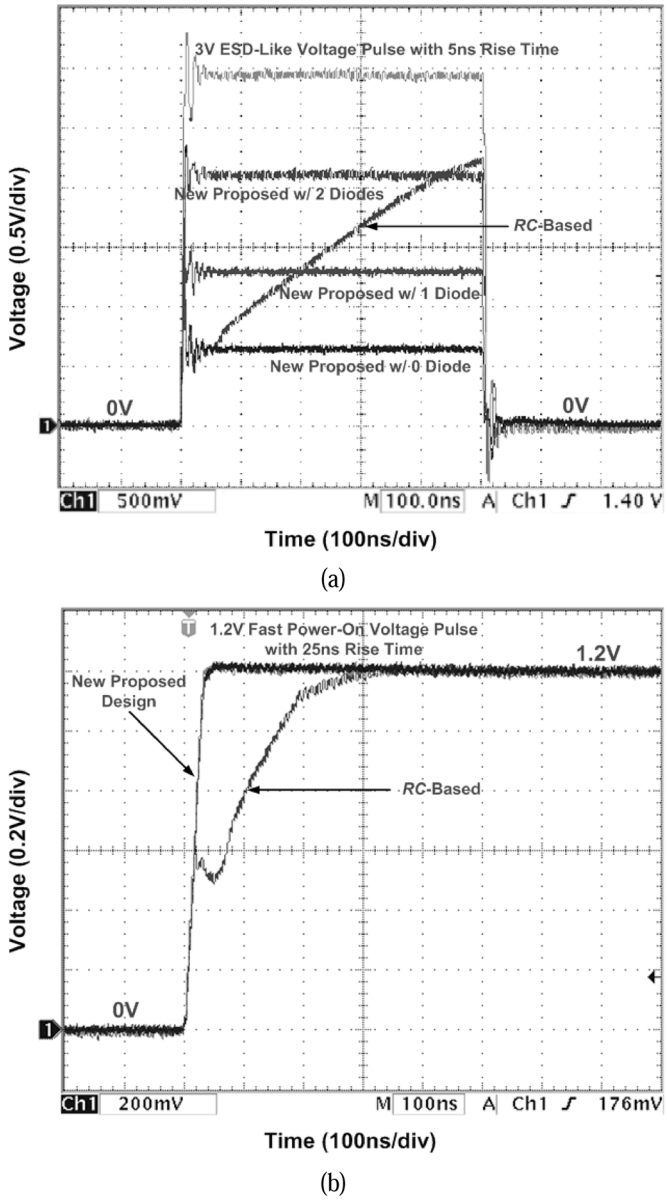


Fig. 10. The voltage waveforms under (a) ESD-transient-like condition with 3 V voltage pulse and 5 ns rise time, (b) fast-power-on condition with 1.2 V voltage pulse and 25 ns rise time.

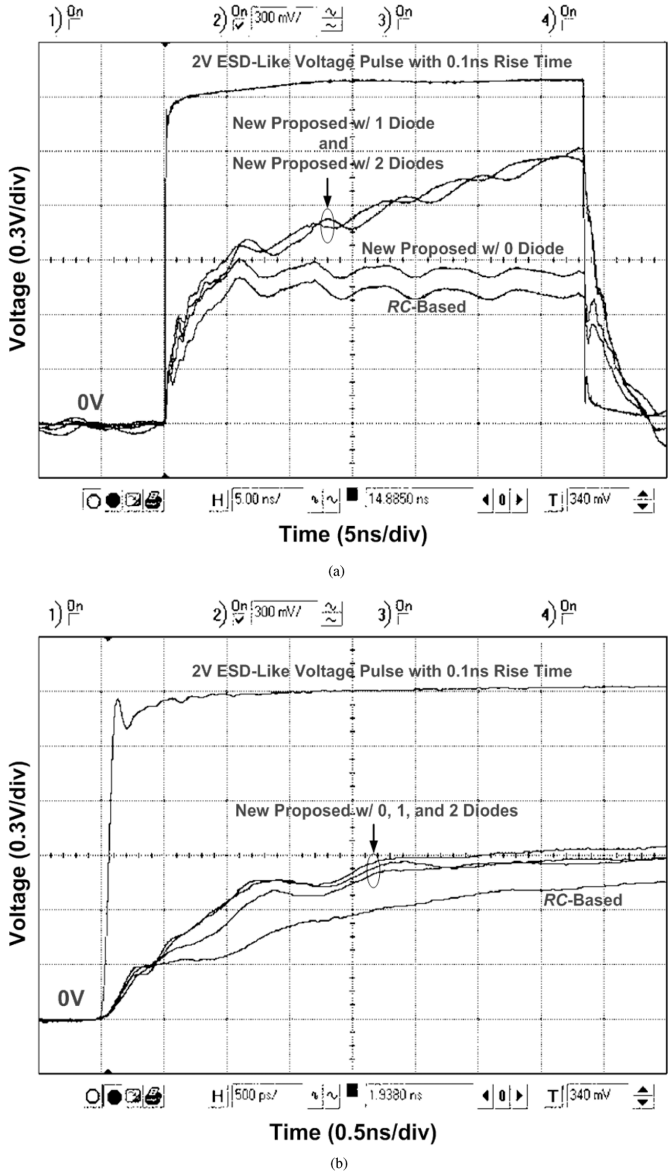
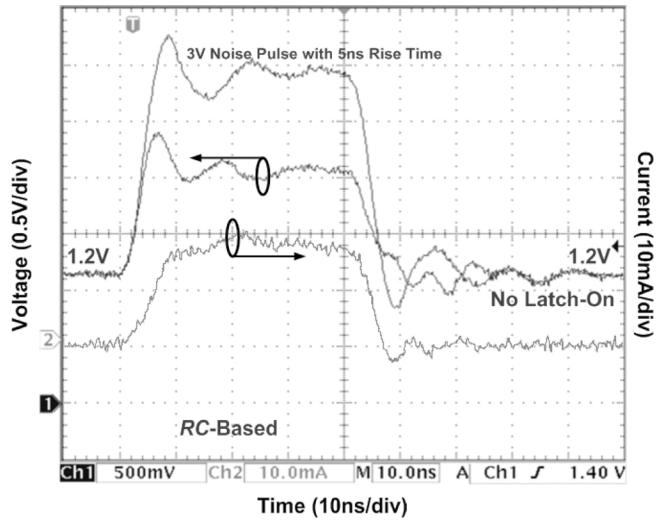


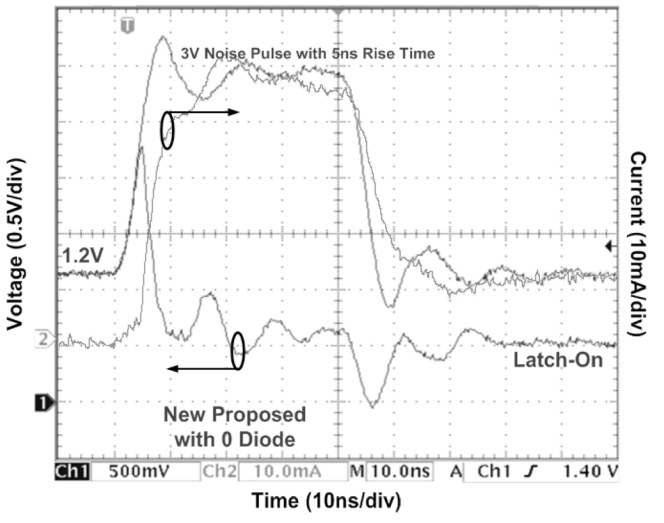
Fig. 11. (a) The measured voltage waveforms of all power-rail ESD clamp circuits under ESD-transient-like condition with 2 V voltage pulse and 0.1 ns rise time, and (b) the zoomed-in illustration on the short rising period for observing the trigger speed.

the mistrigger under the fast power-on condition, and it spends about 300 ns to return back the normal operation voltage level.

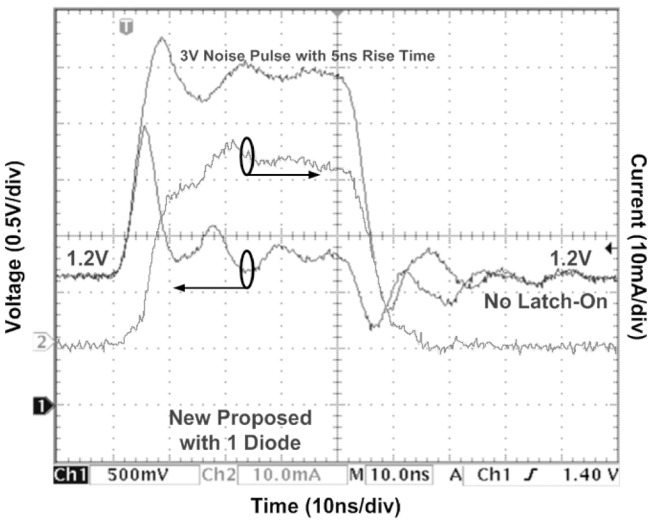
In order to further verify the trigger speed of the proposed capacitor-less power-rail ESD clamp circuit for charged-device-model (CDM) ESD protection, a pulse generator (Agilent 81134A) and a high sampling-rate oscilloscope (Agilent DSO81304A) are used to verify the trigger speed of the new proposed power-rail ESD clamp circuits and the traditional *RC*-based power-rail ESD clamp circuit. The experimentally measured results are shown in Fig. 11(a) and (b). A 2 V ESD-like transient voltage pulse with a rise time of 0.1 ns is directly applied to the V_{DD} of each power-rail ESD clamp circuit with its V_{SS} grounded. As shown in Fig. 11(a), the proposed power-rail ESD clamp circuits can be triggered on immediately, as fast as that of the traditional *RC*-based power-rail ESD clamp circuit. The zoomed-in transient voltage



(a)



(b)



(c)

Fig. 12. The measured voltage and current waveforms of power-rail ESD clamp circuit, realized with (a) the traditional *RC*-based ESD-transient detection circuit, (b) the proposed ESD-transient detection circuit with no diode, and (c) the proposed ESD-transient detection circuit with one diode, under transient noise condition.

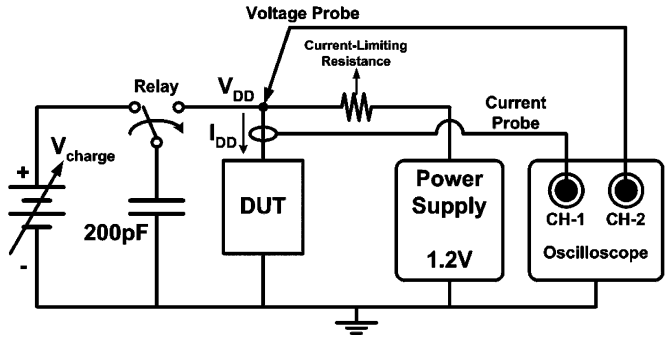


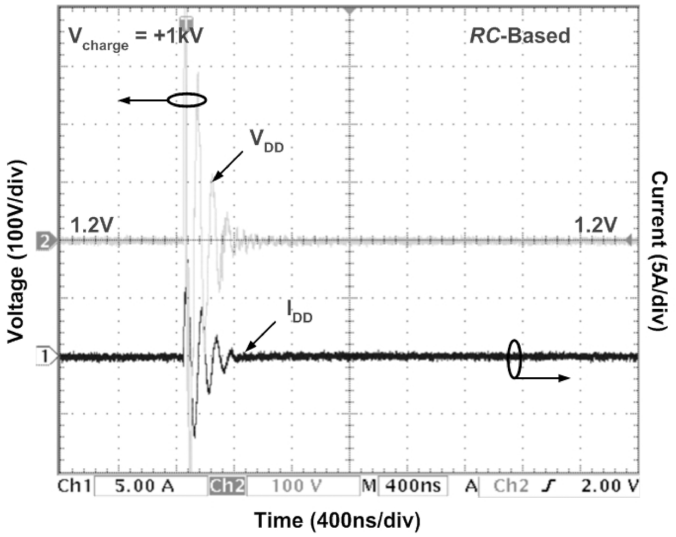
Fig. 13. The setup for transient-induced latch-up (TLU) measurement [19], [20].

waveforms on the short rising period are shown in Fig. 11(b) to clearly observe the trigger speed among the fabricated power-rail ESD clamp circuits. As comparing to the originally applied 2 V voltage pulse, the degraded voltage waveforms in Fig. 11 are due to the turn-on operation of the power-rail ESD clamp circuits. With such experimental verification, the trigger speed of the proposed capacitor-less power-rail ESD clamp circuit can be still fast enough to provide ESD protection against the CDM ESD events.

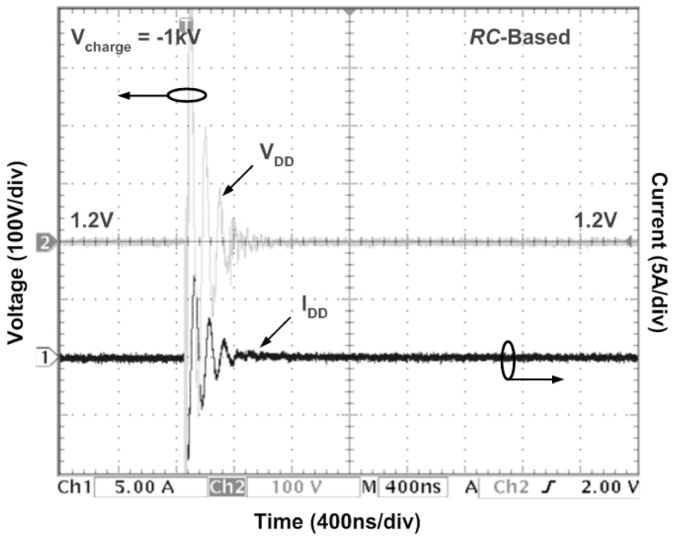
In addition, the turn-on verification with the power line noise at normal operation is another useful justification for the latch-on concerns. The transient noise with 3 V voltage level and a rise time of 5 ns is purposely added to $V_{\rm DD}$ power line with 1.2 V operation voltage. As shown in Figs. 12(a)–(c), the new proposed ESD-transient detection circuit with zero diode is the only circuit to suffer the latch-on issue because its holding voltage is much lower than the 1.2 V operation voltage. However, the holding voltage of the new proposed ESD-transient detection circuit can be adjusted by adding the diodes. Therefore, the ESD-transient detection circuits with positive feedback mechanism and the adjustable holding voltage can be free to latch-on issue. Since the feedback mechanism is not used in the *RC*-based power-rail ESD clamp circuit, the latch-on event is not occurred.

D. Transient-Induced Latch-Up (TLU) Measurement

The transient-induced latch-up (TLU) measurement has been used to investigate the susceptibility of device under test (DUT) to the noise transient or glitch on the power lines under normal circuit operation condition. The TLU measurement setup with bipolar trigger waveform can accurately simulate the practical system-level ESD event [19]. The setup for TLU measurement is shown in Fig. 13 [19], [20]. The charging voltage ($V_{\rm charge}$) has positive ($V_{\rm charge} > 0$) and negative ($V_{\rm charge} < 0$) polarities. The positive (negative) $V_{\rm charge}$ can generate the positive-going (negative-going) bipolar trigger noise into the power pins of the DUT. A 200 pF capacitor is employed as the charging capacitor. The supply voltage of 1.2 V is used as $V_{\rm DD}$ and the noise trigger source is directly connected to DUT through the relay in the measurement setup. The current-limiting resistance of 4.7 Ω is used to avoid electrical overstress (EOS) damage in the DUT under a high-current latch-on state. The voltage and current waveforms of the DUT at $V_{\rm DD}$ node after TLU measurement are monitored by the oscilloscope.

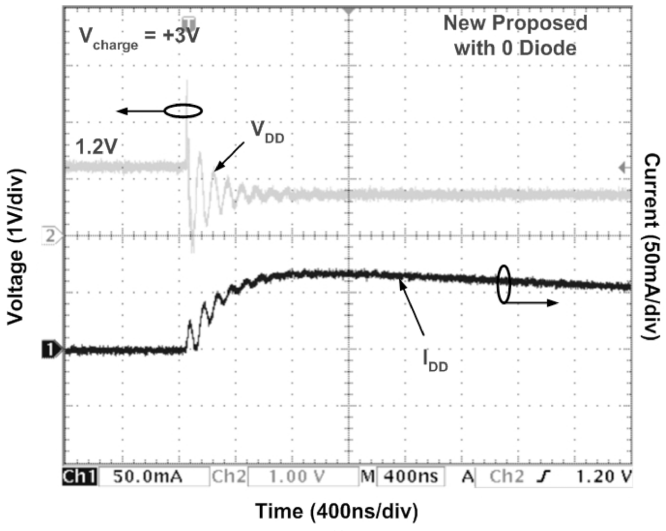


(a)

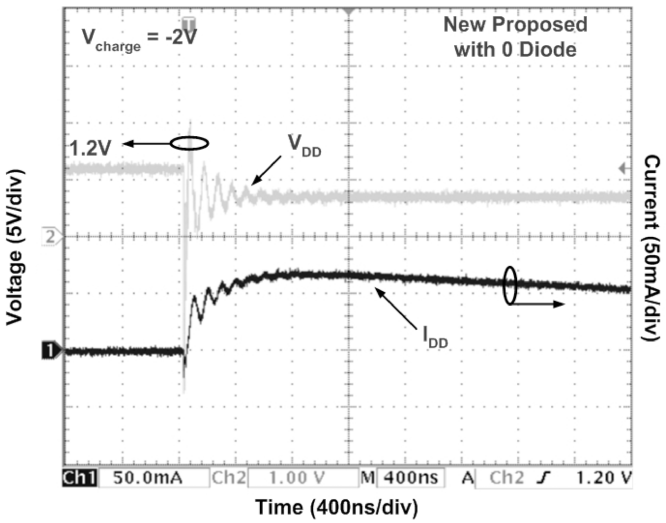


(b)

Fig. 14. Measured $V_{\rm DD}$ and $\rm I_{DD}$ waveforms on the traditional *RC*-based power-rail ESD clamp circuit under TLU measurement with $V_{\rm charge}$ of (a) $+1$ kV and (b) -1 kV.



(a)



(b)

Fig. 15. Measured $V_{\rm DD}$ and $\rm I_{DD}$ waveforms on the new proposed power-rail ESD clamp circuit with no diode under TLU measurement with $V_{\rm charge}$ of (a) $+3$ V and (b) -2 V.

The measured $V_{\rm DD}$ and $\rm I_{DD}$ transient responses of the traditional *RC*-based power-rail ESD clamp circuit under the TLU measurement with $V_{\rm charge}$ of $+1$ kV and -1 kV are shown in Fig. 14(a) and (b), respectively. In Fig. 14, the latch-on event is not occurred because the feedback mechanism is not used in the *RC*-based power-rail ESD clamp circuit. Due to the holding voltage lower than $V_{\rm DD}$, the new proposed power-rail ESD clamp circuit with zero diode suffered the latch-on issue under TLU measurement for $V_{\rm charge}$ of $+3$ V and -2 V, as shown in Fig. 15. The measured results of the new proposed power-rail ESD clamp circuits with the diodes under the TLU measurement with $V_{\rm charge}$ of $+1$ kV and -1 kV are also shown in Fig. 16. In Fig. 16, the new proposed power-rail ESD clamp circuits with adjustable holding voltage can successfully overcome transient-induced latch-on issue. The TLU levels (the minimum $V_{\rm charge}$ to induce the latch-on on $V_{\rm DD}$) among the four power-rail ESD clamp circuits are listed in Table III.

IV. Conclusion

The new capacitor-less power-rail ESD clamp circuits with adjustable holding voltage have been proposed and successfully verified in a 65 nm 1.2 V CMOS technology. The new proposed ESD-transient detection circuit adopts the capacitance-coupling mechanism to command the ESD clamp nMOS transistor. According to the measured results, the capacitor-less power-rail ESD clamp circuits with adjustable holding voltage demonstrate excellent immunity against mistrigger under the fast power-on condition, and also perform no latch-on issue under power noise and transient-induced latch-up (TLU) measurement. Moreover, the new proposed capacitor-less ESD-transient detection circuits are also area-efficient, which save layout area

TABLE III
COMPARISON ON TLU LEVELS AMONG FOUR POWER-RAIL ESD CLAMP CIRCUITS

Power-Rail ESD Clamp Circuits	Positive TLU Level	Negative TLU Level
Traditional *RC*-Based	Over +1kV	Over -1kV
New Proposed with 0 Diode	+3V	-2V
New Proposed with 1 Diode	Over +1kV	Over -1kV
New Proposed with 2 Diodes	Over +1kV	Over -1kV

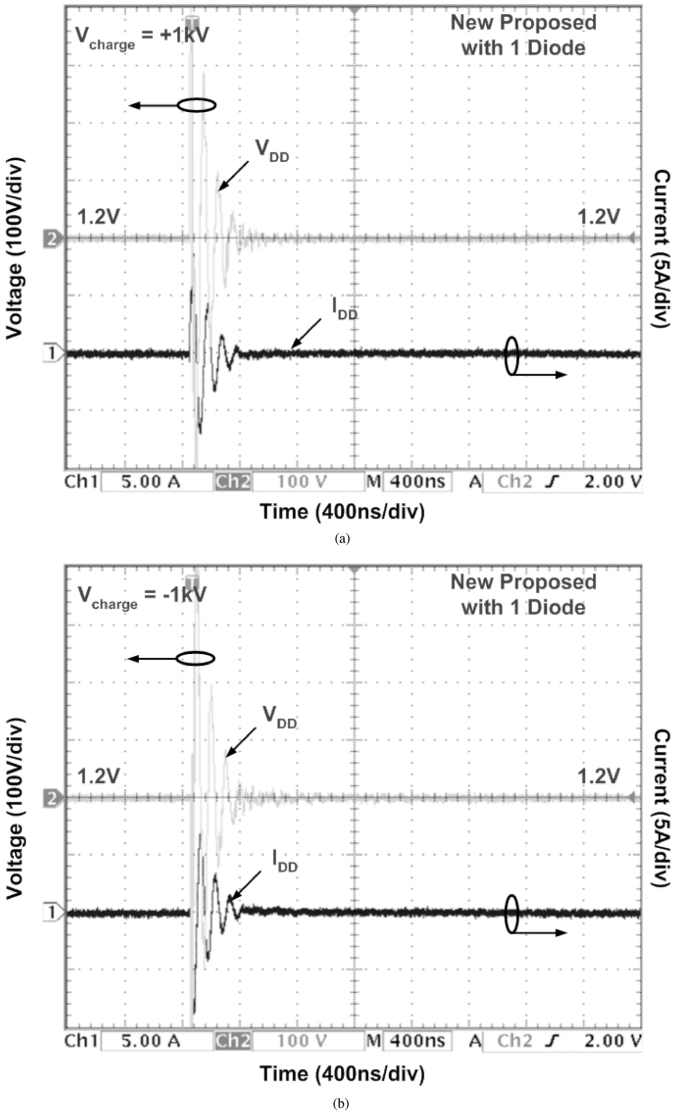


Fig. 16. Measured $V_{\rm DD}$ and $\rm I_{DD}$ waveforms on the new proposed power-rail ESD clamp circuit with one diode under TLU measurement with $V_{\rm charge}$ of (a) $+1$ kV and (b) -1 kV.

by more than 54% compared with the traditional *RC*-based ESD-transient detection circuit.

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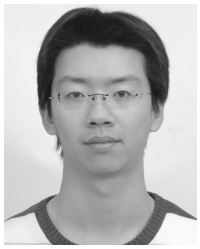

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