In-Plane Gate Transistors Fabricated by Using Atomic Force Microscopy Anode Oxidation

Tung-Hsun Chung, Shu-Han Chen, *Member, IEEE*, Wen-Hsuan Liao, and Shih-Yen Lin, *Member, IEEE*

***Abstract*—An in-plane gate transistor fabricated by using the atomic force microscopy (AFM) lithography is investigated in this letter. By performing repeated oxidation and deoxidation procedures by using the AFM for four times, two V-shaped trenches are fabricated on the prepatterned mesas to isolate the electrical terminals of the device. Without exposing the channel region to the atmosphere, the device has exhibited standard transistor current–voltage characteristics in the 0–5 V range at room temperature, which may be advantageous for the future high-speed application of the device.**

***Index Terms*—Atomic force microscopy (AFM), in-plane gate transistors.**

I. Introduction

TO ACHIEVE a higher transistor density over a single wafer in the Si industry, the photolithography technology has been rapidly developed from 0.18 μm to the current 45-nm nodes. However, with the reduced device sizes, issues like the huge gate leakage currents with thin SiO_2 gate dielectrics and the limitation of the photolithography technology have arisen [1]. To overcome the problem of the huge leakage currents resulting from the thin gate dielectrics, one approach is to develop high-κ materials to replace the SiO_x gate dielectrics. The other approach would be the development of new transistor structures without the requirement for the gate dielectrics. To achieve this goal, one possible candidate would be the in-plane gate transistor [2]. The source, drain, and gate terminals of this device structure are located on the same plane. By using e-beam lithography to fabricate the electrical isolations between the electrical terminals, the conductivity of the 2-D electron gas (2DEG) channel could be modulated by the in-plane gates such that the transistor behaviors could be observed [2], [3]. Although the device is easy to fabricate, the adoption of e-beam technology has made this approach complicated and expensive. An alternate approach to provide the electrical isolations between terminals and leave nanometer-size channels would be the atomic force microscopy (AFM) lithography (AFML). In a previous report, the transistors with in-plane gates fabricated by using the AFML operated at low temperatures have already been demonstrated [4].

In this letter, a transistor with in-plane gates fabricated by using the AFML is investigated. By performing repeated oxidation and deoxidation procedures by using AFM for four times, two V-shaped trenches could be fabricated on the prepatterned mesas. Although the trenches fabricated by using this method do not penetrate through the 2DEG channel, the electrical isolations could still be established between the terminals. The phenomenon is attributed to the depletion-induced isolations resulting from the surface-state pinning on the trench sidewalls. Without exposing the channel region to the atmosphere, the device has exhibited standard transistor current–voltage characteristics in the 0–5 V range at room temperature.

II. Experiments

The wafer discussed in this letter is prepared by RIBER C21 solid-source molecular beam epitaxy. A structure consists of a 30-nm Si-doped GaAs capping layer, a 15-nm Si-doped $Al_{0.3}Ga_{0.7}As$ donor layer, a 15-nm undoped $Al_{0.3}Ga_{0.7}As$ spacing layer, and a 200-nm buffer layer grown on a semi-insulating GaAs substrate. The doping densities for the n-type GaAs and $Al_{0.3}Ga_{0.7}As$ layers are 1.67×10^{18} and 1.15×10^{18} cm^{-3}, respectively. The Hall measurement shows that the room-temperature sheet carrier density and the electron mobility of the 2DEG channel formed in the undoped $GaAs/Al_{0.3}Ga_{0.7}As$ interface are 5.3×10^{11} cm^{-2} and 5.7×10^3 $cm^2/v \cdot s$, respectively. Before the channel definition by the AFML, a crisscross mesa with a width/depth of 20/0.1 μm is fabricated at first by using standard photolithography. The metal electrodes with Ohmic contacts to the n-type GaAs capping layer are deposited at the four ends of the crisscross mesa. The Veeco Innova AFM system is adopted for either the AFML or AFM applications in this letter. The PtIr5-coated Si tips with a cantilever spring constant of 0.2 N/m are employed for local anode oxidation (LAO) in a contact mode with an ac voltage of 10.0 V at 1 kHz [5]. For each deoxidation procedure, the wafer is dipped into 3.7% HCl aqueous solution for 90 s [6].

III. Results and Discussions

The first issue to be investigated is the depth required for the trenches to reach the electrical isolations between the terminals. According to the results obtained on the GaAs substrates, the average trench depth for a given oxidation/deoxidation

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T.-H. Chung, S.-H. Chen, and W.-H. Liao are with the Research Center for Applied Sciences, Academia Sinica, Taipei 11529, Taiwan (e-mail: s9663532@gate.sinica.edu.tw; athuda@gate.sinica.edu.tw; dwater21@hotmail.com).

S.-Y. Lin is with the Research Center for Applied Sciences, Academia Sinica, Taipei 11529, Taiwan, the Department of Photonics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the Institute of Optoelectronic Sciences, National Taiwan Ocean University, Keelung 20224, Taiwan (e-mail: shihyen@gate.sinica.edu.tw).

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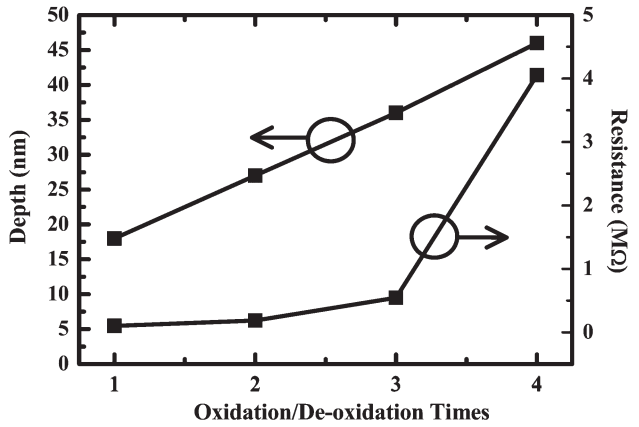

Fig. 1. Trench depth and corresponding electrical resistance between two electrodes with different oxidation/deoxidation times.

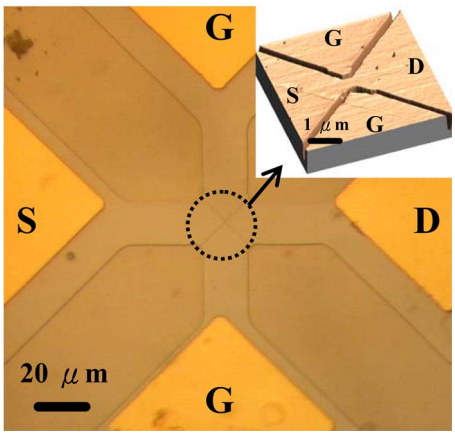

Fig. 2. Top view of the device observed under an optical microscope. The insert shows the 1×1 μm^2 AFM image of the device at the channel region.

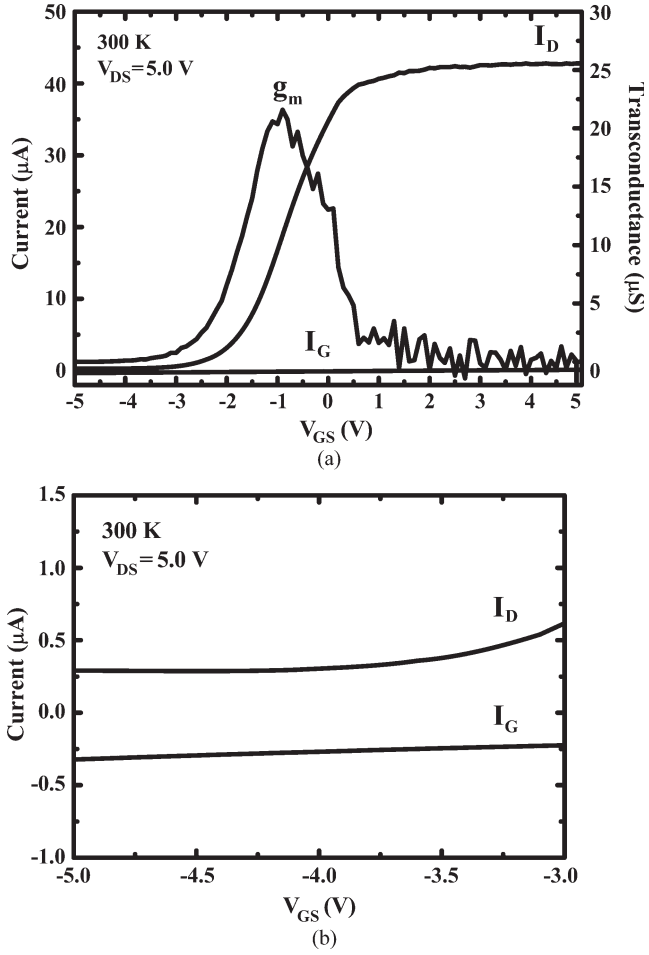

Fig. 3. (a) Room-temperature I_D, I_G, and g_m versus the $V_{\rm GS}$ characteristics at $V_{\rm GS} = -5$–5 V. (b) The I_D and I_G curves at $V_{\rm GS} = -3$ to -5 V of the device at a fixed $V_{\rm DS}$ of 5.0 V.

procedure is ~10–20 nm. Considering that the total layer thickness above the 2DEG channel is 60 nm, repeated oxidation/deoxidation procedures are expected to achieve electrical isolations for the structure. The trench depth and corresponding electrical resistance between two electrodes with different oxidation/deoxidation times are shown in Fig. 1. As shown in the figure, a linear dependence of the trench depth with oxidation/deoxidation times is observed for the sample. However, a sudden increase of the resistance from hundreds of kiloohms to several megaohms is observed after the fourth oxidation/deoxidation procedure. The trench width obtained after four times of the oxidation/deoxidation procedure is ~200 nm. Since the trench depth after four oxidation/deoxidation times is only ~45 nm, which is 15 nm above the 2DEG channel, the results suggest that, even if the trench does not penetrate through the 2DEG channel, the electrical isolations could still be achieved. The phenomenon is attributed to the depletion-induced isolations between the electrodes, which is resulted from the surface-state pinning of the trenches [7].

Based on the results discussed earlier, a transistor with in-plane gates is fabricated on this structure. Four oxidation/deoxidation times are adopted to fabricate the trenches to isolate the four electrical terminals. The top view of the device under an optical microscope is shown in Fig. 2. The AFM image of the device showing the channel region is shown in the insert of the figure. The designed channel width and length of the device are 650 and 500 nm, respectively. As shown in the figure, abrupt trenches and a well-defined channel are observed for the device. The results have demonstrated great repeatability of the AFM LAO at the same position. As discussed in the last paragraph, the trench depth is around 45–50 nm, which is 15 nm above the location of the 2DEG channel. In other words, the trenches do not penetrate through the 2DEG channel.

The room-temperature drain current (I_D)-versus-gate–source voltage $(V_{\rm GS})$ characteristics of the device at a fixed drain–source voltage $(V_{\rm DS})$ of 5.0 V are shown in Fig. 3(a). The corresponding I_G and derived transconductance (g_m) curves are also shown in the figure. As shown in the figure, the obvious ON/OFF difference is observed from the I_D–$V_{\rm GS}$ curve. The device is turned off when $V_{\rm GS}$ is lower than -3.0 V and saturated when $V_{\rm GS}$ is higher than 2.0 V. The results suggest that, when a negative $V_{\rm GS}$ is applied, the electrons in the 2DEG channel would be depleted. The channel is fully depleted of electrons when $V_{\rm GS}$ is lower than -3.0 V. In this case, the device is in the OFF state. When a positive $V_{\rm GS}$ is applied to this device, the depletion regions in the device channel which is resulted from the surface-state pinning near the trench sidewalls would be gradually compensated by the injected I_D currents. When

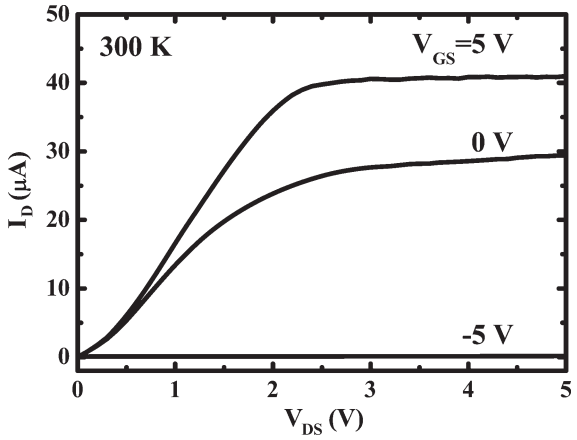

Fig. 4. Room-temperature I_D–$V_{\rm DS}$ curves of the device at $V_{\rm GS} = -5.0,\ 0.0,$ and 5.0 V.

$V_{\rm GS}$ is higher than 2.0 V, the 2DEG channel would be fully opened. In this case, the device is in the ON state. The transconductance of the device derived through the I_D–$V_{\rm GS}$ curve has shown a maximum value of 20 μS, which is much smaller than that of the conventional transistors. The phenomenon is attributed to the long and wide channel of the crisscross mesa. A reduction in the source/drain electrode distance is necessary in the future to reduce the series resistance. The air-bridge process may also help to reduce the parasitic capacitance below the metal [8]. In this case, the effective device area can be reduced, which is advantageous for the high-speed operation of this device.

Moreover, shown in Fig. 3(a) are the gate currents (I_G) under different $V_{\rm GS}$'s. When the device is under the ON state, the low gate currents suggest that, even if the trenches do not penetrate through the 2DEG channel, the electrical isolations between the terminals could still be achieved with the electron depletion in the 2DEG channel which is resulted from the surface-state pinning. However, when the device is in the OFF state, I_D and I_G are of the same value but with different signs. The I_D and I_G curves of the device at $V_{\rm GS} = -3$ to -5 V are shown in Fig. 3(b). The results suggest that the leakage current is mainly from the gate terminals. In this case, although the trenches may act as electrical isolations in the ON state, the leakage currents from the gates are still observed in the OFF state since the trenches do not penetrate through the 2DEG channel.

The room-temperature I_D–$V_{\rm DS}$ curves of the device at $V_{\rm GS} = -5.0,\ 0.0,$ and 5.0 V are shown in Fig. 4. As shown in the figure, standard transistor curves with flat saturation regions are observed for this device. The ON/OFF ratio of the device at $V_{\rm GS} = 5.0$ and -5.0 V and $V_{\rm DS} = 5.0$ V has reached 290. Further improvement in thinning the layer structures to enhance the electrical isolation with a fixed trench depth may help to increase the ON/OFF ratio in the future. The other remaining issue is the actual channel width of the device. Since the surface-state pinning effect plays an important role in the electrical isolation for the terminals, the effect would also influence the actual channel width of the device. Since the 2DEG channel is not exposed to the atmosphere for this device, the electron mobility and the sheet carrier density in the channel could be assumed to be the same as the value obtained by the Hall measurements. In this case, by using the equation $R = L/(q\mu_n N_D W)$, where R is the resistance of the device at the linear region, μ_n and N_D are the electron mobility and the sheet carrier density, respectively, and L and W are the channel length and channel width, respectively, an estimate of the effective channel width could be obtained [9]. The effective channel width of the device obtained by using this equation at $V_{\rm GS} = 0$ V is 13.7 nm, assuming that the channel length is 500 nm. Although the resistance contribution of the crisscross mesa is not excluded in this calculation, the results suggest that the depletion region would spread 200–300 nm into the channel region from a single side of the trench. The results have provided a supporting evidence that the electrical isolation could be achieved through the electron depletion which resulted from the surface-state pinning when the trenches do not penetrate through the 2DEG channel.

IV. Conclusion

In conclusion, a transistor with in-plane gates fabricated by using the AFML is investigated. Without exposing the channel region to the atmosphere, the device has exhibited standard transistor current–voltage characteristics in the 0–5 V range at room temperature, which may be advantageous for the future high-speed application of the device. The development of this device is advantageous for the practical applications of nanodevices.

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