A Novel p-n-Diode Structure of SONOS-Type TFT NVM With Embedded Silicon Nanocrystals

Tsung-Yu Chiang, William Cheng-Yu Ma, Yi-Hong Wu, Kuan-Ti Wang, and Tien-Sheng Chao

***Abstract*—In this letter, for the first time, a novel p-n-diode (PND) structure of SONOS-type thin-film transistor (TFT) nonvolatile memory (NVM) with embedded silicon nanocrystals (Si-NCs) in the silicon nitride layer using an *in situ* method is successfully demonstrated. This novel structure has many advantages, including high density and suitability for 3-D circuit integration. Hot-electron injection and hot-hole injection are used as the program and erase methods, respectively. The sensing current of the three-terminal PND-TFT NVM is 10^{-7} A by the band-to-band tunneling current. A much larger memory window (> 12 V) and good data retention time ($> 10^8$ s for 12% charge loss) are exhibited. The device appears to have great potential for system-on-panel applications.**

***Index Terms*—Band-to-band tunneling (BTBT), nonvolatile memory (NVM), p-n diode (PND), silicon nanocrystal (Si-NC), thin-film transistor (TFT).**

I. Introduction

NONVOLATILE memories (NVMs) have attracted much attention in electronic products. The demands of NVMs include ultrahigh density, large memory window, and good data retention. The tunneling oxide of floating-gate (FG) memory is difficult to scale below 7 nm, and FG memory experiences serious FG interference as the device is scaled down [1], [2]. Thus, conventional FG memories face the scaling-down issue and need to be improved.

Recently, much effort has been devoted to exploring SONOS memories as an alternative to FG memories [3]–[7]. SONOS memories provide many advantages over conventional FG memories, including no FG coupling effect, better immunity to drain-induced turn-on effect, higher density, elimination of SILC, and ease of vertical scale-down [3]–[7]. However, a traditional MOSFET encounters problems as it is scaled down, including serious short-channel effect, larger DIBL, and acute punchthrough effect [8]–[10]. For these reasons, it is difficult to scale down and achieve high density with single-crystal MOSFET SONOS memory devices. Accordingly, in order to achieve high density, thin-film transistors (TFTs) and special structures have been proposed and reported [11]–[13].

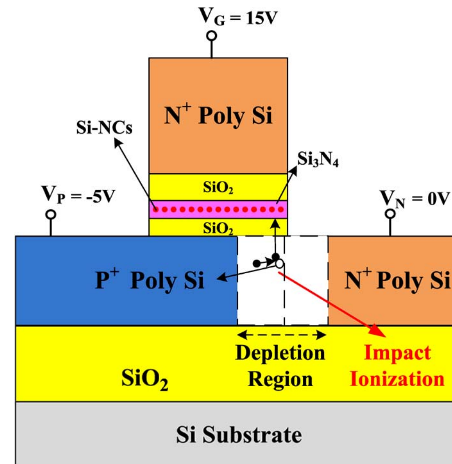

Fig. 1. Cross-sectional scheme of the PND-TFT memory structure with embedded Si-NCs using an *in situ* method.

In this letter, for the first time, a p-n-diode (PND) structure of SONOS-type TFT memory with embedded silicon nanocrystals (Si-NCs) with good data retention using an *in situ* method has been successfully fabricated and proposed. The novel structure avoids the disadvantages of traditional single-crystal MOSFET SONOS-type memory devices, including serious SCE, larger DIBL, and acute punchthrough effect. Furthermore, with embedded Si-NCs in the nitride layer using the *in situ* method, the deep-trapped level can be created in the Si-NCs and the interface between the Si-NCs and silicon nitride [14]. Consequently, the data retention is improved, and the memory window is enhanced. For the aforementioned reasons, the PND-TFT memory with embedded Si-NCs in the nitride layer shows promise for future applications in multilevel operation, high-density, system-on-panel (SOP), and system-on-chip (SOC) technologies.

II. Experimental Procedure

A cross section of the PND-TFT memory device with embedded Si-NCs in the nitride layer is shown in Fig. 1. First, a 500-nm thermal oxide was grown on a 6-in silicon wafer using a furnace system. An undoped polysilicon layer with a thickness of 100 nm was deposited by low-pressure chemical vapor deposition (LPCVD). After patterning and defining the active regions, the active regions were implanted with boron (10 keV at 5×10^{15} cm^{-2}). Then, to form the ONO trilayer, an 8.5-nm tetraethyloxysilane (TEOS) tunneling oxide was

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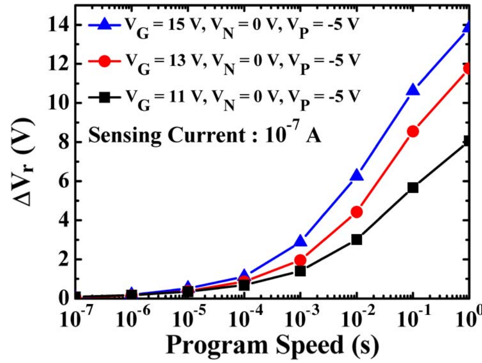

Fig. 2. Program speed characteristics of the PND-TFT memory at different operating voltage biases.

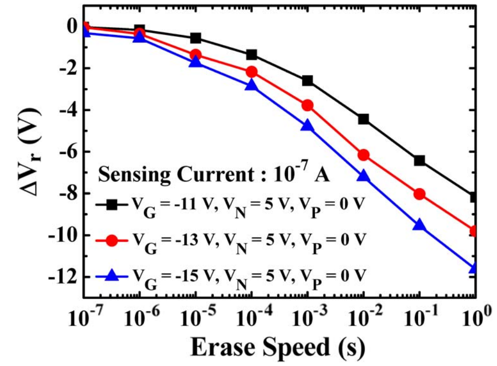

Fig. 3. Erase speed characteristics of the PND-TFT memory at different operating voltage biases.

deposited by LPCVD. To sandwich Si-NCs in the silicon nitride layer, a Si_3N_4 (4-nm)/Si-NCs (by using SiH_2Cl_2, 10 sccm, at 780 °C for 30 s)/Si_3N_4 (4-nm) multilayer of the trapping layer was deposited using an *in situ* method by LPCVD [14]. A TEOS blocking oxide of about 15 nm was deposited by LPCVD. Next, a 200-nm n^+ polysilicon as the gate electrode was deposited and implanted with phosphorous (35 keV at 5×10^{15} cm^{-2}). A 100-nm TEOS oxide was deposited as a hard-mask layer. Then, after gate electrode patterning and definition, the n^+ active regions were implanted with arsenic (50 keV at 1×10^{16} cm^{-2}) after the photolithography process. Subsequently, the PND-TFT memory was annealed in N_2 gas at 950 °C for 10 s. The 500-nm TEOS oxide of the passivation layer was deposited, and the contact hole was patterned. Finally, a 500-nm Al pad was deposited and patterned to finish the fabrication of the PND-TFT memory. The device with a polygate length (L) and an active width (W) of 10 and 10 μm, respectively, was measured.

III. Results and Discussion

The PND-TFT memory was programmed and erased by using hot-electron and hot-hole injection mechanisms, respectively. However, hot carriers were produced using the impact ionization method. In the depletion region, the electrons were accelerated and obtained energy owing to the horizontal electric field under junction bias. A lot of hot-electron–hole pairs can be generated in the depletion region due to impact ionization of the accelerated electrons, as shown in Fig. 1. Figs. 2 and 3 show the program and erase speed characteristics under different operating biases. The program conditions were set at $V_G = 11, 13, 15$ V, $V_N = 0$ V, and $V_P = -5$ V, while the erase conditions were set at $V_G = -11, -13, -15$ V, $V_N =$ 5 V, and $V_P = 0$ V. In read mode, the sweeping of V_G generates a band-to-band tunneling (BTBT) current under a reverse bias of the p-n junction $(V_N = 0.3$ V). The BTBT current represents the sensing current. Read voltage (V_r) is defined as the applied gate voltage when the sensing current is 10^{-7} A in read mode. Memory window is defined as the V_r shift (ΔV_r) between the programmed and erased states. The ratio of the current at program state and the current at erase state is about three orders of magnitude. Under programming conditions, the electrons can tunnel from the P^+ valence band to the depletion region

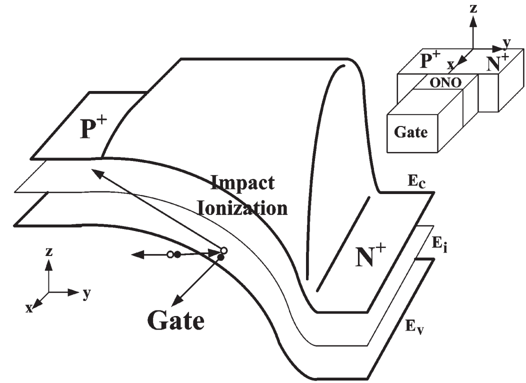

Fig. 4. Three-dimensional band diagram scheme of the PND-TFT memory structure with embedded Si-NCs at programming state.

along the y-axis by BTBT, as shown in Fig. 4. The tunneling electrons were accelerated by the horizontal electric field at reverse junction bias (at $V_P = -5$ V). The hot electron can be injected into the trapping layer and be trapped away from the depletion region along the x-axis by a positive gate voltage bias, as shown in Fig. 4. However, the hot hole can also inject into the trapping layer and be trapped by a negative gate voltage bias. The larger gate voltage bias tends to result in faster program and erase speeds owing to the increased vertical electric filed. After programming, the 12-V shift of V_r was found. The lager memory window (12 V) is sufficient for the application of multilevel operations. The programming speed and drain disturbance should be traded off. So far, we are still trying to optimize the operation voltage. In this letter, the programming voltage $(V_G = 15$ V$, V_N = 0$ V, and $V_P = -5$ V) can be shifted by more than 3 V in 1 ms. According to the present literature, the programming speed of our PND is comparable [15].

The data retention characteristics of the PND-TFT memory device at room temperature are shown in Fig. 5. The program and erase states were set as the PND-TFT memory after programming at $V_G = 15$ V, $V_N = 0$ V, $V_P = -5$ V, 1 s and erasing at $V_G = -15$ V, $V_N = 5$ V, $V_P = 0$ V, 1 s, respectively. The charge loss was below 5% for 10^4 s, as shown in Fig. 5. Extrapolated to 10^8 s, it exhibits only a 12% charge loss. The larger memory window and good data retention of the PND-TFT memory are very suitable for applications of high density, multilevel operation, and SOP, as well as 3-D circuit integration.

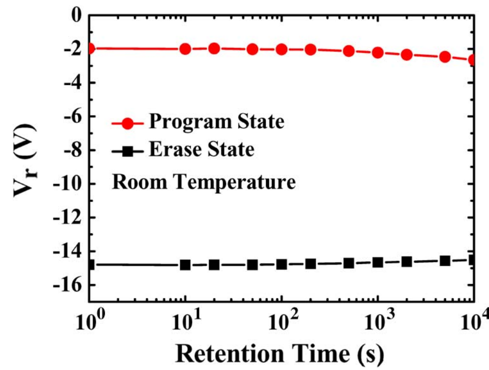

Fig. 5. Data retention characteristics of the PND-TFT memory when programming $\Delta V_t = 12$ V at room temperature.

IV. Conclusion

In this letter, a PND-TFT NVM with embedded Si-NCs in a novel structure, fabricated using an *in situ* method, has been reported and demonstrated for the first time. The PND-TFT memory may well represent a breakthrough in the problems involved in scaling down such devices. At the same time, the PND-TFT memory, which achieves 3-D multilayer stack memory, can carry out ultrahigh-density memory generation. The novel structure has excellent characteristics in terms of larger memory windows, good P/E efficiency, and longer data retention time. Therefore, the PND-TFT memory is an excellent candidate for SOP and SOC applications in the future.

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