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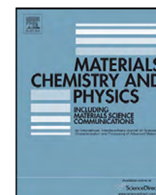

Effect of Ni residues on the performance and the uniformity of nickel-induced lateral crystallization polycrystalline silicon nanowire thin-film transistors

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ABSTRACT

High performance nickel-induced lateral crystallization (NILC) polycrystalline silicon (poly-Si) nanowire (NW) thin-film transistors (TFTs) were fabricated. The phosphorous-doped amorphous silicon (α-Si)/chem-SiO_2 films were employed as Ni-gettering layers to investigate effect of Ni residues on the performance and the uniformity of NILC poly-Si NW TFTs. It was found that the performance and the uniformity of NW TFTs were greatly improved after Ni-gettering process.

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1. Introduction

Low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted considerable interest for their application in active-matrix liquid crystal displays (AMLCDs) on cheap glass substrate [1]. Recently, high performance poly-Si nanowire (NW) TFTs have been fabricated by nickel-metal induced lateral crystallization (NILC) [2,3]. Since NILC grain could be formed parallel to the channel direction, it becomes feasible to form Si NWs with nearly monocrystalline structures [4]. Unfortunately, poly-Si/oxide interfaces and poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates, thus increasing leakage current and shifting the threshold voltage [5–9]. Besides, residual α-Si pockets among poly-Si grains also lead to increased leakage [5]. Since the poly-Si/oxide interfaces/volume ratio of NW TFTs was much higher than that of tradition NILC TFTs, effect of Ni residues on the performance of NILC NW TFTs should be investigated. Several metal gettering methods have been employed to reduce Ni concentration inside NILC TFTs [10–13]. In this study, phosphorus-doped α-Si (p-α-Si) film and chemical SiO_2 (chem-SiO_2) layer were used as gettering layers. Effects of Ni residues on the performance and the uniformity of NILC NW TFTs were investigated.

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2. Experimental

Three kinds of NWs were investigated in this study. One was “SPC” NW fabricated by solid phase crystallization (SPC), and the others were “NILC” and “GETR” NWs fabricated by NILC method without and with Ni-gettering process, respectively.

An approach for making NILC NW channels similar to Ref. [14] was followed. A gate (n^+ poly-Si) was first formed on a Si substrate capped with an oxide layer, followed by the deposition of a chemical vapor deposition (CVD) oxide layer serving as the gate dielectric. An α-Si layer was then deposited by low-pressure CVD. The top view of the device structure is shown in Fig. 1(a). Before NILC process, 5-nm-thick Ni lines were selectively deposited on the α-Si films using lift-off method [13]. NILC length is about 17 μm after lateral crystallization at 540 °C for 24 h, as shown in Fig. 1(b). The unreacted Ni was removed by a mixed solution of H_2SO_4 and H_2O_2. NILC poly-Si films were then dipped into 1% diluted hydrogen fluoride (DHF) solution to remove top annealing oxide, as illustrated in Fig. 1(c).

As for GETR film, an additional Ni-gettering process [13] was carried out to reduce the Ni concentration in NILC film. The gettering structure (p-α-Si/chem-SiO_2) was shown in Fig. 1(d). After gettering at 550 °C for 12 h, p-α-Si and chem-SiO_2 layers were removed using 5% tetra-methyl ammonium hydroxide (TMAH) and 1% DHF solution, respectively. As for SPC film, sample was crystallized by SPC at 600 °C for 24 h.

For comparison, NILC and SPC films were also subjected to an extended heat treatment as Ni-gettering condition. Subsequently, source/drain (S/D) implant was performed. The implant energy was kept low so that most implanted dopants were located near the top surface of the Si layer. S/D photoresist patterns were then formed on the substrate by a standard lithography step. These three poly-Si films were then subjected to an anisotropic etching to form poly-Si spacers (NWs) in a self-aligned manner.

3. Results and discussion

Fig. 2 shows the cross-sectional transmission electron microscopy (TEM) images of NILC NW TFT. Both the vertical

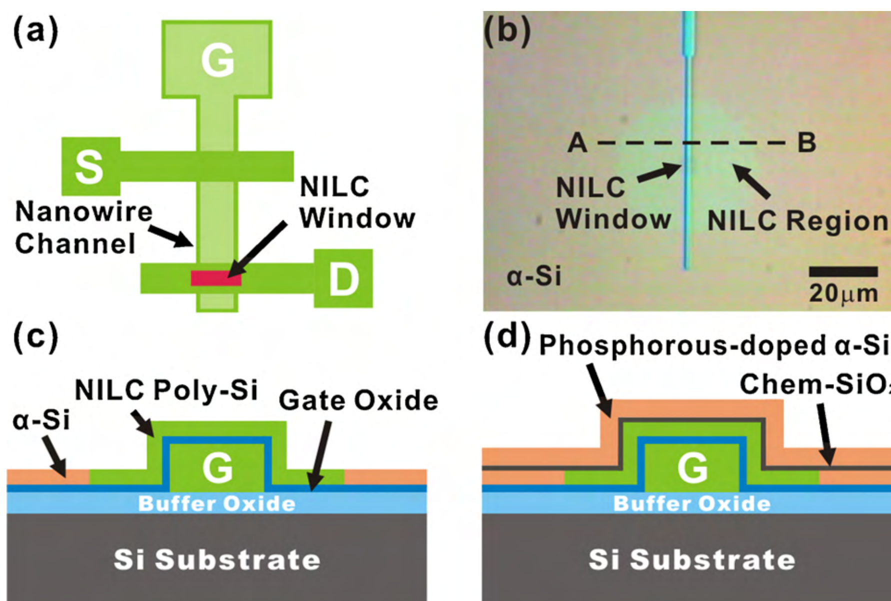

Fig. 1. (a) Top view of the proposed NILC poly-Si NW TFT structure and (b) optical microscopy image of NILC poly-Si after annealing at 540 °C for 24 h. (c) Cross-sectional view along the dashed line A to B in (b). (d) Ni-gettering structure.

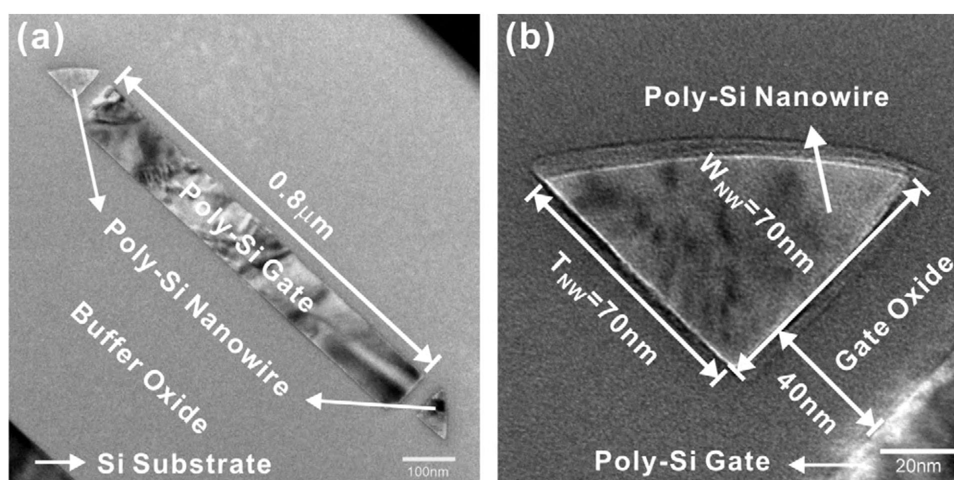

Fig. 2. (a) Cross-sectional TEM image of the NILC NW TFT with a couple of poly-Si NW channels and (b) the high magnification of poly-Si NW in (a).

width (W_{NW}) and the horizontal sidewall thickness (T_{NW}) are about 70 nm. The gate oxide is 40 nm thick, as illustrated in Fig. 2(b).

The TFT devices with a couple of NW channels have a nominal channel (L) of 0.8 μm and an effective channel width (W) of 140 nm ($2 \times W_{NW}$). Typical $I_D - V_G$ transfer characteristics of NW TFTs at $V_D = 0.5$ and 3 V are compared in Fig. 3. The measured and extracted key device parameters are summarized in Table 1. The threshold voltage (V_{TH}) is defined at a normalized drain current of $I_D = (W/L) \times 100$ nA at $V_D = 0.5$ V. The subthreshold swing (S.S.) is extracted at $V_D = 0.5$ V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at $V_D = 0.5$ V. The leakage current (I_{OFF}) is defined as the minimum drain current along the gate voltage at $V_D = 3$ V.

As shown in Table 1, GETR and NILC TFTs reveal higher μ_{FE}, better subthreshold swing (S.S.), and higher I_{ON}/I_{OFF} ratio compared with SPC TFTs. This is because the NILC grain is large, needlelike, and parallel to the channel [2]. Besides, Table 1 also indicates the performance of NILC TFTs was improved after Ni-gettering process. GETR TFTs had lower I_{OFF}, higher I_{ON}/I_{OFF} ratio,

Table 1
Average device characteristics of NW TFTs with standard deviations.

Parameters ($W/L = 2 \times 70$ nm/0.8 μm)	NILC NW TFTs	GETR NW TFTs	SPC NW TFTs
μ_{FE} (cm^2 V^{-1} s^{-1}) at $V_D = 0.5$ V	117.32 ± 17.75	140.73 ± 38.21	24.50 ± 4.14
S.S. (mV dec^{-1}) at $V_D = 0.5$ V	395 ± 66	418 ± 63	694 ± 76
V_{TG} (V) at $V_D = 0.5$ V	0.19 ± 0.40	0.35 ± 0.22	4.12 ± 0.21
I_{ON}/I_{OFF} ratio (10^6) at $V_D = 03$ V	1.4 ± 1.2	3.2 ± 1.0	0.4 ± 0.1
I_{OFF} (pA) at $V_D = 3$ V	81.86 ± 95.71	13.03 ± 5.41	6.37 ± 2.50

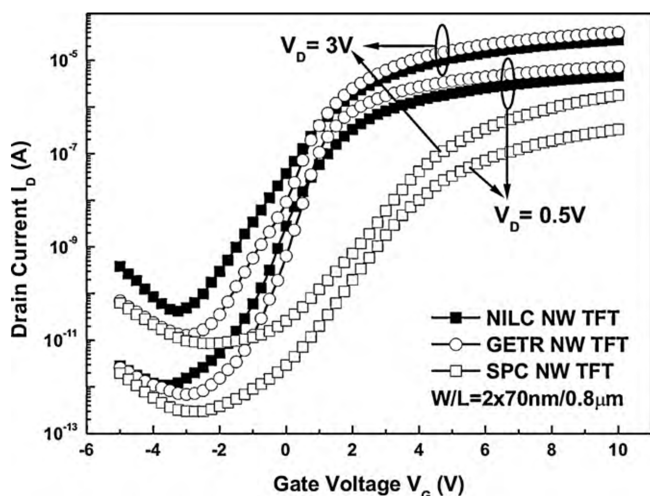

Fig. 3. Comparison of transfer characteristics among SPC, NILC, and GETR NW TFTs.

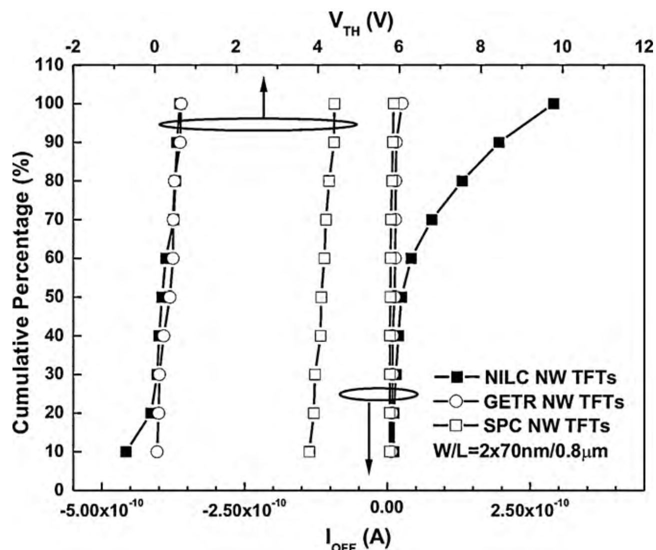

Fig. 4. Ten TFTs were measured in each case in threshold voltage and leakage current to investigate the device-to-device variation.

and higher μ_{FE} compared with NILC TFTs. This improvement indicates the trap state density (N_{trap}) was effectively reduced using phosphorous-doped α-Si gettering processes. The trap state density of the TFTs was extracted using Levinson and Proano's method, which can estimate the N_{trap} from the slope of the linear segment of $\ln[I_{DS}/(V_{GS}-V_{FB})]$ vs. $1/(V_{GS}-V_{FB})^2$ at low V_{DS} and high V_{GS}, where V_{FB} is defined as the gate voltage that yields the minimum drain current at $V_{DS}=0.1$ [15]. The trap density of GETR TFTs is $2.52\times10^{12}\,cm^{-2}$, which is less than that of NILC TFTs ($3.95\times10^{12}\,cm^{-2}$). Since GETR grains (boundaries) were similar to NILC grains, the reduction in N_{trap} values implies that Ni-related defects have been reduced using phosphorous-doped α-Si/chem-SiO_2 gettering structure [10,16–18].

Besides, as shown in Table 1, the V_{TH} of the NILC TFT is 0.19 V, which is less than that of GETR TFT (0.35 V). This is because Ni residues could cause a high density of positive charge at the oxide/NILC poly-Si interface [19]. The negative shift of V_{TH} of NILC TFT was due to the presence of these positive charges and nickel-related donor-like defects.

Similar results have been reported by Yoon et al. [20], who introduced Ni into the α-Si at a dosage of 5×10^{13} atoms cm^{-2} and followed by laser annealing (L-MIC). They found the leakage current and mobility of TFTS were greatly improved. The difference between that and this study is that Ni was introduced by ion implantation and that 1 h H_2 plasma treatment was used to passivate defects in any remaining a-Si pockets [5]. Combining our results and those of Refs. [5,20], it suggests that two regimes may exist in reducing leakage current in MIC poly-Si TFTs. One is the regime at high Ni dose where a benefit exists in removing the excess Ni. The other is the regime at lower Ni dose where leakage due to any remaining non-passivated a-Si pockets [5].

The other important issue of poly-Si TFTs is their uniformity. Fig. 4 shows threshold voltage and leakage current of 10 NW TFTs measured in each case to study device-to-device variation. It was found that the uniformity of SPC and GETR TFTs was much better than that of NILC TFTs. This is because Ni residues were randomly trapped at poly-Si grain boundaries and poly-Si/oxide interfaces [5–10]. With the reduction of the Ni residues, the influence of Ni residues on the performance of NILC NW TFTs was greatly reduced.

Presently, however, the performance of our TFT as 5 V was very unstable, because at 5 V the current density of the nanowire (NW) TFTs was too high leading to failure of most devices. This topic invites further investigation.

4. Conclusion

In this study, high performance NILC NW poly-Si TFTs with a couple of 70-nm NW channels were fabricated, and then improved by Ni-gettering process. The phosphorous-doped α-Si/chem-SiO_2 films were employed as Ni-gettering layers to reduce Ni residues within NILC poly-Si film. After Ni-gettering process, the performance of NILC NW TFTs was improved. GETR NW TFTs had lower I_{OFF}, higher I_{ON}/I_{OFF} ratio, and higher μ_{FE} compared with NILC NW TFTs. The uniformity of GETR NW TFTs was better than that of NILC NW TFTs. This is because Ni and $NiSi_2$ precipitates were randomly trapped at poly-Si/gate oxide interfaces and poly-Si grain boundaries. With the gettering of the Ni residues, the uniformity of NILC NW TFTs was improved in terms of threshold voltage and leakage current.

Acknowledgements

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References

[1] M. Stewart, R.S. Howell, L. Pires, M.K. Hatalis, IEEE Trans. Electron Devices 48 (2001) 845.
[2] C.J. Su, H.C. Lin, T.Y. Huang, IEEE Electron Device Lett. 27 (2006) 582.
[3] C.W. Chang, S.F. Chen, C.L. Chang, C.K. Deng, J.J. Huang, T.F. Lei, IEEE Electron Device Lett. 29 (2008) 474.
[4] J. Gu, S.Y. Chou, N. Yao, H. Zandbergen, J.K. Farrer, Appl. Phys. Lett. 81 (2002) 1104.
[5] P.J. van der Zaag, M.A. Verhejen, S.Y. Yoon, N.D. Young, Appl. Phys. Lett. 81 (2002) 3404.
[6] G.A. Bhat, Z. Jin, H.S. Kwok, M. Wong, IEEE Electron Device Lett. 20 (1999) 97.
[7] Z. Jin, K. Moulding, H.S. Kowk, M. Wong, IEEE Electron Device Lett. 20 (1999) 167.
[8] D. Murley, N. Young, M. Trainor, D. McCulloch, IEEE Trans. Electron Devices 48 (2001) 1145.
[9] G.A. Bhat, H.S. Kwok, M. Wong, Solid State Electron. 44 (2000) 1321.
[10] C.M. Hu, Y.S. Wu, C.C. Lin, IEEE Electron Device Lett. 28 (2007) 1000.
[11] C.Y. Hou, Y.S. Wu, Electrochem. Solid-State Lett. 9 (2006) H65.
[12] B.M. Wang, Y.S. Wu, Electrochem. Solid-State Lett. 12 (2009) J14.
[13] B.M. Wang, Y.S. Wu, J. Electron. Mater. 38 (2009) 767.

[14] H.C. Lin, M.H. Lee, C.J. Su, T.Y. Huang, C.C. Lee, Y.S. Yang, IEEE Electron Device Lett. 26 (2005) 643.
[15] R.E. Proano, R.S. Misage, D.G. Ast, IEEE Trans. Electron Devices 36 (1989) 1915.
[16] T.K. Kim, T.H. Ihn, B.I. Lee, S.K. Joo, Jpn. J. Appl. Phys. 37 (1998) 4244.
[17] K.R. Olasupo, M.K. Hatalis, IEEE Trans. Electron Devices 43 (1996) 1218.
[18] M. Yazaki, S. Takenaka, H. Ohshima, Jpn. J. Appl. Phys. 31 (1992) 206.
[19] Y. Lee, S. Bae, S.J. Fonash, IEEE Electron Device Lett. 26 (2005) 900.
[20] S.Y. Yoon, N. Young, P.J. van der Zaag, D. McCulloch, IEEE Electron Device Lett. 24 (2003) 22.