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A study on low temperature transport properties of independent double-gated poly-Si nanowire transistors

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Abstract
Employing mix-and-match lithography of I-line stepper and e-beam direct writing, independent double-gated poly-Si nanowire thin film transistors with channel lengths ranging from 70 nm to 5 μm were fabricated and characterized. Electrical measurements performed under cryogenic ambient displayed intriguing characteristics in terms of length dependent abrupt switching behavior for one of the single-gated modes. Through simulation and experimental verification, the root cause for this phenomenon was identified to be the non-uniformly distributed dopants introduced by ion implantation.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

To maintain the momentum of CMOS scaling, multiple-gated nanowire (NW) devices have been proposed as one of the most promising future transistor structures [1], due to the better gate controllability to suppress short channel effects (SCE). Also their unique structure makes them suitable for many applications in nanoelectronics and optoelectronics [2, 3]. The paradigm shift creates wholy new concepts and perspectives on device physics, and possibilities that conventional planar counterparts have yet to offer. From a microscopic point of view, this kind of low-dimensional structure is suitable for studying quantum-mechanical effects. In particular, many reports have focused on the carrier transport properties in NW devices, for which well-established theories of three- or two-dimensional materials are no longer appropriate. Quantum confinement, sub-band splitting, and surface and interface relaxation [4–6], etc are among a plethora of effects that must be taken into account in order to correctly interpret the NW characteristics, including the unexpected increase of threshold voltage (V_{TH}) with reduced NW width [7], the oscillation of drain current and mobility [5], and the reduced Stark effect [8]. Recently, dopant distribution has been identified as another major factor influencing the carrier conduction behavior in ultra-short NW devices [9]. In this paper, to investigate the underlying transport mechanism of our previously proposed independent double-gated NW polycrystalline silicon (poly-Si) thin film transistors [10], devices with channel lengths (L) ranging from 70 nm to 5 μm were fabricated and characterized using mix-and-match lithography of I-line stepper and e-beam direct writing methods. Electrical characterization performed in the temperature (T) range 300–78 K showed abnormal switching phenomena for one of the single-gated modes, with a very steep subthreshold swing (SS) that completely disappeared when altering the gate doping technique. It was also found that such a phenomenon is related to a number of structural parameters. A simple model based on the process of electron trapping and detrapping in the channel is proposed.

2. Device structures and fabrication

By cleverly forming a cavity on two sides of a nitride/Si/nitride stack through selective etching of the sandwiched Si, followed by refilling with an active layer, we previously demonstrated a novel and simple method for fabricating devices with decananometer NW dimensions using an optical I-line

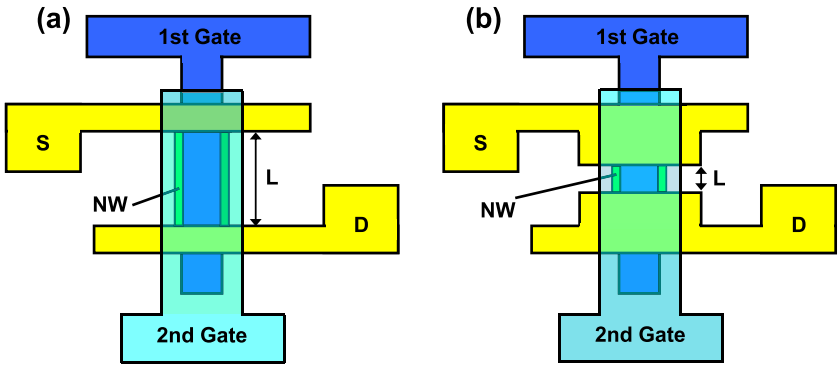

Figure 1. Layout of the device fabricated using (a) I-line only and (b) mix-and-match between e-beam and I-line. L defines the channel length, which is greater than 0.4 μm in (a) and smaller than 100 nm in (b).

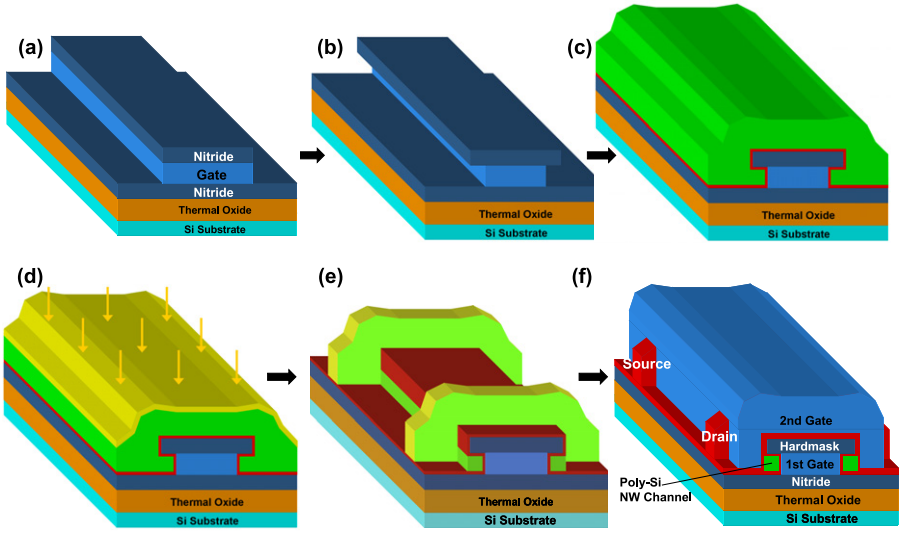

Figure 2. Schematic process flow for the double-gated NW devices with long and short L. (a) First gate stack (100 nm *in situ* doped n^+ poly) patterning. (b) Selective plasma etching of the first gate using chlorine (Cl_2) and sulfur hexafluoride (SF_6) gases. (c) First gate dielectric (15 nm TEOS oxide) and 100 nm amorphous Si layer deposition by LPCVD. (d) Recrystallization of amorphous Si performed at 600 °C for 24 h in N_2 ambient and S/D implantation by phosphorus with 5×10^{15} cm^{-2} dosage and 15 keV energy. (e) Definition of S/D and NW channels by Cl_2 dry etching. For long channel devices patterned by I-line, L is larger than 0.4 μm; for short channel devices patterned by e-beam, L is smaller than 100 nm. (f) Second gate stack deposition (5 nm TEOS oxide and 100 nm implanted n^+ poly) by LPCVD and patterning.

stepper [10, 11]. The layout and process flow are shown in figures 1(a) and 2, respectively. To overcome the L limit set by the resolution of the I-line stepper, which is only 0.4 μm, while maintaining a low cost approach, a slightly modified fabrication process, adding e-beam direct writing, was adopted in this study to achieve sub-100 nm L, with the layout given in figure 1(b). It is worth mentioning that this new approach requires only one additional lithographic step, and can be easily integrated with the original version on the same wafer. In short, the new version is only different in the manner L is defined. That is, instead of directly forming source/drain (S/D) and the channels in a single step, in the newly proposed method, mesa-isolation of the active layer was first performed, followed by another patterning to simultaneously define S/D and the channels using e-beam writing, which in turn also determined L.

3. Electrical characteristics

Plane-view and cross-sectional transmission electron microscope (TEM) images of the fabricated device are shown in figures 3(a) and (b), respectively. It can be seen from the plane-view picture that the grain sizes of the first and second gates are quite different which can be ascribed to the difference in doping methods [12]. Namely, the first gate of larger grain size is of *in situ* doped n^+ poly-Si, while the second gate with smaller grain size is of implanted n^+ poly-Si. Note that the dielectrics for the first and second gates are 15 nm and 5 nm tetraethyl orthosilicate (TEOS) oxide, respectively, while the thickness of NW (or the width between the two gate dielectrics) is 23 nm.

Transfer characteristics as a function of T for a device with $L = 70$ nm are shown in figure 4. Because of the independent double-gated feature, there are three feasible

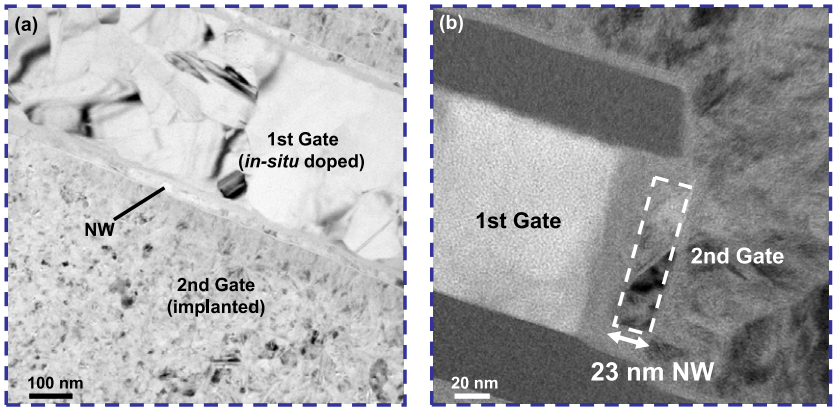

Figure 3. (a) Plane- and (b) cross-sectional view images of a fabricated device showing a 23 nm thick NW channel surrounded by the first and second gates. The marked grain size discrepancy between the first and second gates is a consequence of the different doping methods implemented: the first gate uses *in situ* doping while the second gate uses implantation.

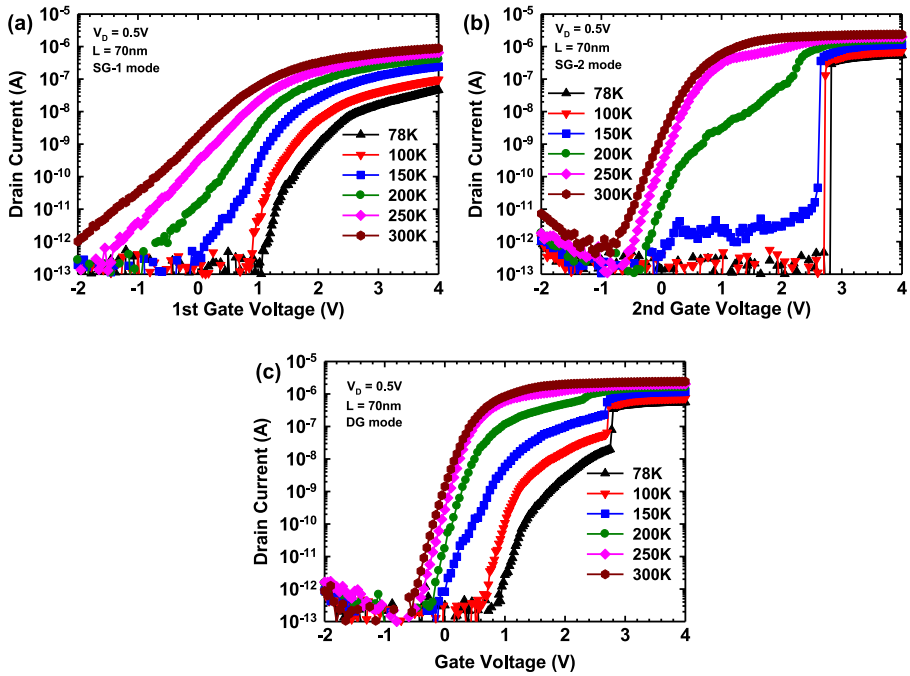

Figure 4. Transfer characteristics as a function of temperature for a device with 70 nm channel length in (a) SG-1, (b) SG-2, and (c) DG modes. The behavior of the SG-1 mode is in accordance with the thermionic emission model while the SG-2 mode starts to exhibit a very steep SS when T is below 150 K. An abrupt increase of I_D for the DG mode at 100 and 78 K is caused by the channel controlled by the second gate.

operation modes, i.e., SG-1, SG-2, and DG. Specifically, SG-1 and SG-2 modes refer to, respectively, the scheme when the first or second gate serves as the driving gate with the other gate electrode grounded. While for DG mode the two gates are tied together to drive the device simultaneously. As compared with single-crystalline Si, carrier transport in poly-Si tends to experience additional scattering from trapping centers in the grain boundaries, resulting in carrier depletion and the formation of potential barriers that impede carrier motion from one grain to another [13]. Therefore, thermionic emission over these energy barriers is usually considered as the major conduction mechanism when dealing with poly-Si, and our recent simulation results have shown that thermionic conduction indeed describes the transfer and output characteristics of the proposed device well at room T [14]. This kind of thermally activated process also manifests itself in a way that the mobility and V_{TH} decrease and increase, respectively, as T is reduced [15, 16]. Transfer curves in the SG-1 mode, shown in figure 4(a), are clearly consistent with the above statements. More importantly, an intriguing phenomenon is found in the SG-2 mode. As shown in figure 4(b), V_{TH} depicts an unexpected drastic increase for T below 200 K. Moreover, the SG-2 mode displays a very abrupt turn-on phenomenon when T is lower than 150 K. Specifically, SS in the SG-2 mode is 3.4 mV/dec at 78 K and 4 mV/dec at 100 K. Finally for the DG mode, the contribution from the

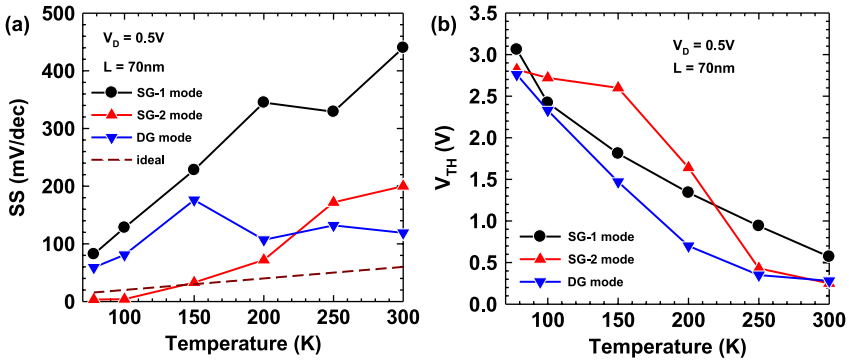

Figure 5. (a) SS and (b) V_{TH} as a function of temperature for the three operating modes extracted from figure 4. SS of the SG-2 mode is 3.4 and 4 mV/dec at 78 K and 100 K, respectively. The ideal value of SS equal to $\ln 10 \times kT/q$ is also included for comparison in (a).

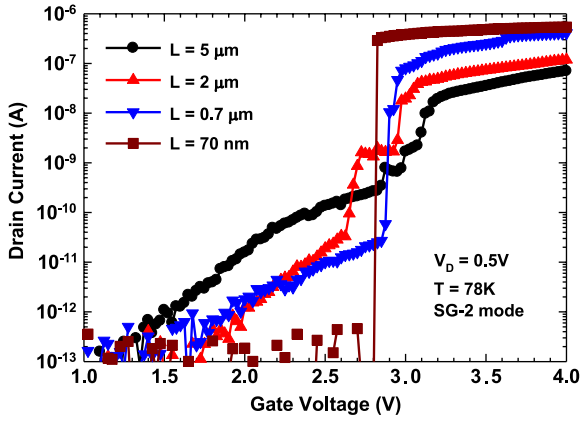

Figure 6. Transfer characteristics at 78 K showing the impact of L on determining the occurrence of steep SS. Contrary to conventional SCE theory, the subthreshold current is reduced as L is shortened.

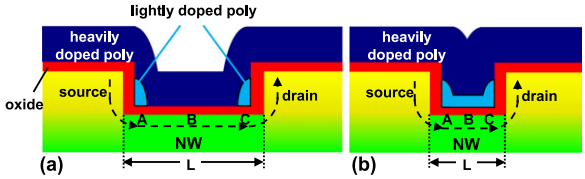

Figure 7. Schematic structures along the length direction showing the second-gate-controlled side of the channel for a device whose L is (a) long (>100 nm) and (b) short (<100 nm). Points A and C correspond to regions of the channel adjacent to S/D controlled by the locally thickened gate and point B to the middle of the channel. Because the thickness of the second gate is 100 nm, the part of the second gate between S/D is thicker in (b) than in (a).

channel controlled by the second gate also causes a sudden increase of I_D at 100 and 78 K. Extracted SS and V_{TH} as a function of T are shown in figures 5(a) and (b), respectively. Note that V_{TH} is defined as the gate voltage when the drain current reaches 10 nA $\times$ W/L, where W is the channel width. The ideal value of SS, which is equal to $\ln 10 \times kT/q$, where k is the Boltzmann constant and q the elemental charge, is also plotted for comparison. From figure 5(a), at 100 and 78 K, SS of the SG-2 mode is already smaller than the ideal value, an indicator that conventional the drift–diffusion principle [17] is no longer the dominant mechanism governing the transport behavior in these cases. On the other hand, as explained in [10], operation in the SG-1 mode tends to exhibit higher V_{TH} than the SG-2 mode due to additional non-gated routes in the SG-1 mode at room temperature; however, the higher V_{TH} in the SG-2 mode over the SG-1 mode within the range of 200–100 K, shown in figure 5(b), implies that some implicit effects in the SG-2 mode may start to become prominent in the low T regime. Transfer curves at 78 K in figure 6 reveal that the occurrence of this abrupt turn-on phenomenon has a strong dependency on L and is in stark contrast to the widely accepted theory concerning SCE; the subthreshold current is seen to decrease with reduced L. Since all of the aforementioned unconventional features are exclusively found in the SG-2 mode, the following discussion will focus on the SG-2 mode unless otherwise specified.

4. Model establishment and discussion

A closer look at the process flow suggests this exclusivity is most likely caused by the different doping methods of the two gates. Namely, doping of the first gate was done by an *in situ* technique that adds phosphine to silane during the LPCVD (low pressure chemical vapor deposition) deposition of poly-Si, where a very uniform and heavy doping concentration throughout the whole first gate electrode is achieved. As for the second gate, dopants were introduced by phosphorus ion implantation at 15 keV with a 5 $\times$ 10^{15} cm^{-2} dose. Taking into account the unique device structure measured in this paper, i.e., one with raised S/D, a schematic device structure along the L direction showing the second-gate-controlled side of the channel is depicted in figure 7(a) for a long L (>100 nm) device and figure 7(b) for a short L (<100 nm) device. For devices with L shorter than the thickness of the second gate (100 nm), the central part of the trench between S/D is filled with thicker poly-Si compared with those with L longer than 100 nm, based on the nature of LPCVD deposition. As a result, for a given implantation energy, the doping concentration is distributed in a manner such that the portion of the second gate farthest from the top surface (i.e., closest to the channel) is only lightly doped, as in figure 7(b), compared with the much higher doping concentration, as shown in figure 7(a).

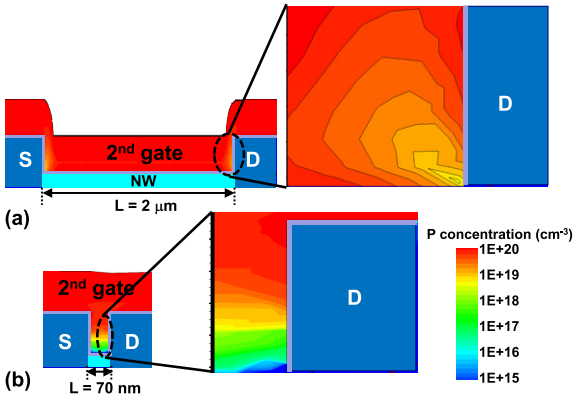

Figure 8. Simulated dopant distribution in an implanted gate corresponding to a device with (a) $L = 2\ \mu$m and (b) $L = 70$ nm. It is observed that the bottom portion of the second gate has a much lower concentration in (b) than in (a).

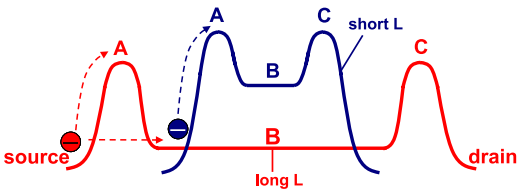

Figure 9. Qualitative band diagrams for devices with long and short L. Points A, B, and C correspond to the regions labeled in figure 7. For a short L device, thermionic emission is the dominant transport mechanism, while both thermionic emission and tunneling should be considered for a long L device.

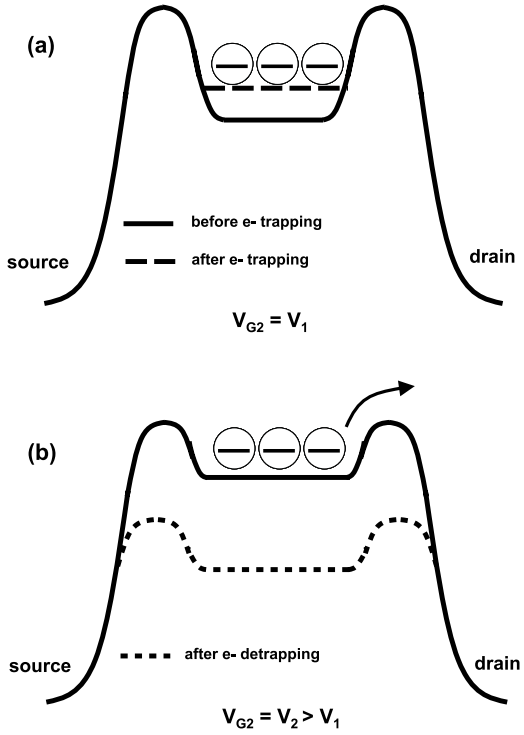

Figure 10. Proposed model for the origin of the steep SS. (a) For a low second gate voltage ($V_{G2} = V_1$), after electron trapping in the channel (dashed line), the potential is raised from its original level (solid line), which deters further injection from the source. (b) For a larger second gate voltage ($V_{G2} = V_2$) which considerably reduces the barrier height at drain side, electrons are detrapped and flow to the drain, leading to a channel potential drop (dotted line) and an abrupt increase in drain current.

In figure 7, points A and C correspond to the regions of the channel adjacent to S/D controlled by the locally thickened gate, and point B to the middle of the channel. Since the second gate is thickest in the regions abutting S/D, the lightly doped area of the second gate spreads to a greater extent in the channel edge than the middle of the channel. The above proposition is clearly confirmed by the simulation results in figure 8.

This non-uniform dopant distribution then leads to variation in gate controllability along the channel, i.e., the gate to channel capacitance is highest in the middle of the channel and decreases toward the channel edge. In this respect, akin to [18], the electrostatic potential along the channel exhibits two humps near S/D, as qualitatively depicted in figure 9. Due to the good step coverage offered by LPCVD, those segments of the second gate of a long L device making contact with the central channel are still heavily doped (figure 7(a)), giving the reason why the potential of the central channel is much lower in a long L device than in a short one, as shown in figure 9. Meanwhile, even though the potential barriers from the two humps are always present for all the characterized L, the barrier height of the humps is smaller in a long L device owing to the stronger gate fringing fields from the more heavily doped gate for a given second gate voltage. With this picture in mind, the behavior of the transfer characteristics with strong L dependency shown in figure 6 becomes reasonable based on the model shown in figure 10. Before further discussion, it should be noted that the tunneling current in poly-Si is often assumed to have a minor contribution because in practical situations the thermionic emission current is always the preponderant component [13]. Nonetheless, tunneling should become appreciable at cryogenic ambient and in the scenario when the tunneling barrier is narrow enough.

For a short L device, the large barrier height of the humps and the high channel potential by virtue of lower second gate doping concentration render tunneling less likely to happen, and thermionic emission then assumes a major role even at low T. In this regard, as T is lowered, the thermionic emission current is gradually reduced, which in turn increases V_{TH}, and, because the barrier heights of the two humps are essentially independent of T, it is rational that below a certain T, when thermal energy is far smaller than the barrier height, the second gate voltage must be high enough ($V_{G2} = V_1$) to reduce the barrier height at point A in figure 9 to a extent that carriers are able to be thermally emitted from the source. Yet, instead of directly transporting to drain, carriers coming from the source to the channel will get trapped therein (in point B of figure 9), raising the channel potential level and preventing further injection from the source, as illustrated in figure 10(a). This scenario will persist until the barrier height present at point C is reduced significantly by a higher applied gate voltage ($V_{G2} = V_2 > V_1$) for the trapped electrons to overcome the barrier with ease and be released to the drain. As a consequence, the channel potential is lowered suddenly and an

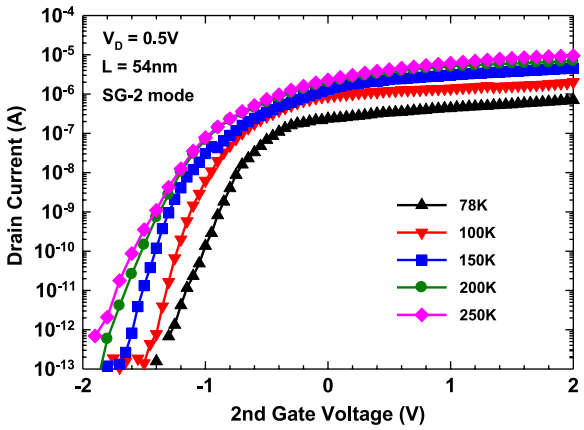

Figure 11. Transfer characteristics as a function of temperature for a device whose first and second gates are both *in situ* doped. Compared with figure 4(b), the steep SS completely vanishes owing to the removal of barriers when very uniform doping concentration throughout the whole second gate electrode is achieved by *in situ* doping.

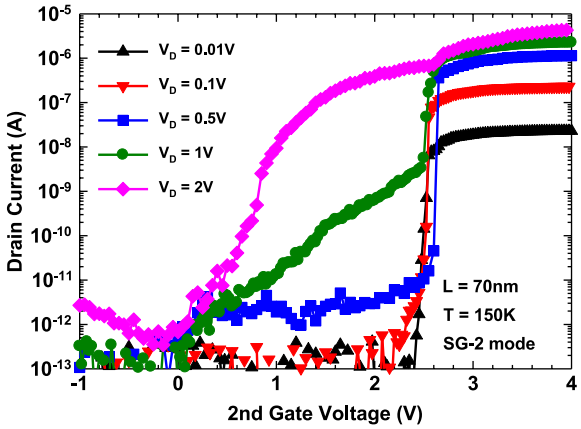

Figure 12. Drain voltage dependent transfer characteristics suggest DIBL could eliminate the occurrence of steep SS, in agreement with the proposed model.

abrupt increase of drain current is observed (figure 10(b)). To further validate our argument, the elimination of the barriers is achieved by *in situ* doping both the first and second gates, and the characteristics in figure 11 evidently corroborate the previous model that the implanted gate is indeed the culprit for the peculiar abrupt switching phenomenon.

With a long L device, the same theory still applies. As mentioned previously with respect to the channel potential profile, the potential difference between the central channel and the source is sufficiently small that tunneling through the barrier is possible besides thermionic emission. The critical T below which thermionic emission is no longer possible without strong gate-induced barrier reduction is supposed to be lower for a long L device thanks to its smaller magnitude of barrier height. It is then expected that thermionic emission and tunneling are both participating conduction mechanisms, explaining the larger subthreshold current for a long L device. Further lowering of the measurement T can help verify this statement by examining the evolution of mobility and V_{TH} with respect to T, based on the fact that the degree of T dependence of thermionic emission and tunneling is drastically different; that is, tunneling should have little temperature dependence as opposed to thermionic emission, which as its name suggests is strongly temperature dependent. Accurate modeling of the shape and magnitude of the barriers is of significance as well in distinguishing between the individual contribution from thermionic emission and tunneling processes, and is still under investigation owing to the complex structure of our proposed device. Nevertheless, the electron-trapping effect can also occur if T is low enough, so that an abrupt switching (e.g., see $L = 0.7\ \mu$m in figure 6), though with a larger SS compared with a device with short L, is attained. Given that the dominant factor determining the occurrence of an abrupt transition lies in the barrier height present at S/D, the impact of the drain-induced barrier lowering (DIBL) is investigated in figure 12. Consistent with the proposed model, the profound influence exerted by DIBL which lessens the barrier height at the source side with increasing drain bias is apparently demonstrated.

5. Conclusion

The origin of abrupt turn-on characteristics observed in an independent double-gate NW transistor at cryogenic ambient is comprehensively studied in this paper. It is found that the occurrence of this behavior is greatly influenced by L, T, and drain bias. A model taking into account the dopant distribution of an implanted gate is proposed to interpret our findings. It suggests that unintentionally formed barriers at the channel edge give rise to carrier-trapping effects until an adequately large gate voltage is applied to lower the magnitude of the barriers for the trapped electrons to flow to the drain. This kind of process-induced barrier is an attractive scheme to build single electron transistors with simple complementary metal–oxide–semiconductor (CMOS) compatible process flow, and with the aid of further surface engineering should help realize steep SS transistors at room temperature.

Acknowledgments

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