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Morphological study on pentacene thin-film transistors: the influence of grain boundary on the electrical properties

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Abstract

We have prepared organic thin-film transistors (OTFTs) featuring pentacene molecules deposited at various substrate temperatures onto either hexamethyldisilazane (HMDS)- or poly(α-methylsyrene) (PαMS)-treated SiO_2 surfaces. As a result, we obtained different grain boundary densities in the conducting channel. Since the surface-modified devices featured similar grain boundary densities in their active layers, but displayed different electrical performances, we suspected that different trap states probably existed at the grain boundaries for the two different kinds of OTFTs. In addition, the surface morphologies of the initial layers featured grain boundaries that were rather blurred for the thin films prepared on the PαMS-treated substrates, whereas shallow boundaries appeared for the pentacene layers on the HMDS-treated surfaces. Therefore, we deduced that the different surface treatment processes resulted in different Schwoebel (step-edge) barriers, and hence, different morphologies. These results suggested that different trap states existed at the grain boundaries of the two types of surface-treated devices, leading to variations in the electrical performance, even though the grain boundary densities were similar.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Organic thin-film transistors (OTFTs) are promising candidates for use in next-generation electronics because they possess many advantageous properties, including low-cost fabrication, mechanical flexibility and light weight. Indeed, they have been incorporated into several potential devices, including smart cards, radio frequency identification tags and flexible displays [1–4]. Recent reports have described OTFT hole mobilities of greater than 1 $cm^2\ V^{-1}\ s^{-1}$, suggesting electrical performance that can be compared with that of amorphous Si [4–7]. Among the various organic semiconductors, pentacene ($C_{14}H_{22}$), a planar aromatic molecule comprising five benzene rings, is one of the most promising candidates for use in *p*-channel devices [8, 9]. Because of its high molecular symmetry, it has a strong tendency to form highly ordered thin films, which would, in principle, increase the hopping rates of charge carriers between the molecules. Furthermore, the device performance of pentacene-based OTFTs is highly correlated with the pentacene layer's morphology, which is significantly affected by many processing parameters, such as the surface properties of the dielectric, the substrate temperature, the deposition rate and the basal pressure of the processing chamber [10–13]. For example, Knipp *et al* reported that an increase in dielectric roughness reduced the charge carrier mobility; meanwhile, a lower growth temperature led to smaller grains and influenced the trap distribution [12]. On the other hand, although many

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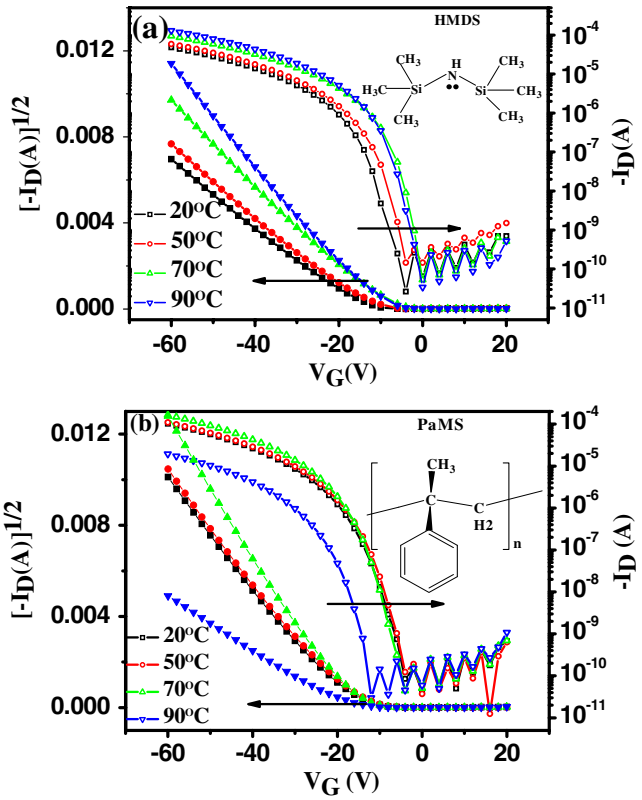

Figure 1. Transfer characteristics of OTFTs featuring pentacene deposited at various substrate temperatures onto (*a*) HMDS- and (*b*) PαMS-treated substrates. The drain voltage (V_D) was maintained at -60 V.

reports have connected the morphological and structural properties of pentacene thin films to the corresponding device performance, thorough investigations still remain rare [14, 15].

In this study, we systematically investigated the influence of grain boundary on the performance of pentacene-based OTFTs. We used two types of modified dielectric surfaces to obtain different dielectric/channel interfaces and then deposited pentacene films onto these surfaces at various substrate temperatures. As a result, we obtained different grain boundary densities in the conducting channel. Since the surface-modified devices featured similar grain boundary densities in their active layers, but displayed different electrical performances, we suspect that different trap states probably existed at the grain boundaries for the two different kinds of OTFTs. Hence, to explain these observations we propose herein a pentacene growth pattern that takes into consideration the Schwoebel barrier effect on the dielectric surfaces.

2. Experimental details

Heavily n-doped Si wafers featuring a 200 nm-thick thermally grown SiO_2 layer were used as substrates. The SiO_2 surface was further modified with either hexamethyldisilazane (HMDS) or poly(α-methylsyrene) (PαMS) (see the insets to figure 1) to improve the device performance. HMDS modification was performed in an oven at 150 °C; no further post-annealing process was employed. On the other hand, PαMS modification was performed through spin-coating from a dilute toluene solution (0.1 wt%); the resulting film was annealed at 80 °C for 1 h [16]. Next, pentacene (60 nm) was thermally evaporated to form the semiconductor layer. Using an infrared heater, the substrate could be heated from room temperature (20 °C) to 90 °C during the deposition processes in the thermal evaporator. The deposition rate was controlled at 0.5 Å s^{-1} using a quartz oscillator. Finally, Au was evaporated, through a shadow mask, to function as the source and drain electrodes. The channel width (W) and length (L) were 2000 μm and 90 μm, respectively. Electrical characterization, at room temperature in an atmosphere of air, was performed using a semiconductor parameter analyzer (Keithley 4200). The surface morphology was measured using a Digital Instruments Dimension 3100 atomic force microscope. The x-ray diffraction (XRD) patterns were obtained using a thin film x-ray diffractometer (M18XHF-SRA, MAC Science) and Cu Kα ($\lambda = 1.5406$ Å) radiation.

3. Results and discussion

3.1. Electrical properties

Figure 1 displays the representative transfer characteristics of the OTFTs deposited on the HMDS- and PαMS-modified SiO_2 surfaces at various substrate temperatures. The device mobility (μ) was extracted from the conventional field-effect transistor model in the saturation regime [17]:

$$I_D = \frac{WC_i\mu}{2L}(V_G - V_T)^2, \qquad (1)$$

where I_D is the source–drain current, C_i is the capacitance per unit area of the dielectric, V_G is the gate voltage and V_T is the threshold voltage. Figure 2 summarizes the calculated mobilities. For the HMDS-treated devices, the mobility increased from 0.21 to 0.33 $cm^2\,V^{-1}\,s^{-1}$ upon increasing the substrate temperature from 20 to 70 °C. The mobilities of the PαMS-treated devices increased similarly, reaching an even higher value of 0.72 $cm^2\,V^{-1}\,s^{-1}$ at 70 °C, but decreased dramatically to 0.10 $cm^2\,V^{-1}\,s^{-1}$ when the substrate temperature was 90 °C. Meanwhile, the V_T shift proceeded pronouncedly in the negative direction (figure 1(*b*)). We suspected that the morphology of the semiconducting layer changed significantly at such a high temperature.

3.2. Morphological study on the pentacene thin films

To study the effect of substrate temperature during the deposition of pentacene, we used atomic force microscopy (AFM) to observe the resulting surface morphologies. Figures 3 and 4 display AFM images of the 60 nm-thick pentacene layers deposited on the HMDS- and PαMS-treated substrates, respectively. Note that no stable films were obtained when the substrate temperature was above 110 °C, presumably because of a higher rate of pentacene desorption relative to absorption at that temperature. In general, the grain size increased upon increasing the deposition temperature for both kinds of devices. With larger amounts of thermal energy, the pentacene molecules were able to diffuse longer

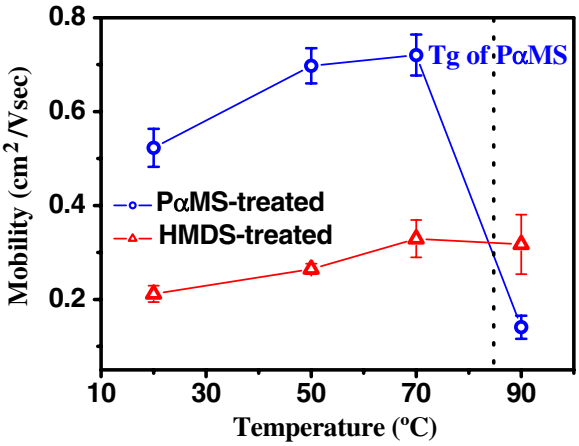

Figure 2. Variation in the mobility calculated from the I–V characteristics in figure 1 as a function of the substrate temperature for the pentacene-based OTFT devices prepared on the HMDS- and PαMS-modified SiO_2 substrates.

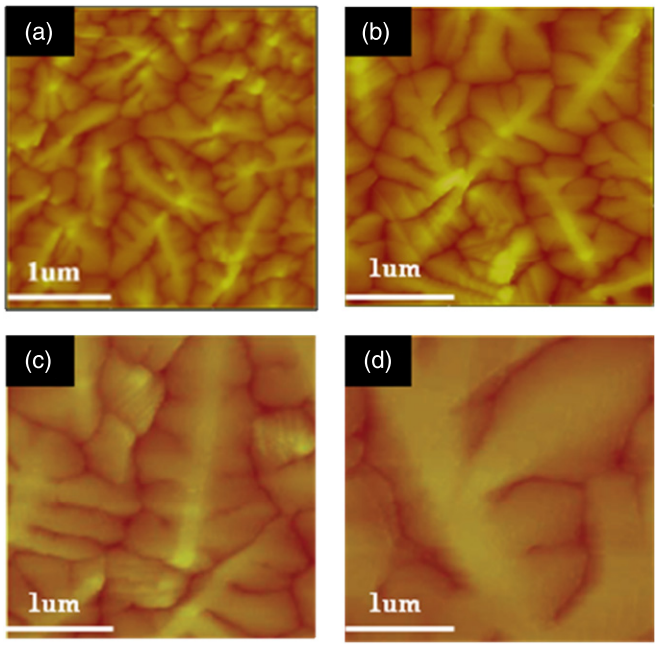

Figure 3. AFM images of 60 nm-thick pentacene films deposited at various deposition temperatures at a fixed flux rate (0.5 Å s^{-1}) onto HMDS-treated SiO_2 substrates; image size: 3 × 3 μm^2. The substrate temperatures were (*a*) 20, (*b*) 50, (*c*) 70 and (*d*) 90 °C.

on the dielectric surface, thereby having a higher probability of finding energetically preferred sites for nucleation and facilitating grain growth. For the PαMS-treated samples, although the grain size continued to grow upon increasing the temperature to 70 °C, it decreased when the substrate temperature reached 90 °C; interestingly, we observed poor connectivity between the grains (figure 4(*d*)). Because the glass transition temperature (T_g) of PαMS is ca 85 °C, the polymer chains became rubbery when the substrate temperature was greater than T_g. The higher level of thermal motion led to a shorter diffusion length of pentacene molecules, and therefore, diminished grain sizes. Accordingly, we observed a dramatic change in morphology when the pentacene thin film was deposited onto the PαMS-modified samples at a

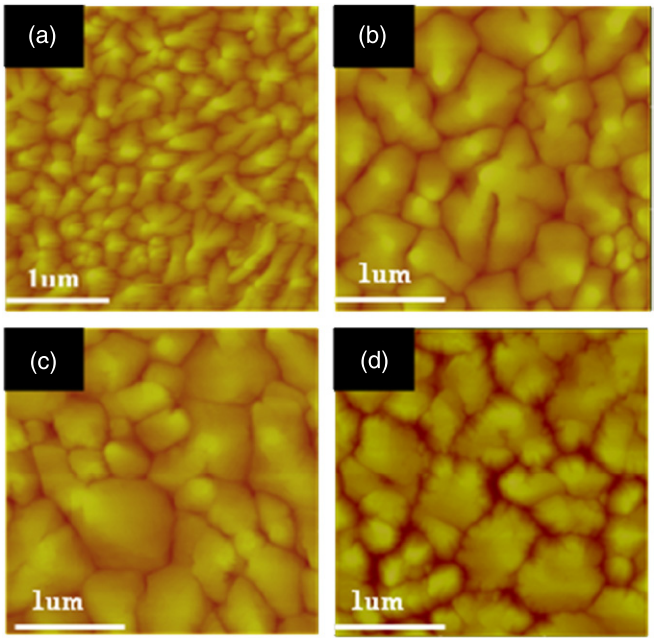

Figure 4. AFM images of 60 nm-thick pentacene films deposited at various deposition temperatures at a fixed flux rate (0.5 Å s^{-1}) onto PαMS-treated SiO_2 substrates; image size: 3 × 3 μm^2. The substrate temperatures were (*a*) 17, (*b*) 50, (*c*) 70 and (*d*) 90 °C.

substrate temperature of 90 °C.

Next, we used XRD to examine the crystalline phase of the pentacene thin films. For the thin film deposited on the HMDS-treated substrate at 20 °C (figure 5(*a*)), we observed one set of diffraction peaks, having a d spacing of 15.4 Å. This set of peaks, indexed as (0 0 l') reflections, has been identified as a thin film phase of pentacene [18]. For higher substrate temperatures, another set of (0 0 l) peaks appeared; this second phase, having a d spacing of 14.4 Å, was consistent with the bulk phase of pentacene [18]. A similar phase transition has been reported for pentacene films deposited on bare SiO_2 surfaces [18]. Previous reports have suggested that this change in phase is related to the relaxation of the initially strained thin film [19]. In contrast, the thin film phase of the pentacene crystals on the PαMS-treated substrate remained almost unchanged after increasing the substrate temperature (figure 5(*b*)). Thus, treatment with PαMS suppressed the phase transition. We inferred that the softer texture and flexibility of the PαMS polymer could aid in releasing the strain, thereby stabilizing the thin film phase. On the other hand, because the bulk phase was thermodynamically stable, the greater mobility of pentacene at higher substrate temperatures facilitated the molecules to reposition themselves to the lowest energy configuration [18]. Hence, some bulk phase was observed for the films deposited on the PαMS-treated substrates at higher temperatures.

3.3. Effect of grain boundaries on the device performance

The effective mobility (μ_{eff}) in polycrystalline TFTs can be determined using the equation [20]

$$\mu_{eff}^{-1} = \mu_0^{-1} + \mu_{GB}^{-1}, \qquad (2)$$

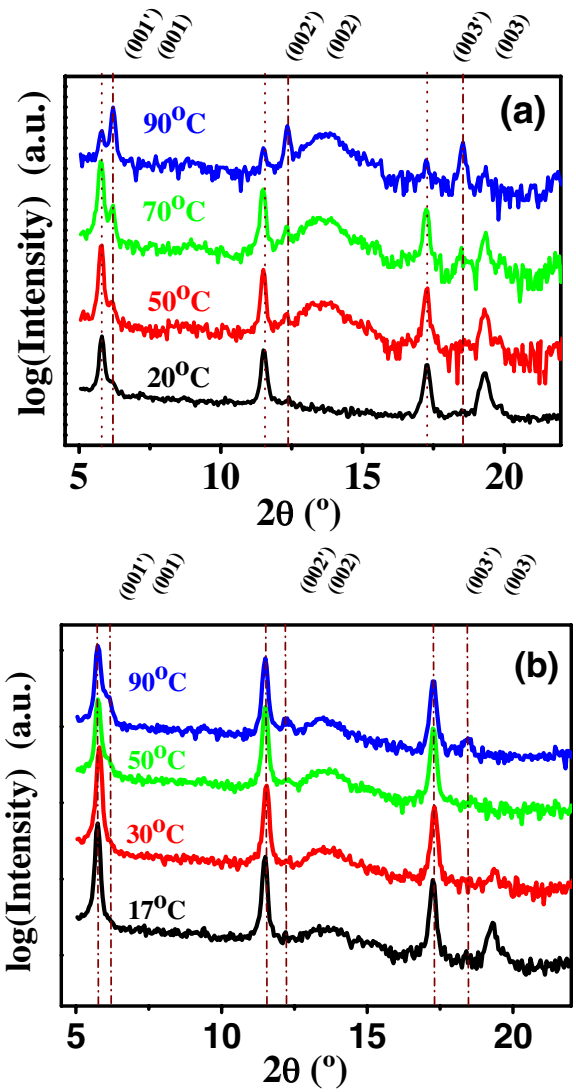

Figure 5. XRD spectra of 60 nm-thick pentacene films deposited at various deposition temperatures onto the (*a*) HMDS- and (*b*) PαMS-treated substrates. The peak at a value of 2θ of ca 14° represents the diffraction of SiO_2.

where μ_0 is the bulk mobility and μ_{GB} is the grain boundary mobility. Thus, we know that the device mobility is related to the bulk and grain boundary status. Furthermore, if μ_{GB} is much less than μ_0, the effective mobility will be close to μ_{GB}. In other words, the charge transport is limited mainly by the grain boundaries. Assuming that the charge transport at grain boundaries is governed by thermionic emission, μ_{GB} can be further expressed as

$$\mu_{GB} = \mu_{GB0} \exp\left(-\frac{E_B}{kT}\right), \tag{3}$$

where E_B is the barrier height and μ_{GB0} is the trap-free mobility in the grain boundary. To see the effect of grain boundary, we developed a program (appendix) to estimate the 'length' of the grain boundaries from the AFM images in figures 3 and 4 and, thereby, to calculate the density of the grain boundary per unit area. From the data, we found, surprisingly, that the mobility was generally inversely proportional to the grain boundary

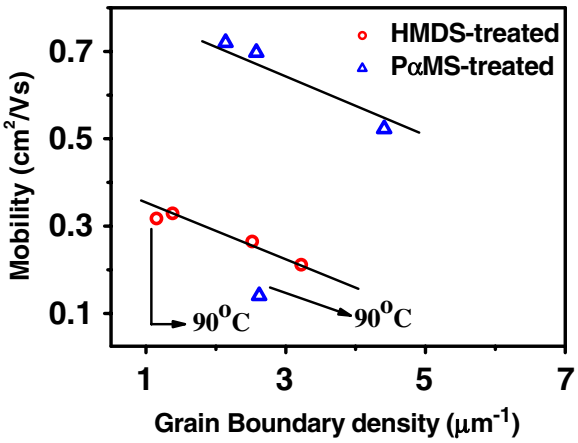

Figure 6. Calculated mobility plotted with respect to the grain boundary density for devices prepared on the two types of surface-treated dielectric surfaces. The grain boundary density was calculated from the AFM images of the 60 nm-thick films in figures 3 and 4.

density (figure 6). This result suggests that the effect of grain boundary is the dominant factor in determining the degree of charge transport in the devices. In addition, the mobilities of the PαMS-treated devices were always greater than those of the HMDS-treated ones, even though the holes were being transported through the same number of grain boundaries. We inferred that the difference was due to the presence of different trapping states at the grain boundaries. Notably, we observed two exceptions to the devices' performances: (i) for the HMDS-treated OTFT device prepared with pentacene deposition at 90 °C, when serious phase transition occurred, and (ii) for the PαMS-treated device prepared with pentacene deposition at 90 °C, when the polymer turned rubbery. In these two cases, other factors became important; the derivation from the general trend in figure 6 was, therefore, expected.

3.4. Analysis of the origins of the different traps states at the grain boundaries

To understand the origins of the different trap states at the grain boundaries of the two different surface-treated devices, figure 7 displays the morphologies of the corresponding 8 nm-thick pentacene films (ca five monolayers (MLs)) deposited at various temperatures. For the thin films deposited on the HMDS-treated substrates, we clearly observe grain boundaries within the first few MLs. On the other hand, for the pentacene layers deposited on the PαMS-treated substrates, many of the grain boundaries were too blurry to recognize, in particular for the thin film prepared at a substrate temperature of 70 °C. We suspected that the growth of the pentacene layers on the HMDS-treated substrates was similar to the 'mound growth mode', whereas that on the PαMS-treated substrates favoured the layer-by-layer mode [21, 22] (figure 8). Furthermore, the difference in the growth modes probably resulted from the presence of the Schwoebel barrier effect (see below) [21].

The growth mechanism of pentacene on various substrates has been investigated extensively. In addition to diffusion-limited aggregation in the lateral direction, some previous

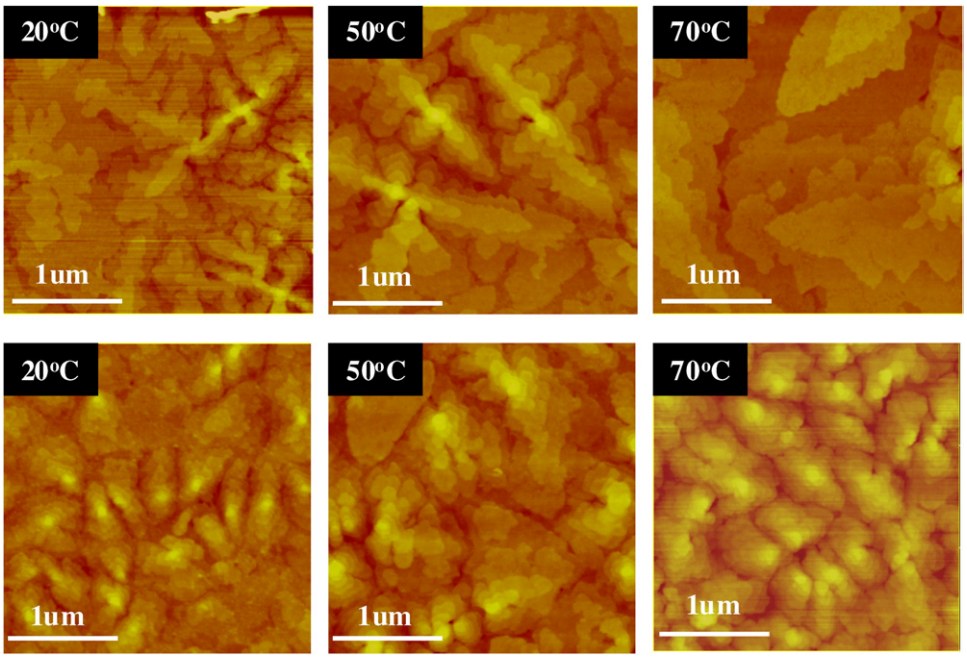

Figure 7. AFM images of 8 nm-thick pentacene films deposited at various temperatures onto HMDS- (top panel) and PαMS-treated (bottom panel) SiO_2 substrates; image size: $3 \times 3\ \mu m^2$.

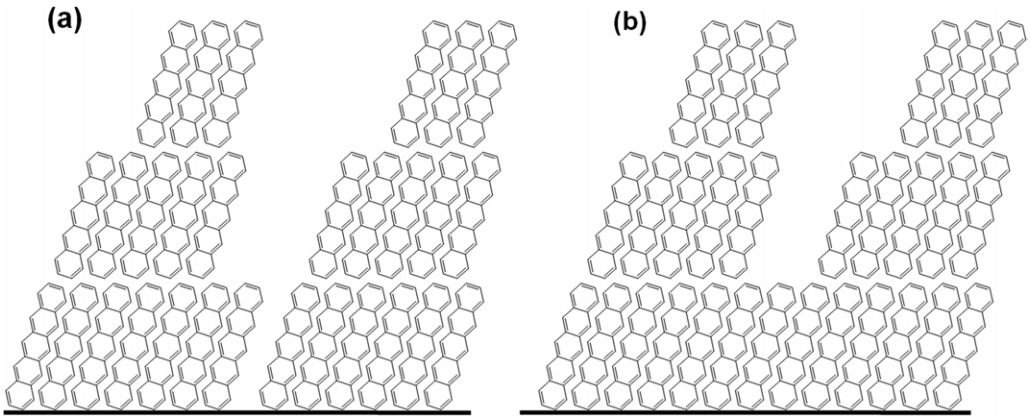

Figure 8. Schematic representation of the structures of pentacene films on the (*a*) HMDS- and (*b*) PαMS-treated substrates. The higher Schwoebel barriers on the HMDS-treated surfaces resulted in deeper crevices.

reports have also indicated that the Schwoebel barrier disrupts the desired epitaxial growth of pentacene molecules [21]. The presence of such a step-edge barrier on a terrace will prevent the landing molecules from hopping down the edge. Hence, they prefer to remain on the islands, thereby leading to a three-dimensional (3D) growth mode. In short, the presence of such a barrier leads to a fractal shape. That is, the pentacene layers approach a dendrite-like morphology (figure 7). In contrast, in the absence of such a Schwoebel barrier, the molecules will jump down to a lower layer, resulting in a two-dimensional (2D) growth mode [21, 22].

Since the Schwoebel barrier effect can be strengthened or alleviated after surface treatment [21], we expected different phenomena to occur for the devices prepared on our two different substrates. Since a potential energy (Schwoebel) barrier existed in the HMDS-treated devices, the apparent uphill flux of the pentacene molecules led to fast upward growth, causing the deep crevices that are apparent in figure 8(*a*). On the other hand, for the PαMS-treated devices, either the Schwoebel barrier was relatively small or thermal energy could easily overcome the edge barrier. Therefore, we observed layer-by-layer growth of the pentacene molecules and the grain boundaries became relatively blurred (figure 8(*b*)). From the schematic plot of the structures of the pentacene films, we deduced that the barrier height (E_B) for the grain boundaries on the HMDS-treated surfaces was higher, because charge transport is believed to occur only in the first few layers of pentacene near the dielectric/semiconductor interfaces. In short, the two different growth modes led to grain boundaries possessing various barrier heights. As a result, the PαMS-modified devices exhibited higher mobilities, even though the grain boundary densities, which we measured from the surfaces of 60 nm-thick pentacene films, were the same as those of the HMDS-treated devices (figure 6).

4. Conclusion

We have prepared pentacene thin-film transistors on either HMDS- or PαMS-treated SiO_2 surfaces at different substrate temperatures. AFM analysis of the surface morphologies revealed that the grain size increased upon increasing the substrate temperature. Electrical analysis indicated that the device performance was highly related to the grain boundary density. In addition, using AFM to investigate the surface morphologies of the corresponding initial layers (ca 5 MLs), we found that the grain boundaries were rather blurry for the thin films deposited on the PαMS-treated substrates, whereas shallow boundaries existed for the pentacene layers deposited on the HMDS-treated surfaces. We deduced that the different surface treatment processes resulted in different Schwoebel (step-edge) barriers, and hence, different morphologies. As a result, different trap states existed at the grain boundaries for the two different surface-treated devices, leading to dissimilar hole mobilities even though the grain boundary densities were similar. Our results suggest that surface treatment has a pronounced effect on the barrier heights of grain boundaries. We conclude that grain boundary is the dominant factor in determining the electrical performance for OTFT devices incorporating pentacene.

Acknowledgments

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Appendix

Matlab Program to define the grain boundary density from the N*N matrix of AFM images:

```
function GB_count (AFM file)
rgb=imread (AFM file);
rgb=imresize(rgb, [512 512]);
r=rgb(:,:,1);
gray2log=(r>139);
figure; imshow(gray2log);
[u,v]=meshgrid(-255:256, -255:256);      % to define a space for Fourier transform
highpass=1-1./(1+(sqrt(u.^2+v.^2)/60).^4);   % highpass filter
F=fftshift(fft2(double(gray2log)));
y=real(ifft2(fftshift(highpass.*F)));
Y=(y>0.1);                               % to show the pattern obviously
image_i = Y;
dimension = size(image_i);
target = 0;                              % to count how many white pixels is
for i=1 : dimension(1,1)
    for j = 1 : dimension(1,2)
        if image_i(i,j) == 1
                    target = target + 1;
        end;
  end;
end;
ratio = target/(dimension(1,1)*4)
```

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