Formation of iridium nanocrystals with highly thermal stability for the applications of nonvolatile memory device with excellent trapping ability

Terry Tai-Jui Wang, Chang-Lung Chu, Ing-Jar Hsieh, and Wen-Shou Tseng

---

Formation of iridium nanocrystals with highly thermal stability for the applications of nonvolatile memory device with excellent trapping ability

Terry Tai-Jui Wang,[1] Chang-Lung Chu,[2] Ing-Jar Hsieh,[3] and Wen-Shou Tseng[4,a]

[1]Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan
[2]Institute of Nanotechnology, National Chiao Tung University, Hsinchu 30050, Taiwan
[3]Department of Electric Engineering, Chung Hua University, Hsinchu 30012, Taiwan
[4]Center for Measurement Standards, Industrial Technology Research Institute (ITRI), Hsinchu 30011, Taiwan

This paper presents the formation of iridium nanocrystals (Ir-NCs) embedded in SiO_2 matrix and it can be used for potential applications of nonvolatile memory devices. The NC formation is investigated by varying Ir film thickness; and the thermal agglomeration is also studied by applying various annealing temperatures and process time. The results of systematic characterization including capacitance-voltage, transmission electron microscopy, and x-ray photoelectron spectroscopy show that the high work-function (5.27 eV) metallic-NCs have a highly thermal stability (up to 900 °C) and the resulted $Al/SiO_2/Ir$-NCs$/SiO_2/Si/Al$ stack can have a good retention ability and significant hysteresis window of 17.4 V. © 2010 American Institute of Physics. [doi:10.1063/1.3498049]

Recently, owing to their discrete storage characteristics for largely immunizing the local oxide defects and aggressively reducing the tunneling oxide layer, nanocrystals (NCs) are regarded as important materials in nonvolatile memory (NVM) applications and the replacement for conventional floating gate memory devices.[1,2] Metallic-NC memory devices can have higher programming/erasing (P/E) efficiency and lower operating voltage than conventional devices so as to economize device power consumption. Besides, these devices also have larger charge capacity and wider range work function modulation.[3–6] However, their inherency of low-thermal stability is unfavorable for most complementary metal oxide semiconductor (MOS) fabrication processes which often require high temperature annealing procedure. Ni and W are considered as the popular materials due to their high work functions of 5.15 and 4.55 eV.[7] Unfortunately, Ni is easily oxidized at room temperature (RT) and very unstable during the annealing process.[8] W is shown to be with higher melting temperature and better thermal stability while its work function is insufficient to challenge device scale limit.[9,10] When metallic-NCs are used to fabricate NVM devices, it is expected to endure the source/drain activation process conducted at about 900 °C without causing a significant self-oxidation and to be easily etched by a scalable production process. In this paper, with natures of high work-function (5.27 eV), high etchability, and thermal stability,[11–14] Iridium-NCs are used as the trapping center to fabricate metal insulator semiconductor (MIS) capacitors for NVM application.

A 6 nm SiO_2 tunneling oxide layer was grown on p-type silicon substrate by a thermal oxidation process after a pre-cleaning process. Subsequently, it was coated with an Ir film with thickness ranging from 4.5 to 9 nm by a sputter, and followed by a rapid thermal annealing process at 900 °C for 60 s in N_2 atmosphere. A 20 nm SiO_2 blocking layer was then deposited by plasma enhanced chemical vapor deposition (PECVD) and followed by a thermal annealing process at 400 °C for 30 min in O_2 atmosphere so as to improve the quality of the blocking oxide layer. Al electrodes with 300 nm thickness were finally deposited on the top and bottom sides of the stack by a thermal coater to form $Al/SiO_2/Ir$-NCs$/SiO_2/p$-Si substrate$/Al$ stack while the top electrode was patterned and etched by using a $H_3PO_4/HNO_3/CH_3COOH/H_2O$ solution with a volume ratio of 50/2/10/9.

After the Ir films are annealed at 900 °C for 60 s, as revealed in scanning electron microscope (SEM) images in Figs. 1(a)–1(d), the films are transformed into very uniform and densely dispersed nanoparticles on the SiO_2 layer. Both the particle size and dot number density of the Ir-NCs increase as the Ir film thickness increases from 4.5 to 9.0 nm.
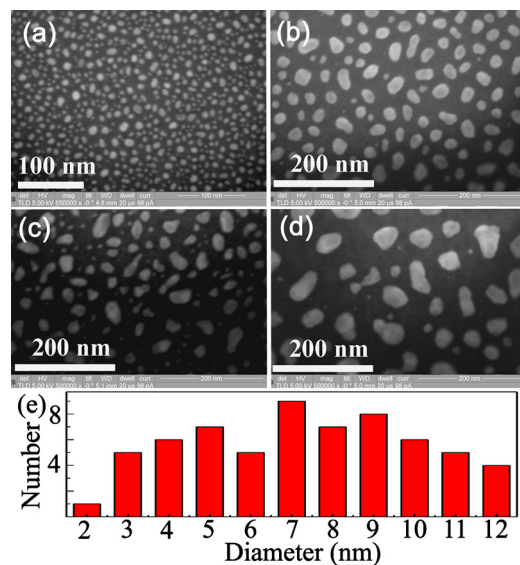

FIG. 1. (Color online) The SEM images of the Ir-NCs derived from various Ir film thicknesses of (a) 4.5, (b) 6.0, (c) 7.5, and (d) 9 nm after a rapid thermal annealing process at 900 °C for 60 s in N_2 atmosphere. (e) The corresponding size distribution of Ir-NCs of (a).

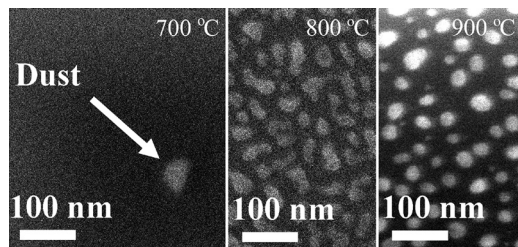a)Electronic mail: marine.mse92g@g2.nctu.edu.tw.

FIG. 2. The SEM images of the Ir film under various annealing temperatures of 700, 800, and 900 °C when the thickness is 12 nm.

In addition, as compared to the Ir-films with other thicknesses in Figs. 1(b)–1(d), after the annealing process, the resulting nanoparticles in Fig. 1(a) are found to be more uniform and dense with dot density of approximately 6 $\times 10^{11}$ cm^{-2} when the thickness is 4.5 nm. This is likely because the cluster effect may become dominant so that larger particles are easily formed as the film thickness increases.[15] In Fig. 1(e), it is shown that the mean diameter of the size distribution is approximately 8 nm while the initial thickness is 4.5 nm. On the other hand, as shown in Fig. 2, when annealing temperatures are lower than 900 °C, the resulted Ir-NCs are found to be with asymmetrical shape and less size uniformity. This agrees with the fact that annealing temperature and initial thickness are essential to determine NC size.[5]

The transmission electron microscope (TEM) image in Fig. 3 reveals that the dark and circular like particles of Ir-NCs are embedded in the silicon dioxide matrix with different sizes ranging from 5 to 9 nm but, as compared with the Ir-NCs in Fig. 1(a), it is more difficult to accurately estimate the size distribution of Ir-NCs. In order to demonstrate conveniently, the structure schematic corresponding to the resulted $SiO_2/Ir\text{-}NCs/SiO_2/Si$ stack is revealed in the inset.

The results of the x-ray photoelectron spectroscopy (XPS) survey spectra in Fig. 4(a) depict that, after the Ir film is annealed at 900 °C for 60 s, the Si $2p$ peak appears. This suggests that the Ir film can cover the tunneling oxide layer completely prior to the annealing process. It is noted that the XPS results have been calibrated by using C $1s$ peak at 284.6 eV. In Fig. 4(b), no significant shifts have been observed upon the Ir $4f_{7/2}$ and $4f_{5/2}$ peak positions before and after the annealing process at 800 and 900 °C, showing that no oxidation of Ir-NCs occurs in this case.

Because the electric performance is essential for analyzing the feasibility of using Ir-NC to fabricate an ideal floating gate memory device, capacitance voltage (CV) tests are conducted to measure the device. The comparison results of the CV curves of the MOS capacitor stacks with and without
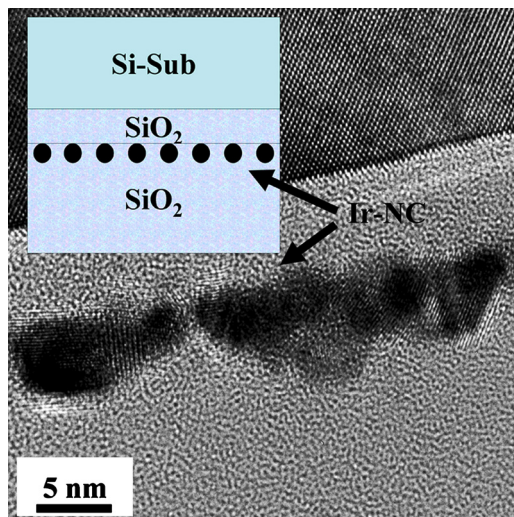

FIG. 3. (Color online) The TEM image of the $Al/SiO_2/Ir\text{-}NCs/SiO_2/Sub$ stack. The structure schematic corresponding to the resulted stack is revealed in the inset.

Ir-NCs are shown in Fig. 5(a), where the gate voltage is swept from −15 to +13 V with step of 0.2 V. Meanwhile, the stacks with Ir-NCs are shown to be with flat-band voltage shift (ΔV_{FB}) of approximately 17.4 V. According to the curve, the carrier trap density is estimated to be approximately $1.17 \times 10^{13}/cm^2$ by formula: $N = (C/A^*q)\Delta V_{FB}$, where C and q are 1.08×10^{-11} F and 1.6×10^{-19} C, respectively, ΔV_{FB} is about 17.4 V, and A is the gate pad area of 10^4 μm^2. Estimated by combining the results and the Ir-NCs density in Fig. 1(a), each Ir-NC could store about 20 electrons or equivalent holes. In addition, the large hysteresis window should be caused by the heterointerface of defect states between the Ir-NCs and SiO_2 layer.

Note that smaller dot size and higher dot density may increase the trapping density of the device and give rise to a larger memory which can be observed in the CV curves. Meanwhile, predicted by Hou *et al.*,[16] the increase in NC size and decrease in dot spacing could result in charging efficiency decay. Based on above, the CV measurement is conducted with applying the highest dot density, determined by the resulted process conditions of initial film thickness and temperature as mentioned. However, providing the curves of various specimen with related information of the Ir NC size and density, and process conditions of initial film thickness as well as annealing temperature is very important to determine the optimal conditions for fabricating a commercial device in future study.
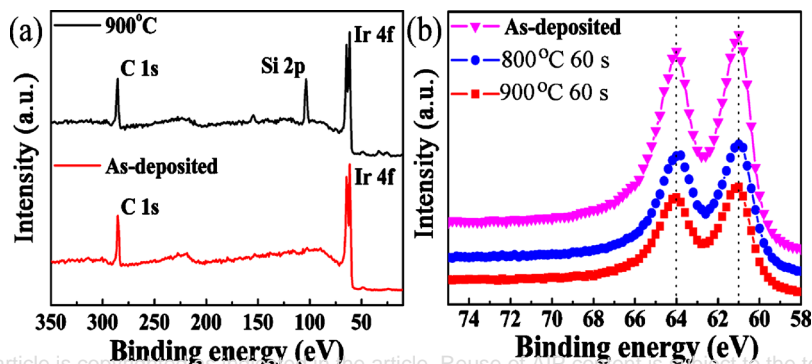

FIG. 4. (Color online) (a) Comparison of XPS survey spectra of the Ir film before and after 900 °C annealing process for 60 s. (b) The XPS Ir $4f$ spectra of the Ir-NCs on SiO_2 layer before and after 800 and 900 °C annealing processes.
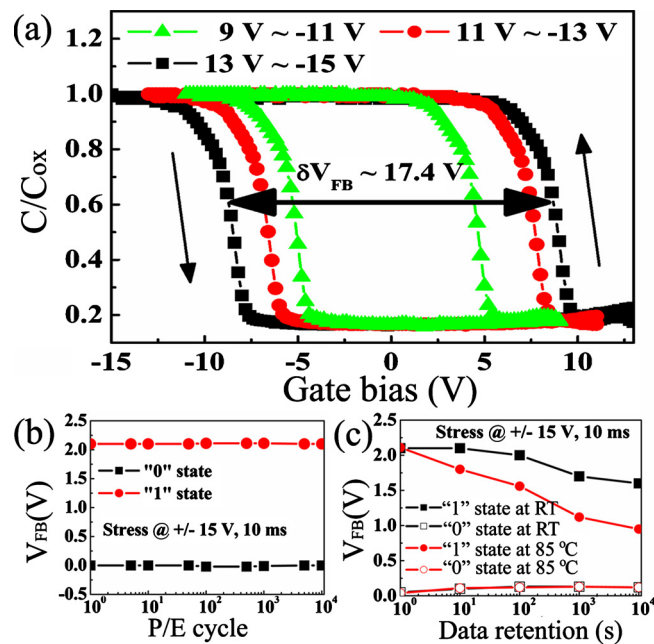
FIG. 5. (Color online) (a) CV curves of Al/SiO$_2$/Ir-NCs/SiO$_2$/Sub/Al device stack at different sweeping voltages. (b) Device durability curves of the device stack with +/−15 V and 10 ms stressing condition. (c) The data retention characteristic of the device stack with Ir-NCs obtained by electron charging (+15 V, 10 ms) and discharging (−15 V, 10 ms) at RT and 85 °C.

It is also predicted by previous study that a device with a denser dot density, i.e., smaller dot spacing, may have a larger memory window and longer service life but this device may also have the issue of a steeper degradation slope.[16] Therefore, a mean diameter of approximately 8 nm and the optimal dot density of approximately 6×10^{11} cm^{-2} are used as the design parameters for the metal NC memory.[16]

In programming operation of the device, the tunneling current is mainly originated from Si-substrate. Some electrons will be trapped by the energy well formed by Ir-NCs. In erasing operation, the trapped electrons tunnel back to Si-substrate through the tunneling oxide layer. Thus, the Ir-NCs embedded stack can be used to fabricate a NVM device through manipulating the charging and discharging effects in the stack while the flat-band voltage shift is large enough for defining "1" and "0" states.

The P/E cycling characteristics of the memory capacitor stack under the pulse condition of gate voltage at +/−15 V for 10 ms is depicted in Fig. 5(b). It indicates that the flat-band voltages under P/E conditions show almost no significant drifts up to 10^4 stressing cycles, signifying good device durability. On the other hand, because the dot size has a significant effect on the surface roughness of the oxide layer, when a 20 nm SiO$_2$ film is deposited by PECVD, applying a large dot size to fabricate device may yield the blocking oxide layer with a high surface roughness and result in poor endurance of the device due to a strong electric field in the surround of dots.[17]

In Fig. 5(c), the charge loss characteristics of the presented MIS capacitor stack at two different temperatures are measured by a capacitance time method with applying +/

−15 V as prestressing for 10 ms.[18] It is shown that, when the retention time is 10^4 s, the difference of flat-band voltage is 1.41 V at RT and the voltage is only 0.82 V at 85 °C. It is also shown in this figure that the V$_{FB}$ of "1" state decreases as the retention time increases. This is likely because the 10^4 cycle prestressing test may introduce some positive charge traps in the silicon dioxide, the electrons trapped in the Ir-NCs are easily tunneled out by the "trap assistant tunneling mechanism," and the tunneling effect can be further activated as the measurement temperature increases.[19–21] Moreover, in contrast to "1" state, the decreases of "0" state is shown to be marginal as the retention time increases. This could be due to free of over-erase phenomenon when the erasing conditions of this test are applied in this case.

In summary, high density Ir-NCs are formed by a thermal annealing process at 900 °C with XPS results showing that the crystals are thermally stable. Results also show that the resulted Al/SiO$_2$/Ir-NCs/SiO$_2$/Si/Al stack can be with excellent device durability, good retention ability, and a significant hysteresis window of 17.4 V under a sweep voltage ranging from −15 to +13 V. Theses demonstrate that the Ir-NCs in SiO$_2$ matrix can be considered as a highly potential trapping stack for NVM device application.

[1]S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan, Appl. Phys. Lett. **68**, 1377 (1996).
[2]C. Y. Lu, T. C. Lu, and R. Liu, *Proceedings of the 13th International Physical and Failure Analysis of Integrated Circuits Symposium*, Singapore, 2006 (IEEE, New York, 2006), pp. 18–23.
[3]C. Lee, A. Gorur-Seetharam, and E. C. Kan, Tech. Dig. - Int. Electron Devices Meet. **2003**, 557.
[4]B. Li, J. Ren, and J. Liu, Appl. Phys. Lett. **96**, 172104 (2010).
[5]J. J. Lee, Y. Harada, J. W. Pyun, and D. L. Kwong, Appl. Phys. Lett. **86**, 103505 (2005).
[6]S. Choi, S. S. Kim, M. Chang, and H. Hwang, Appl. Phys. Lett. **86**, 123110 (2005).
[7]H. B. Michaelson, J. Appl. Phys. **48**, 4729 (1977).
[8]J. Dufourcq, P. Mur, M. J. Gordon, S. Minoret, R. Coppard, and T. Baron, Mater. Sci. Eng., C **27**, 1496 (2007).
[9]C. Y. Lu, K. Y. Hsieh, and R. Liu, Microelectron. Eng. **86**, 283 (2009).
[10]Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, IEEE Trans. Electron Devices **49**, 1614 (2002).
[11]C. W. Chung, H. I. Kim, and Y. S. Song, J. Electrochem. Soc. **150**, G297 (2003).
[12]M. Youm, H. S. Sim, H. Jeon, S. I. Kim, and Y. T. Kim, Jpn. J. Appl. Phys., Part 1 **42**, 5010 (2003).
[13]M. Hasan, H. Park, J. M. Lee, and H. Hwang, Electrochem. Solid-State Lett. **11**, H124 (2008).
[14]B. F. Hung, C. H. Wu, A. Chin, S. J. Wang, F. Y. Yen, Y. T. Hou, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang, IEEE Trans. Electron Devices **54**, 257 (2007).
[15]W. S. Tseng, W. H. Wang, T. H. Hong, and C. T. Kuo, Jpn. J. Appl. Phys. **48**, 085502 (2009).
[16]T. H. Hou, C. Lee, V. Narayanan, U. Ganguly, and E. C. Kan, IEEE Trans. Electron Devices **53**, 3095 (2006).
[17]W. R. Chen, T. C. Chang, J. L. Yeh, S. M. Sze, and C. Y. Chang, Appl. Phys. Lett. **92**, 152114 (2008).
[18]H. R. Lee, S. Choi, K. Cho, and S. Kim, Thin Solid Films **516**, 412 (2007).
[19]A. Teramoto, K. Kobayashi, Y. Matsui, M. Hirayama, and A. Yasuka, IEEE Proc. Int. Reliab. Phys. Symp. **1996**, 113.
[20]T. H. Wang, N. K. Zous, and C. C. Yeh, IEEE Trans. Electron Device **49**, 1910 (2002).
[21]T. Wang, H. C. Ma, C. H. Li, Y. H. Lin, C. H. Chien, and T. F. Lei, IEEE Electron Device Lett. **29**, 109 (2008).