New Transient Detection Circuit for On-Chip Protection Design Against System-Level Electrical-Transient Disturbance

Ming-Dou Ker, *Fellow, IEEE*, and Cheng-Cheng Yen, *Member, IEEE*

***Abstract*—A new transient detection circuit for on-chip protection design against system-level electrical-transient disturbance is proposed in this paper. The circuit function to detect positive or negative electrical transients under system-level electrostatic-discharge (ESD) and electrical-fast-transient (EFT) testing conditions has been investigated by HSPICE simulation and verified in silicon chip. The experimental results in a 0.18-μm complementary-metal–oxide–semiconductor (CMOS) process have confirmed that the new proposed on-chip transient detection circuit can successfully memorize the occurrence of system-level electrical-transient disturbance events. The output of the proposed on-chip transient detection circuit can be used as a firmware index to execute the system recovery procedure. With hardware/firmware codesign, the transient disturbance immunity of microelectronic products equipped with CMOS integrated circuits under system-level ESD or EFT tests can be significantly improved.**

***Index Terms*—Electrical-fast-transient (EFT) test, electromagnetic compatibility, electrostatic discharge (ESD), system-level ESD test, transient detection circuit.**

I. Introduction

Complementary-metal-oxide-semiconductor (CMOS) integrated circuits (ICs) have been widely used in industrial electronic products, such as motor drives, robot system, uninterruptible power supply, and global positioning system, etc. [1]–[5]. With increasing electromagnetic emission sources in a microelectronic system, such as radio-frequency transmitters, high-speed digital devices, mobile phones, etc., the environment where these CMOS ICs are located has more system-level electrical-transient disturbance than before. Therefore, electrical-transient disturbance has become a primary reliability issue in industrial electronic products equipped with CMOS ICs [6]–[9]. With more circuit blocks being integrated into a chip, such as mixed signal, mixed voltage, system on chip, etc., CMOS devices will suffer more electrical transients coming from the interior of CMOS ICs.

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With the scaled clearance between PMOS and NMOS devices in advanced semiconductor technology, it has been proven that such electrical-transient noises can cause transient-induced latchup (TLU) failure on the inevitable parasitic silicon-controlled rectifier in CMOS ICs [10], [11]. The reliability issue of system-level electrical-transient disturbance results from not only the progress of more integrated circuit blocks into a single chip but also from the strict requirements of reliability performance requested by the IC industry, such as the system-level electrostatic-discharge (ESD) test of the IEC 61000-4-2 standard [12] and the electrical-fast-transient (EFT) test of the IEC 61000-4-4 standard [13].

It has been observed during system-level ESD and EFT tests that the ESD-generated or EFT-induced transient voltages are quite large (with amplitudes of up to hundreds of volts), fast (with periods of several tens of nanoseconds), and randomly exist on the power, ground, and input/output (I/O) pins of the ICs inside the microelectronic system. High-voltage electrical fast transients often cause the CMOS ICs inside the equipment under test (EUT) to be upset or frozen after system-level electrical-transient disturbance. It has been reported that system-level electrical-transient disturbance coupled to the power and ground pins of a super-twisted nematic liquid-crystal-display (LCD) driver circuit had been reported to cause abnormal function of the LCD panel [14]. The CMOS ICs inside the microelectronic products are very susceptible to system-level electrical-transient disturbance [15]–[17], even though they have passed the component-level ESD specifications, such as the human-body model of ± 2 kV, the machine model of ± 200 V, and the charged-device model of ± 1 kV.

In order to protect the microelectronic system against transient disturbance events, the traditional solution used in microelectronic products is to add some discrete noise-bypassing components or board-level noise filters into the printed circuit board (PCB) to decouple, bypass, or absorb the electrical-transient energy under system-level electrical-transient disturbance conditions [18]–[20]. The immunity of CMOS ICs against the system-level electrical-transient disturbance test can be significantly enhanced by choosing the proper noise filter networks added into the PCB together. However, the additional discrete noise-bypassing components substantially increase the total cost of microelectronic products. Therefore, the chip-level solutions to meet the high-transient-disturbance immunity specification for microelectronic products without additional discrete noise-decoupling components added on the PCB are highly desired by the IC industry [21]–[23].

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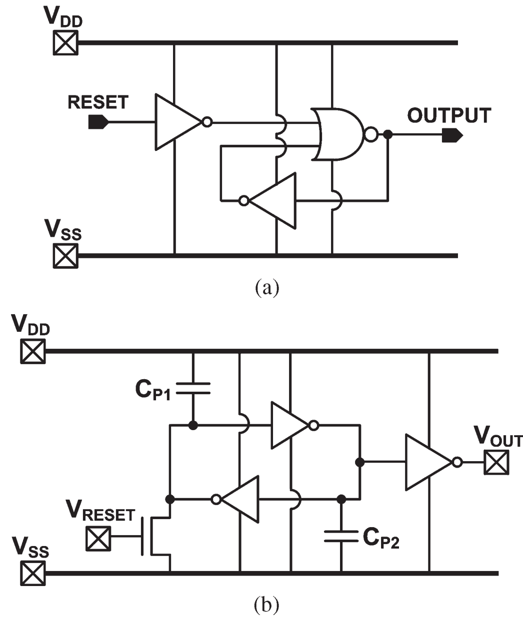


Fig. 1. Previous on-chip transient detection circuits composed of (a) a latch circuit and (b) a latch circuit with additional capacitors (C_{P1} and C_{P2}) to enhance the detection sensitivity.

In previous works, two on-chip transient detection circuits have been proposed to detect transient noise, as shown in Fig. 1(a) and (b). The circuit structure in Fig. 1(a) is composed of a latch circuit [15]. The detection sensitivity was adjusted by the device ratio between PMOS and NMOS in the latch circuit. The modified design in Fig. 1(b) was realized with additional capacitors (C_{P1} and C_{P2}) located between $V_{\rm DD}/V_{\rm SS}$ power lines and the I/O nodes of the latch circuit to enhance its detection sensitivity [21]. However, the detection sensitivity could be degraded by the large on-chip decoupling capacitors between power lines in the CMOS IC products.

In this paper, a new on-chip transient detection circuit is proposed to detect the positive and negative electrical transients under system-level ESD or EFT tests [24]. By using a longer time delay in the RC circuit during system-level ESD and EFT tests, the proposed transient detection circuit can memorize the occurrence of electrical-transient disturbance events. It had been proven that the hardware/firmware codesign can effectively improve the electrical-transient disturbance robustness of CMOS ICs in microelectronic products [15]. When system-level electrical-transient disturbance happens, the detection results from the proposed transient detection circuit can be stored as a firmware index to start the system recovery procedure after the disturbance events. The circuit function to detect different positive or negative electrical transients has been investigated by HSPICE simulation and verified by silicon chip. The TLU measurement method [25], the system-level ESD gun [26], and the EFT generator with an attenuation network and a capacitive coupling clamp [27] are used to evaluate the detection function of the proposed transient detection circuit. The experimental results in a 0.18-μm CMOS process have verified that the proposed transient detection circuit can successfully detect and memorize the occurrence of electrical transients during system-level ESD or EFT testing conditions.

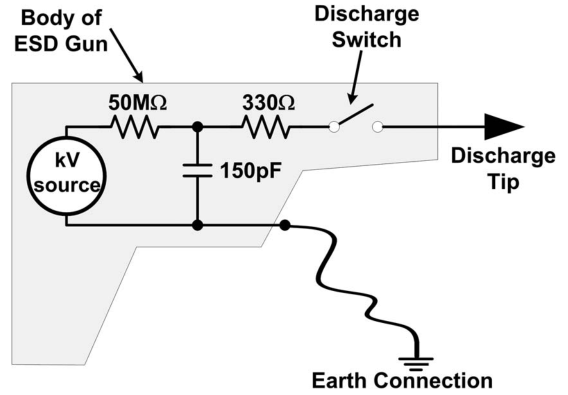


Fig. 2. Equivalent circuit of the ESD gun used in the system-level ESD test [12].

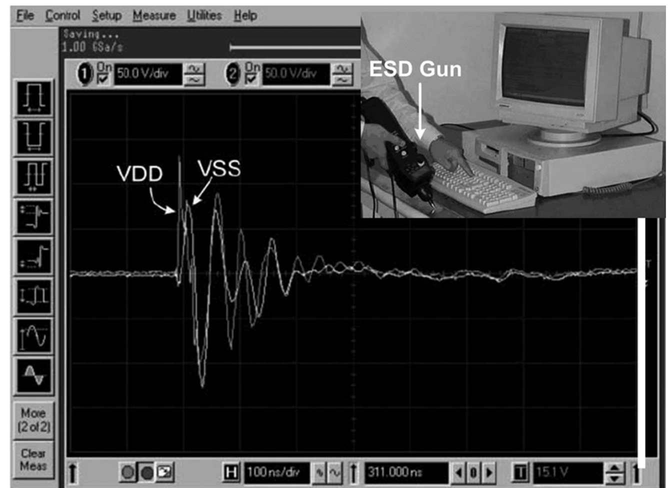


Fig. 3. Measured $V_{\rm DD}$ and $V_{\rm SS}$ waveforms of the microcontroller ICs inside the keyboard under system-level ESD test [22].

II. Tests of System-Level Electrical-Transient Disturbance

A. System-Level ESD Test

The standard of IEC 61000-4-2 defines the immunity requirements and test methods for microelectronic products to a system-level ESD event [12]. Under system-level ESD tests, the ESD energy is released from the ESD gun. The equivalent circuit of the ESD gun used in the system-level ESD test is shown in Fig. 2. Different discharge tips are used for two different discharge test modes. The round tip of the ESD gun is used for the air-discharge test and brought close to the EUT. The sharp tip of the ESD gun is used for the contact-discharge test and held in contact with the EUT. The ESD gun has a charging (energy-storage) capacitor of 150 pF and a discharging resistor of 330 Ω. It has been reported that a robust CMOS IC product with high component-level ESD level could still be very susceptible to the system-level ESD test [15]. The inset of Fig. 3 shows an EUT (keyboard) that was stressed by an ESD gun with a charged voltage of +1 kV zapping on the horizontal coupling plane (HCP). During the system-level ESD test, the power/ground lines of the microcontroller IC inside the keyboard no longer maintain their normal voltage levels, but an

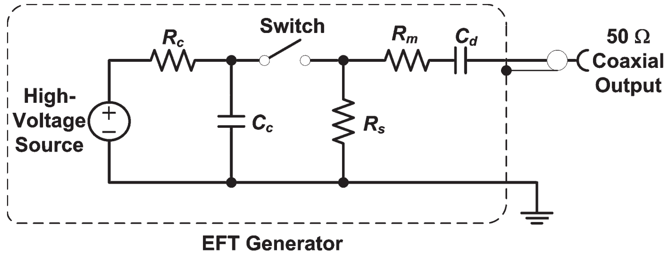


Fig. 4. Simplified circuit diagram of the EFT generator [13].

underdamped sinusoidal voltage with an amplitude of several tens of volts occurred, as shown in Fig. 3.

B. EFT Test

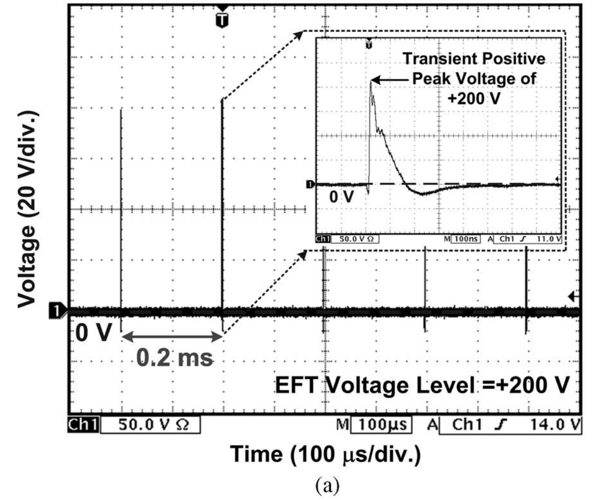
The standard of IEC 61000-4-4 defines the immunity requirements and test methods for electronic equipment to repetitive fast transients [13]. The EFT is a test with repetitive burst string consisting of a number of fast pulses, coupled to the power supply, control, signal, and ground ports of microelectronic products. The characteristics of EFT are high amplitude, short rise time, and high repetition rate of the transients. The EFT test is intended to demonstrate the immunity of microelectronic products to transient disturbances, such as those originating from switching transients (interruption of inductive loads, relay contact bounce, etc.).

According to the standard of IEC 61000-4-4, the simplified circuit diagram of the EFT generator is shown in Fig. 4, with an impedance-matching resistor R_m of 50 Ω and a dc-blocking capacitor C_d of 10 nF. The charging capacitor C_c is used to store the charging energy, and R_c is the charging resistor. Resistor R_s is used to shape the pulse duration.

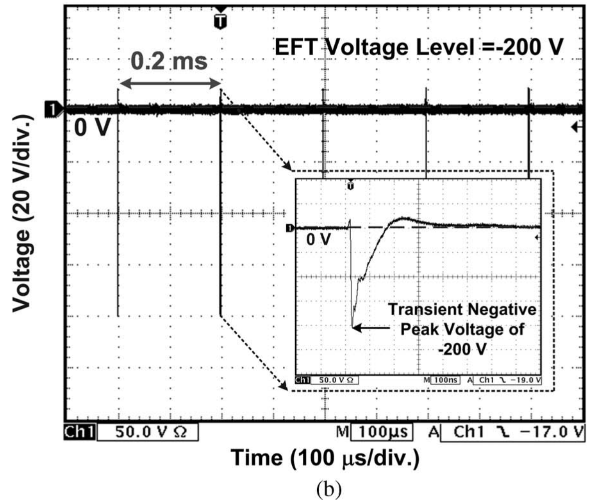
The standard of IEC 61000-4-4 defines the test voltage waveforms of these fast transients with repetition frequencies of 5 and 100 kHz. The use of 5-kHz repetition rate is the traditional EFT test, and 100 kHz is closer to reality. For an EFT pulse with a repetition frequency of 5 kHz, there are 75 pulses in each burst string, and the burst duration time is 15 ms. For an EFT pulse with a repetition frequency of 100 kHz, there are 75 pulses in each burst string, and the burst duration time is only 0.75 ms. For both repetition rates, the burst string repeats every 300 ms.

For EFT pulses with a repetition frequency of 5 kHz, the measured +200- and −200-V voltage waveforms on the 1-kΩ load are shown in Fig. 5(a) and (b), respectively. Because the output loading (1 kΩ) is larger than impedance-matching resistor R_m (50 Ω), the measured output pulse peak is close to the input EFT voltage pulse. As shown in Fig. 5(a) and (b), the measured output pulse peaks on the 1-kΩ load are approximately +200 and −200 V, respectively. For an EFT repetition frequency of 5 kHz, the time interval between each pulse is 0.2 ms. Under EFT tests, the application time should not be less than 1 min, and both polarities have to be tested.

With the 1-kΩ load, the voltage waveforms of a single pulse with EFT voltages of +200 and −200 V are shown in the inset of Fig. 5(a) and (b), respectively. The EFT waveforms of a single pulse have a rise time of ∼5 ns and a pulse duration (time interval at half of the peak EFT voltage) of ∼50 ns.



(a)



(b)

Fig. 5. Measured voltage waveforms under EFT tests with EFT voltages of (a) +200 V and (b) −200 V on a 1-kΩ load with a repetition rate of 5 kHz.

III. New Transient Detection Circuit

The transient detection circuit is designed to detect the positive or negative fast electrical transients after system-level ESD or EFT tests. Under normal power supply condition ($V_{\rm DD} = 1.8$ V), the output state ($V_{\rm OUT}$) of the proposed transient detection circuit is kept at 0 V as logic "0." After transient disturbance, the output state ($V_{\rm OUT}$) of the proposed transient detection circuit will transit from 0 to 1.8 V as logic "1." Therefore, the proposed transient detection circuit can memorize the occurrence of transient disturbance events.

A. Circuit Implementation

Fig. 6 shows the proposed transient detection circuit. An NMOS ($M_{\rm nr}$) is used to provide the initial reset function to set the initial voltage level to 0 V at node V_1 and the output node ($V_{\rm OUT}$). C_P is the parasitic capacitance on node V_1 of the transient detection circuit. In Fig. 6, node V_X is biased at $V_{\rm DD}$ during the normal operating condition. Under system-level ESD or EFT tests, the transient voltage coupled to the $V_{\rm DD}$ line has a fast rise time on the order of nanoseconds. The voltage level of V_X has a much slower voltage response than the voltage

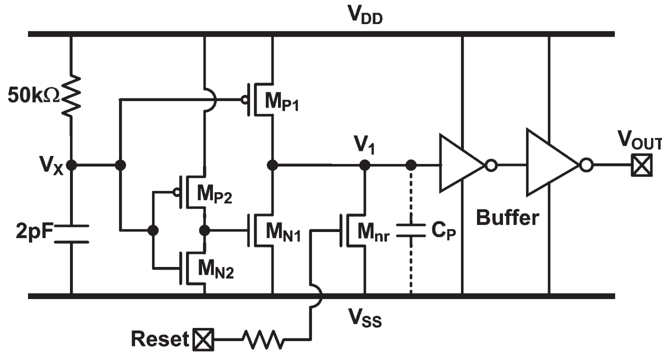


Fig. 6. New proposed on-chip transient detection circuit.

TABLE I
DEVICE DIMENSIONS USED IN THE PROPOSED TRANSIENT DETECTION CIRCUIT

M_{nr}	50/0.18 (μm/μm)
M_{P1}	40/0.18 (μm/μm)
M_{N1}	10/0.18 (μm/μm)
M_{P2}	24/0.18 (μm/μm)
M_{N2}	24/0.18 (μm/μm)

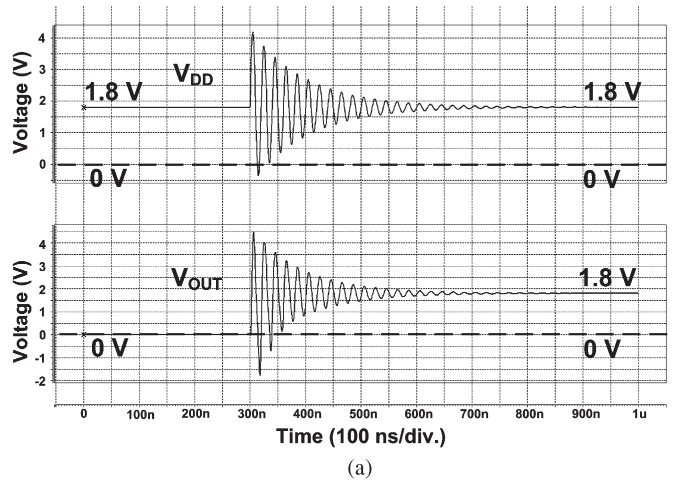
level at $V_{\rm DD}$ because the RC circuit has a time constant on the order of microseconds. Due to the longer delay of the voltage increase at node V_X, the PMOS device (M_{P1}) can be turned on by the overshooting transient voltage at $V_{\rm DD}$ to pull up the voltage level at node V_1. Therefore, the logic level stored at node V_1 can be changed during transient disturbance events. Finally, the output voltage of the proposed transient detection circuit can transit from 0 to 1.8 V to memorize the occurrence of system-level electrical-transient disturbance after system-level ESD or EFT tests. The device dimensions (W/L) used in the proposed transient detection circuit are listed in Table I.

B. HSPICE Simulation

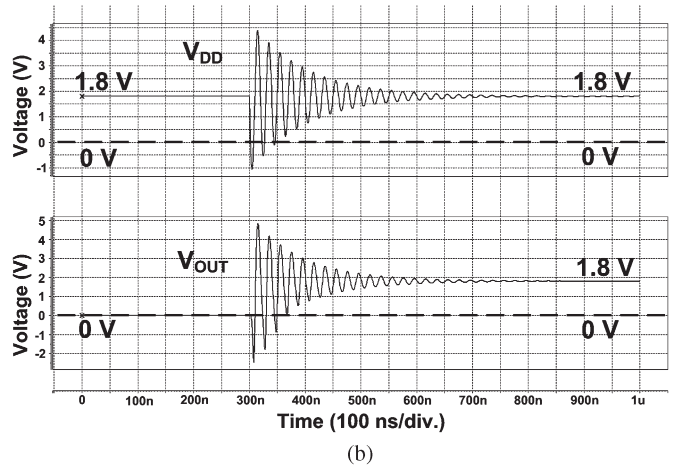
1) System-Level ESD Testing Conditions: From the measured electrical-transient waveforms shown in Fig. 3, the underdamped sinusoidal voltage waveform on the power line of the CMOS IC during system-level ESD stress has been observed. There, a sinusoidal time-dependent voltage source with a damping factor parameter given by

$$V(t) = V_0 + V_a \cdot \sin\left(2\pi f(t - t_d)\right) \cdot \exp\left(-(t - t_d)D_a\right) \quad (1)$$

is used to simulate an underdamped sinusoidal voltage on the power lines of the proposed transient detection circuit. With the proper parameters (including applied voltage amplitude V_a, initial dc voltage V_0, damping factor D_a, frequency f, and time delay t_d), the underdamped sinusoidal voltage can be used to simulate the electrical-transient waveforms under system-level ESD tests. In HSPICE simulation with positive- or negative-going underdamped sinusoidal waveforms, the same parameters of $D_a = 2 \times 10^7\ \text{s}^{-1}$, $f = 50$ MHz, and $t_d = 300$ ns are used (which is corresponding to the measured transient waveforms in Fig. 3). For the positive-going (negative-going) underdamped sinusoidal waveform, the polarity of V_a parameter is positive (negative). V_0 is the initial voltage of the applied



(a)



(b)

Fig. 7. Simulated $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms of the new proposed on-chip transient detection circuit under system-level ESD test with (a) positive-going and (b) negative-going underdamped sinusoidal voltages.

transient waveform. When the transient waveform is applied to $V_{\rm DD}$ $(V_{\rm SS})$, V_0 is set to 1.8 V (0 V) in the simulation.

The simulated $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms of the proposed transient detection circuit with a positive-going underdamped sinusoidal voltage on the $V_{\rm DD}$ line are shown in Fig. 7(a). The positive-going underdamped sinusoidal voltage with an amplitude of $+2.5$ V is used to simulate the coupling ESD transient noise under system-level ESD test. From the simulated waveforms, $V_{\rm DD}$ begins to increase rapidly from 1.8 to 4 V. $V_{\rm OUT}$ also acts with a positive-going underdamped sinusoidal voltage waveform during the simulated transient disturbance on the $V_{\rm DD}$ line. After this disturbance duration, $V_{\rm DD}$ returns to its normal voltage level of 1.8 V, and the output state $(V_{\rm OUT})$ of the proposed transient detection circuit is changed from 0 to 1.8 V, as shown in Fig. 7(a). As a result, the proposed transient detection circuit can detect the occurrence of positive-going ESD-induced underdamped sinusoidal transient disturbance on the $V_{\rm DD}$ line.

The simulated $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms of the proposed transient detection circuit with a negative-going underdamped sinusoidal voltage on $V_{\rm DD}$ are shown in Fig. 7(b). The negative-going underdamped sinusoidal voltage with an amplitude of -3 V is used to simulate the coupling ESD transient noise under system-level ESD test with negative voltage. From the

simulated waveforms, $V_{\rm DD}$ begins to decrease rapidly from 1.8 to -1 V. $V_{\rm OUT}$ also acts with a negative-going underdamped sinusoidal voltage waveform during the simulated transient disturbance on the $V_{\rm DD}$ line. After this disturbance duration, $V_{\rm DD}$ returns to its normal voltage level of 1.8 V, and the output state $(V_{\rm OUT})$ of the proposed transient detection circuit is changed from 0 to 1.8 V, as shown in Fig. 7(b). Therefore, the proposed transient detection circuit can detect the occurrence of negative-going ESD-induced underdamped sinusoidal transient disturbance on the $V_{\rm DD}$ line.

2) EFT Testing Conditions: For microelectronic products, the shielding plate is often designed into microelectronic products to bypass or reduce the EFT-induced electrical-transient disturbance. Therefore, the electrical transients injected into the CMOS ICs inside the microelectronic products can be degraded with smaller amplitude compared with the original testing voltage. Therefore, the EFT-induced transients with different degraded amplitudes are taken into considerations in HSPICE simulation on the proposed transient detection circuit.

From the measured electrical-transient waveforms shown in Fig. 5(a) and (b), the approximated exponential voltage pulse waveforms during EFT tests have been observed. There, an exponential pulse time-dependent voltage source with rise/fall-time constant parameters is used to simulate EFT-induced transient disturbance on the proposed transient detection circuit. The rising edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(\rm rise)}(t) = V_1 + (V_2 - V_1) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right)\right], \quad \text{when } t_{d1} \le t \le t_{d2}. \quad (2)$$

The falling edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(\rm fall)}(t) = V_1 + (V_2 - V_1) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right)\right] + (V_1 - V_2)\left[1 - \exp\left(-\frac{t - t_{d2}}{\tau_2}\right)\right], \text{ when } t \ge t_{d2}. \quad (3)$$

With the proper parameters (including rise-time constant τ_1, fall-time constant τ_2, rise-time delay t_{d1}, fall-time delay t_{d2}, initial dc voltage value V_1, and exponential pulse voltage value V_2), the exponential voltage pulse can be constructed to simulate the EFT-induced disturbance under EFT tests. In HSPICE simulation with positive or negative exponential voltage pulse waveforms, the same parameters of $\tau_1 = 3$ ns, $\tau_2 = 25$ ns, and $t_{d2} - t_{d1} = 10$ ns are used [which is corresponding to the measured transient waveforms in Fig. 5(a) and (b)].

For the positive exponential voltage pulse, the value of V_2 parameter is larger than the value of V_1 parameter. For the negative exponential voltage pulse, the polarity of $V_2 - V_1$ parameter is negative. In addition, V_1 is 1.8 V as the initial dc voltage on the $V_{\rm DD}$ line of the proposed transient detection circuit.

The simulated $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms of the proposed transient detection circuit with a positive exponential pulse transient disturbance on the $V_{\rm DD}$ line are shown in Fig. 8(a).

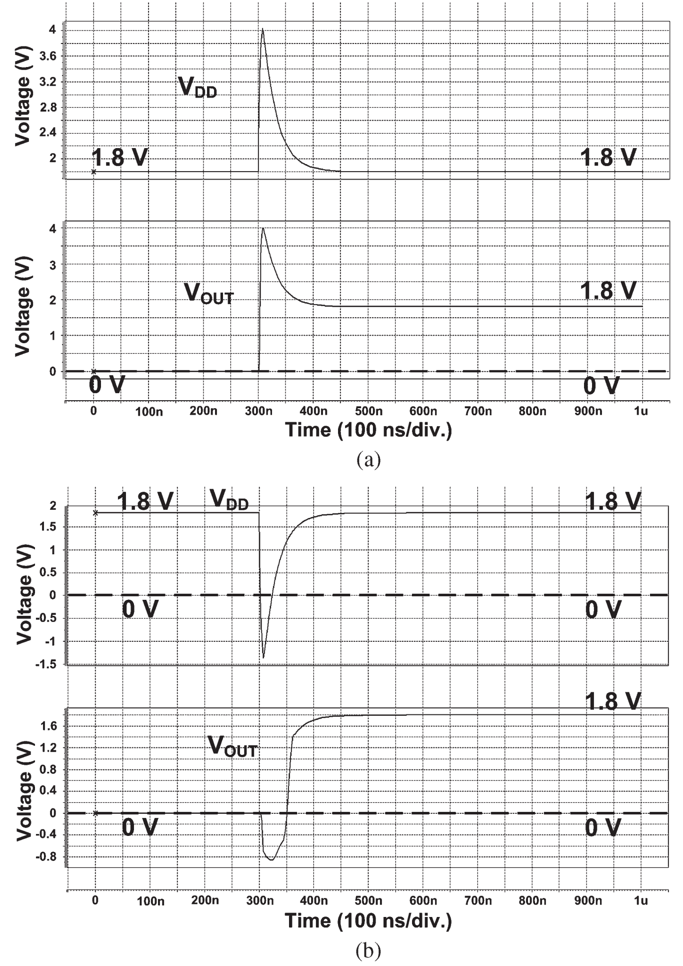


Fig. 8. Simulated $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms of the new proposed on-chip transient detection circuit under EFT tests with (a) positive and (b) negative exponential voltage pulse waveforms coupled to $V_{\rm DD}$.

The exponential voltage pulse with an amplitude of $+2.5$ V is used to simulate the coupling positive transient disturbance under EFT test. From the simulated waveforms, $V_{\rm DD}$ begins to increase rapidly from 1.8 to $+4$ V. $V_{\rm OUT}$ also acts with a positive exponential voltage pulse waveform during the simulated transient disturbance on the $V_{\rm DD}$ line. After the transient disturbance duration, $V_{\rm DD}$ returns to its normal voltage level of 1.8 V, and the output state $(V_{\rm OUT})$ of the proposed transient detection circuit transits from 0 to 1.8 V, as shown in Fig. 8(a). As a result, the proposed transient detection circuit can detect the occurrence of positive EFT-induced exponential pulse transient disturbance.

The simulated $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms of the proposed transient detection circuit with a negative exponential pulse transient disturbance on the $V_{\rm DD}$ line are shown in Fig. 8(b). The exponential voltage pulse with an amplitude of -3.5 V is used to simulate the coupling negative transient disturbance under EFT test. From the simulated waveforms, $V_{\rm DD}$ begins to decrease rapidly from 1.8 to -1 V. $V_{\rm OUT}$ also acts with a negative exponential voltage pulse during the simulated transient disturbance on the $V_{\rm DD}$ line. After the transient disturbance duration, $V_{\rm DD}$ returns to its normal voltage level of 1.8 V, and the output state $(V_{\rm OUT})$ of the proposed transient detection

circuit transits from 0 to 1.8 V, as shown in Fig. 8(b). As a result, the proposed transient detection circuit can detect the occurrence of negative EFT-induced exponential pulse transient disturbance.

From the aforementioned simulation results shown in Fig. 8(a) and (b), the proposed transient detection circuit can successfully memorize the occurrence of positive or negative EFT-induced exponential pulse transient disturbance.

C. Consideration With Leakage

The voltage level at node V_1 of the proposed transient detection circuit will be charged high after ESD/EFT electrical transitions, such as those shown in the aforementioned simulation results to get the output node voltage changing from 0 V to 1.8 V. However, after electrical transition, M_{P1} and M_{N1} will be switched to OFF state again. The charged voltage at node V_1 would be leaked down due to the parasitic drain junction diodes of the transistors in the circuit. If the leakage current of the parasitic diodes of the transistors connecting to parasitic capacitance (C_P) on node V_1 is taken into consideration, the discharge time of the charged V_1 with this parasitic capacitance to cause the output node V_{OUT} to return to 0 V due to leakage can be estimated from the following:

$$C_P \times \left(V_{1(\max)} - \frac{V_{\mathrm{DD}}}{2}\right) = I_{\mathrm{Leakage}} \times \Delta t \tag{4}$$

where I_{Leakage} is the leakage current. The logic threshold voltage of the buffer stage is often designed about half of the supplied voltage. The maximum voltage staying on node V_1 will be around V_{DD} plus the threshold voltage of the M_{P1} device. The higher voltage charged to node V_1 will be discharged back to V_{DD} through the channel current of the M_{P1} device after ESD/EFT electrical transitions. The parasitic capacitance (C_P) is about 0.3 pF in this design, with the device dimensions being listed in Table I. If the leakage current is assumed to be 30 pA (process-dependent parameter), the estimated discharge time is about 10 ms, which is long enough for the firmware to execute system autorecovery procedures. After that, node V_1 will be reset to 0 V again for detecting the next events of ESD or EFT transitions.

IV. Experimental Results

The proposed transient detection circuit has been designed and fabricated in a 0.18-μm 1P5M CMOS process. The fabricated chip for transient disturbance tests is shown in Fig. 9.

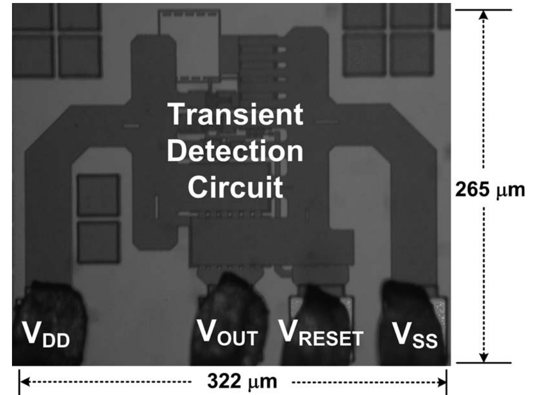


Fig. 9. Die photograph of the new proposed on-chip transient detection circuits fabricated in a 0.18-μm CMOS process.

A. TLU Test

With the system-level ESD test, it can only judge whether the EUT passes the required criterion through its abnormal function (e.g., EUT shuts down). Nevertheless, it is hard to directly evaluate the system-level ESD immunity of a single IC inside the EUT. To solve this problem, a component-level TLU measurement setup was reported [28] with the following two advantages. First, the TLU immunity of a single IC can be evaluated by the measured voltage and current waveforms through an oscilloscope. Second, with the ability of generating an underdamped sinusoidal voltage, how an IC inside the EUT is disturbed by the ESD-generated noise during the system-level ESD test can be accurately simulated. Fig. 10 shows such a component-level TLU measurement setup. An ESD simulator is used to generate the TLU-triggering source (V_{Charge}) to produce an underdamped sinusoidal voltage stimulus. By applying a positive (negative) charged voltage V_{Charge}, the intended positive-going (negative-going) underdamped sinusoidal voltage can be generated similarly with that generated from the ESD gun during the system-level ESD test.

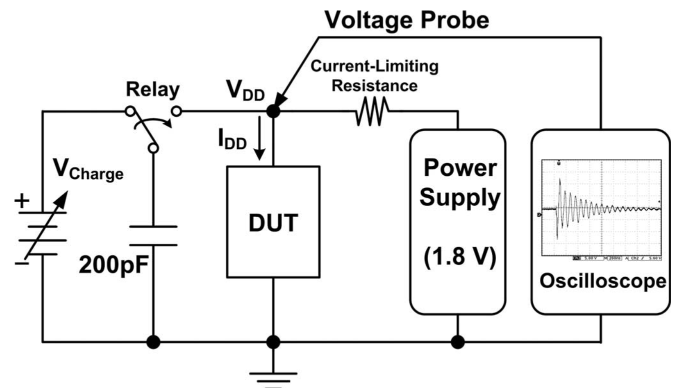
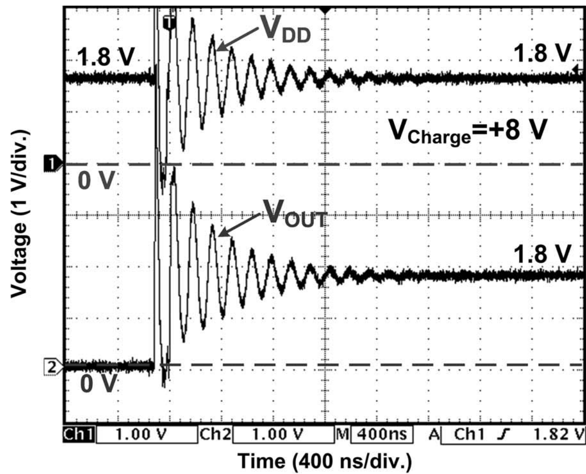


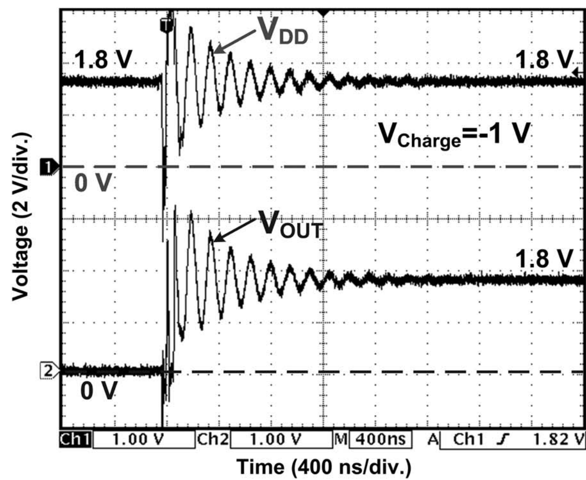
Fig. 10. Measurement setup for TLU [25].

In the measurement setup shown in Fig. 10, a charging capacitance of 200 pF is used to store charges for the TLU-triggering source (V_{Charge}), and then, these stored charges are discharged to the device under test (DUT) through a relay. The intended underdamped sinusoidal voltage can be produced to simulate the transient voltage on the power pins of CMOS ICs under system-level ESD test, no matter which polarity (positive or negative) the ESD voltage is. Moreover, a small current-limiting resistance of 5 Ω is recommended to protect the DUT from electrical-overstress damage during a high-current (low-impedance) latchup state [25]. A supply voltage of 1.8 V is used as V_{DD}, and the triggering source is directly connected to the DUT through the relay in the measurement setup.

Fig. 11(a) and (b) shows the measured V_{DD} and V_{OUT} transient responses of the proposed transient detection circuit under TLU test with V_{Charge}'s of $+8$ and -1 V, respectively.



(a)



(b)

Fig. 11. Measured V_{DD} and V_{OUT} waveforms on the new proposed on-chip transient detection circuit under TLU tests with V_{Charge}'s of (a) $+8$ V and (b) -1 V.

As shown in Fig. 11(a), under TLU test with a V_{Charge} of $+8$ V, V_{DD} begins to increase rapidly from 1.8 V with positive-going underdamped sinusoidal voltage waveform. During the TLU test, V_{OUT} is influenced simultaneously with positive-going underdamped sinusoidal voltage coupled to the V_{DD} power line. After the TLU test with a V_{Charge} of $+8$ V, the output voltage (V_{OUT}) of the proposed transient detection circuit can transit from 0 to 1.8 V. In Fig. 11(b), under TLU test with a V_{Charge} of -1 V, V_{DD} begins to decrease rapidly from 1.8 V with negative-going underdamped sinusoidal voltage waveform. During the TLU test, V_{OUT} is influenced simultaneously with negative-going underdamped sinusoidal voltage coupled to the V_{DD} power line. After the TLU test with a V_{Charge} of -1 V, the output voltage (V_{OUT}) of the proposed transient detection circuit can transit from 0 to 1.8 V.

From the TLU test results, the proposed transient detection circuit can successfully memorize the occurrence of electrical transients. With positive or negative underdamped sinusoidal voltages coupled to the V_{DD} power line, the output voltages (V_{OUT}'s) of the proposed transient detection circuit can be changed from 0 to 1.8 V after TLU tests.

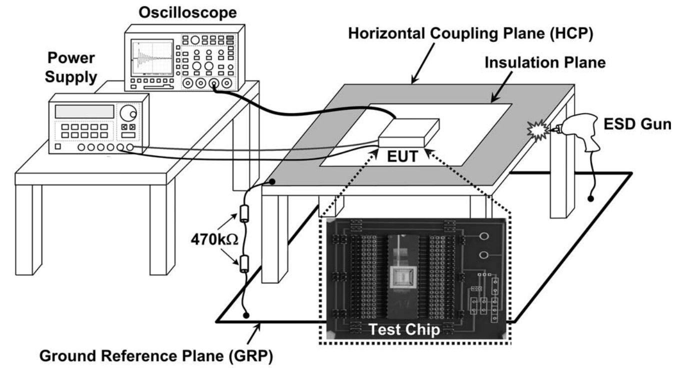


Fig. 12. Measurement setup for a system-level ESD test with indirect contact-discharge test mode [12] to evaluate the detection function of the fabricated on-chip transient detection circuit.

B. System-Level ESD Test

In IEC 61000-4-2, two test modes have been specified, which are the air- and contact-discharge test modes. In the case of air-discharge test mode, the round discharge tip should be approached as fast as possible to touch the EUT. The air discharge is actuated by a spark to the EUT, and the ESD energy holding time is at least 5 s. The contact discharge is applied to the conductive surfaces of the EUT (direct application) or to the horizontal or vertical coupling planes (indirect application). Fig. 12 shows the measurement setup of the system-level ESD test standard with indirect contact-discharge test mode. The measurement setup of the system-level ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulation plane is used to separate the EUT from the HCP. The HCP is connected to the GRP with two 470-kΩ resistors in series. When the ESD gun zaps the HCP, the electromagnetic interference coming from the ESD gun will be coupled into all CMOS ICs inside the EUT. The power lines of the CMOS ICs inside the EUT will be disturbed by the ESD-coupled energy.

According to the IEC 61000-4-2 standard, under system-level ESD test with direct contact-discharge test mode, the discharge tip should apply to the metallic shell or accessible connector/surface of microelectronic products. The ESD-induced transient disturbance can couple into the CMOS ICs inside the microelectronic products. Therefore, under system-level ESD with direct/indirect contact-discharge modes, the CMOS ICs inside the microelectronic products are suffering the coupled ESD-induced electrical-transient disturbance. By using the insulation plane between the EUT and HCP, the indirect contact-discharge mode can couple ESD transient noise into the test chip inside the PCB. Therefore, in this paper, the indirect contact-discharge mode is used as the test mode to evaluate the detection function/performance of the proposed transient detection circuit.

By using a digital oscilloscope, the transient responses on the power lines and output signals of CMOS IC products can be recorded and analyzed. Before each system-level ESD test, the initial output voltage (V_{OUT}) of the proposed transient detection circuit is reset to 0 V. After each system-level ESD test, the output-voltage (V_{OUT}) level is monitored to check the

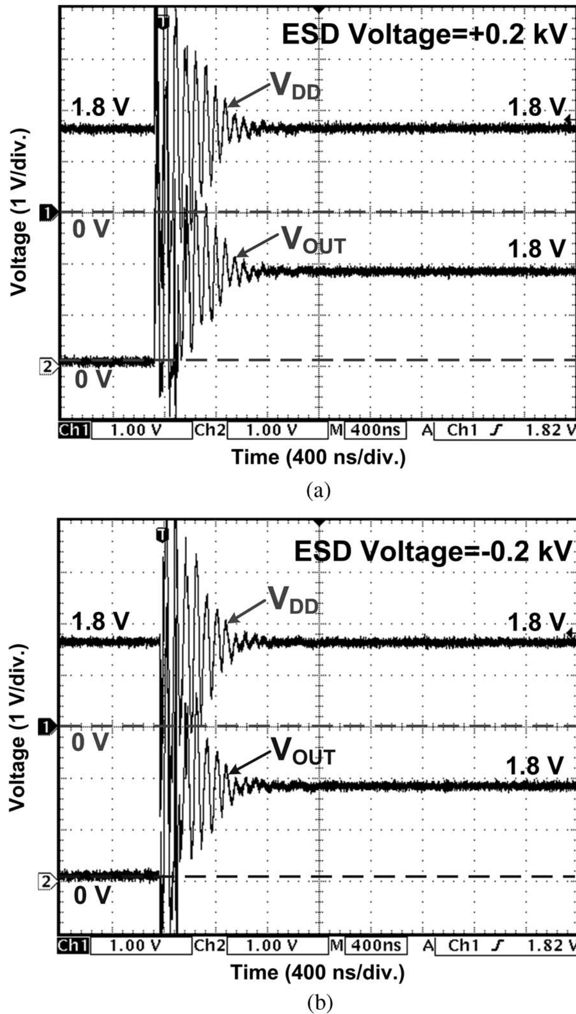


Fig. 13. Measured V_{DD} and V_{OUT} transient voltage waveforms of the new proposed on-chip transient detection circuit under system-level ESD tests with ESD voltages of (a) +0.2 kV and (b) −0.2 kV.

final voltage level and to verify the detection function. Thus, the circuit function of the proposed transient detection circuit can be evaluated by the system-level ESD test.

The measured V_{DD} and V_{OUT} waveforms of the proposed transient detection circuit under system-level ESD test with an ESD voltage of +0.2 kV zapping on the HCP are shown in Fig. 13(a). V_{DD} begins to increase rapidly from the normal voltage of +1.8 V. Meanwhile, V_{OUT} is disturbed under such a high-energy ESD stress. During the period with positive-going ESD-induced electrical-transient disturbance, V_{DD} and V_{OUT} are influenced simultaneously. Finally, the output voltage (V_{OUT}) of the proposed transient detection circuit transits from 0 to 1.8 V. Therefore, the proposed transient detection circuit can sense the positive-going electrical transient on the power line and memorize the occurrence of system-level ESD event.

The measured V_{DD} and V_{OUT} transient voltage waveforms of the proposed transient detection circuit with an ESD voltage of −0.2 kV zapping on the HCP under system-level ESD test are shown in Fig. 13(b). During the negative-going ESD-induced electrical-transient disturbance on the V_{DD} power line, V_{OUT} is disturbed simultaneously. After the system-level ESD test with

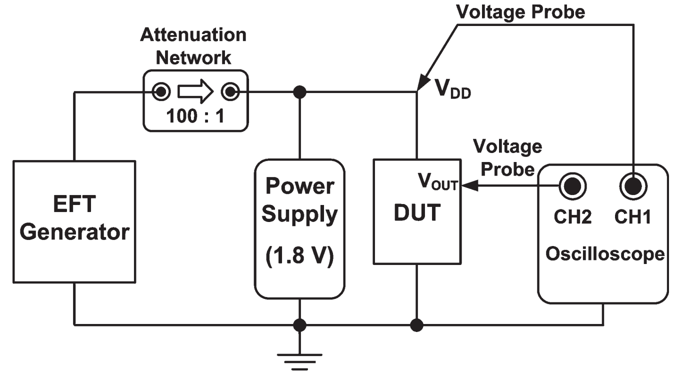


Fig. 14. Measurement setup for an EFT test combined with an attenuation network.

an ESD voltage of −0.2 kV, V_{OUT} transits from 0 to 1.8 V. The detection function of the transient detection circuit after system-level ESD tests has been verified by the experimental results in silicon chip and HSPICE simulation.

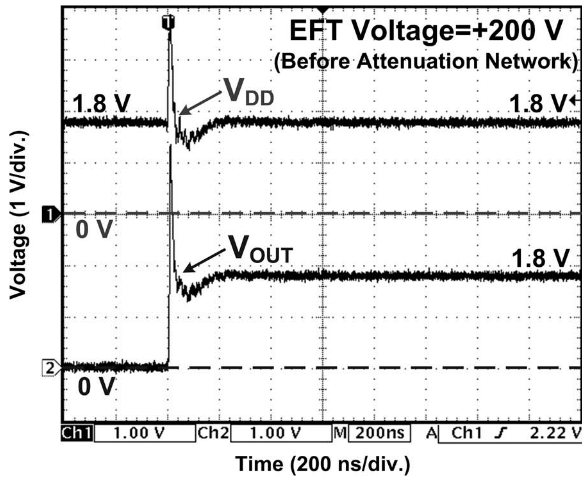
C. EFT Test

In order to simulate the EFT-induced transient disturbance on CMOS ICs inside the microelectronic products, the attenuation network with −40 dB degradation is used in this paper. The amplitude of EFT-induced transients can be adjusted through the attenuation network.

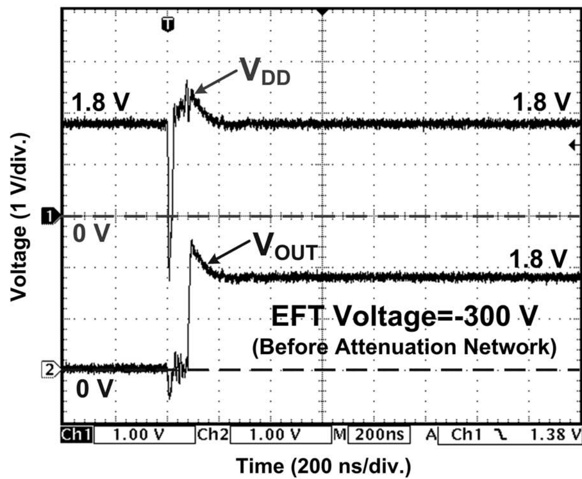
The measurement setup for the EFT test combined with the attenuation network is shown in Fig. 14. The EFT generator is connected to the DUT through the attenuation network with a V_{DD} of 1.8 V. The V_{DD} and V_{OUT} transient responses of the proposed transient detection circuit are monitored by a digital oscilloscope. Before each EFT test, the initial output voltage (V_{OUT}) of the proposed transient detection circuit is reset to 0 V. After each EFT test, the output-voltage (V_{OUT}) level is monitored to check the final voltage level and to verify the detection function.

Fig. 15(a) and (b) shows the measured V_{DD} and V_{OUT} transient responses of the proposed transient detection circuit under EFT tests with input EFT voltages of +200 and −300 V, respectively. As shown in Fig. 15(a), under EFT test with a positive voltage of +200 V, V_{DD} begins to increase rapidly from 1.8 V with positive exponential voltage pulse. During the EFT test, V_{OUT} is influenced simultaneously with positive exponential voltage pulse coupled to the V_{DD} power line. After the EFT test, the output voltage (V_{OUT}) of the proposed transient detection circuit transits from 0 to 1.8 V. In Fig. 15(b), under EFT test with a negative voltage of −300 V, V_{DD} begins to decrease rapidly from 1.8 V with negative exponential voltage pulse. After the EFT test, the output voltage (V_{OUT}) of the proposed transient detection circuit transits from 0 to 1.8 V.

From the EFT test results shown in Fig. 15(a) and (b), with positive or negative exponential voltage pulses coupled to the V_{DD} power line, the output voltages (V_{OUT}) of the proposed transient detection circuit can be changed from 0 to 1.8 V. The experimental results are consistent with the HSPICE simulation results under positive and negative EFT zapping conditions, as shown in Fig. 8(a) and (b). Therefore, the proposed transient



(a)



(b)

Fig. 15. Measured V_{DD} and V_{OUT} waveforms on the new proposed on-chip transient detection circuit under EFT tests with (a) positive and (b) negative EFT voltages combined with an attenuation network.

detection circuit can successfully memorize the occurrence of EFT-induced exponential pulse transient disturbance.

In IEC 61000-4-4, the capacitive coupling clamp has been recommended as another measurement setup to couple the EFT testing voltages into the EUT. The capacitive coupling clamp provides the ability of coupling the fast transients and bursts to the circuit under test without any galvanic connection to the terminals of the EUT, shielding the cables or any other part of the EUT. The coupling capacitance of the clamp depends on the diameter, material of the cables, and shielding. The typical coupling capacitance between the cable and clamp ranges from 50 to 200 pF. For providing maximum coupling capacitance between the cable and the clamp, the EFT generator is connected to the end of the clamp that is nearest to the EUT.

The measurement setup for the EFT test combined with the capacitive coupling clamp is shown in Fig. 16. The capacitive coupling clamp is connected with the EFT generator to directly couple the EFT testing voltages into the V_{DD} cable line. The V_{DD} and V_{OUT} voltage waveforms of the proposed transient detection circuit are monitored by a digital oscilloscope during EFT tests combined with the capacitive coupling clamp.

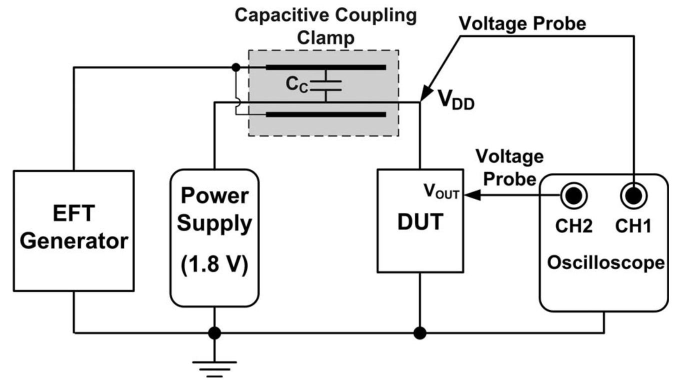
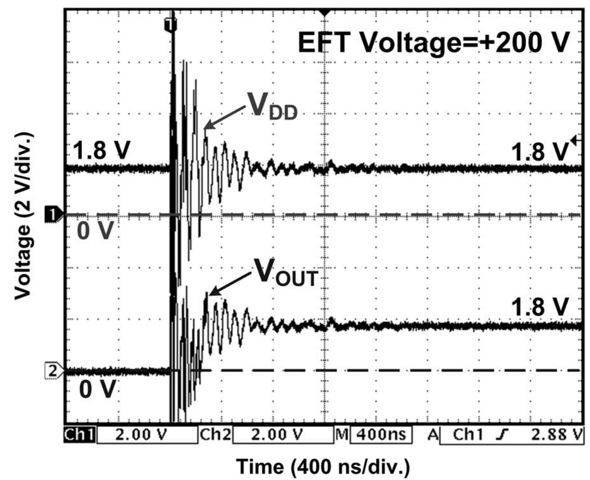
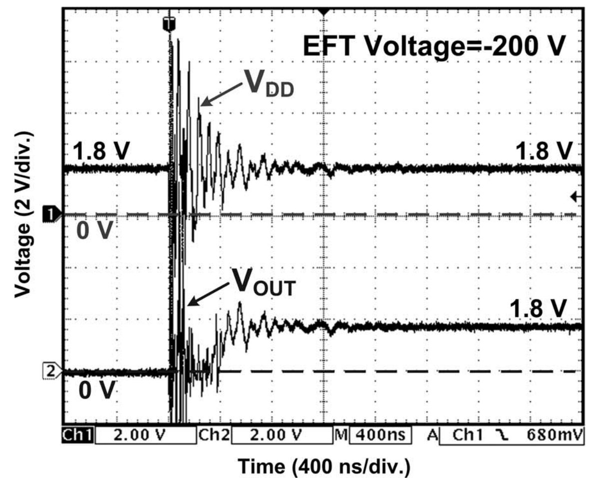


Fig. 16. Measurement setup for an EFT test combined with a capacitive coupling clamp.



(a)



(b)

Fig. 17. Measured V_{DD} and V_{OUT} transient voltage waveforms of the new proposed on-chip transient detection circuit under EFT tests with EFT voltages of (a) +200 V and (b) −200 V combined with a capacitive coupling clamp.

Fig. 17(a) and (b) shows the measured V_{DD} and V_{OUT} transient responses of the proposed transient detection circuit under EFT test with input EFT voltages of +200 and −200 V, respectively. As shown in Fig. 17(a), under EFT tests with an input EFT voltage of +200 V, V_{DD} begins to increase rapidly from 1.8 V with positive-going underdamped sinusoidal voltage

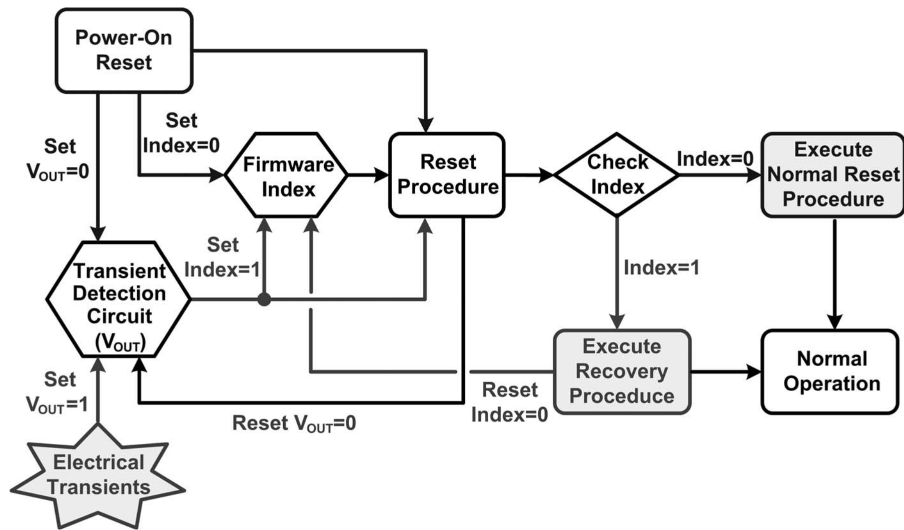


Fig. 18. Firmware flowchart to recover the system when electrical transients happen.

waveform. During the EFT test, V_{OUT} is influenced simultaneously with positive-going underdamped sinusoidal voltage coupled to the V_{DD} power line. After the EFT test with an input EFT voltage of $+200$ V, the output voltage (V_{OUT}) of the proposed transient detection circuit transits from 0 to 1.8 V. In Fig. 17(b), under EFT test with an EFT voltage of -200 V, V_{DD} begins to decrease rapidly from 1.8 V with negative-going underdamped sinusoidal voltage waveform. After the EFT test with an input EFT voltage of -200 V, the output voltage (V_{OUT}) of the proposed transient detection circuit transits from 0 to 1.8 V.

From the EFT test results shown in Fig. 17(a) and (b), the new proposed on-chip transient detection circuit can successfully memorize the occurrence of positive- or negative-going EFT-induced underdamped sinusoidal transient disturbance.

D. Hardware/Firmware Codesign

It has been proven that the hardware/firmware codesign can effectively improve the robustness of microelectronic products against system-level ESD and EFT stresses [21]. To perform the hardware/firmware codesign, the detection result from the transient detection circuit can be temporarily stored as a system recover index for firmware check. For example, the output (V_{OUT}) state of the transient detection circuit is initially reset to logic "0" in the beginning by the power-on reset circuit. When electrical transients happen, the transient detection circuit can detect the occurrence of system-level electrical-transient disturbance and transit the output state (V_{OUT}) to logic "1." At this moment, the system-check index is also changed to logic "1" to initiate the firmware recover procedure to restore the system to a known stable state as soon as possible. After the recover procedure, the output of the transient detection circuit and the firmware index are reset to logic "0" again for detecting the next electrical-transient disturbance events. The firmware flowchart is shown in Fig. 18.

The power-on reset circuit is designed to reset the system operation after power-on transition. Under normal power-on condition, the V_{DD} power-on voltage waveform has a rise time on the order of milliseconds. As there is no input signal except power-on voltage waveform, the power-on reset circuit is often designed with an internal delay that is longer than the rise time of power-on transition. The proposed transient detection circuit is designed to detect the ESD- or EFT-induced fast electrical transients in the range of nanoseconds. However, if the power-on reset circuit would be mistriggered under electrical-transient disturbance, a two-input OR logic-gate circuit can be further added into the hardware/firmware codesign flow. The output signals of the power-on reset and transient detection circuits are connected as the two-input signals of the OR logic gate. When electrical-transient disturbance happens, the system recovery procedure can be still initiated to protect the microelectronic products against the electrical transitions from system-level ESD and EFT events.

V. Conclusion

A new on-chip transient detection circuit has been proposed and successfully verified in a 0.18-μm CMOS process. The detection function under different positive or negative system-level electrical-transient disturbance has been investigated by HSPICE simulation. The experimental results in silicon chip have successfully verified that the proposed transient detection circuit can detect and memorize the occurrence of electrical transients under system-level ESD or EFT testing conditions. With hardware/firmware codesign, the proposed transient detection circuit can be used as a firmware index to provide an effective solution against the malfunction in microelectronic products caused by system-level electrical-transient disturbance.

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