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Low temperature Ni-nanocrystals-assisted hybrid polycrystalline silicon thin film transistor for non-volatile memory applications

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ABSTRACT

The nickel-nanocrystals (Ni-NCs)-embedded silicon nitride acting as a trapping layer has been successfully demonstrated to manipulate the charging and discharging of electrons in a thin film transistor (TFT) for non-volatile memory (NVM) applications. Regarding device performance, with and without Ni-NCs in the stack and under a programming/erasing condition of +/−18 V for 1 s, a better threshold voltage shift of 3.2 V can be reached compared to a shift of 2.0 V for a stack without Ni-NCs. The shift is an index representing the value required to differentiate "0" or "1" states during operation. In this case, the diameter range and number density of Ni-NCs are 5–13 nm and 5.3×10^{11} cm^{-2}, respectively.

1. Introduction

Low temperature poly-Si (LTPS) thin film transistors (TFTs) have been widely studied for applications in driving integrated circuits on glass panels due to their high field effect mobility and driving current [1–3]. Recently, non-volatile memory LTPS-TFT has been further investigated for applications in system-on-panel (SOP), 3-D stacked memory device and organic light-emitting displays (OLEDs) [4–6]. In these applications, the non-volatile memory TFT (NVM-TFT) is a required component. However, one of the problems of the TFT with metal/oxide/nitride/oxide/ silicon (MONOS-TFT) gate stack is their lower programming/erasing (P/E) efficiency due to higher operating voltage (>30 V) across the gate stack required to program or erase carriers [5]. One possible solution is to use metallic-nanocrystals (NCs) as trapping centers [7–9]. They have several advantages, such as larger charging capacity, stronger coupling with the conduction channel, a wider range of available work functions, higher density of states around the Fermi level, and smaller energy perturbation due to carrier confinement. However, most of the NCs studies are not in TFT device applications but on applications in metal/insulator/semiconductor capacitors on Si substrates. In this study, the NVM-TFT with "SiO_2/Ni-NCs in Si_3N_4/SiO_2" trapping stack was proposed, where Ni-NCs are nickel-nanocrystals. This trapping stack was adopted by considering a higher work function (~5.15 eV) of metallic Ni [10], which can form a deeper energy well to improve data retention and to enhance the coupling effect with the conduction channel to reduce power consumption. In addition, the hetero-interfaces of Ni-NCs in Si_3N_4 matrix may create more trapping centers to trap more carriers than the traditional oxide/nitride/oxide (ONO) stack.

2. Experimental

The structure of Ni-NCs embedded in NVM-TFT device is shown in Fig. 1. Fabrication of the NVM-TFT started from a Si wafer, which was oxidized in a furnace to form a layer of SiO_2 (500 nm) on the surface to simulate a glass substrate, then deposited by low pressure chemical vapor deposition at 550 °C to form amorphous-Si films (100 nm). It was then followed by low temperature (≦600 °C) annealing for 24 h in N_2 atmosphere to transform the amorphous-Si to a poly-Si film. An additional SiO_2 (500 nm) film as the field oxide was deposited by plasma enhanced chemical vapor deposition (PECVD), and subjected to patterning and etching processes for defining active regions. The source and drain regions were implanted with phosphorus (35 keV at 5×10^{15} cm^{-2}) and activated at 600 °C for 24 h under N_2 atmosphere. The SiO_2 (7.5 nm) and Si_3N_4 (3 nm) gate dielectric layers were then deposited on the patterned active regions by PECVD with SiH_4/N_2O (5/90 sccm/sccm) and SiH_4/NH_3 (20/80 sccm/sccm) as the reaction gases, respectively. The stack was then deposited with 4.5 nm Ni thin film by electron-gun evaporation, followed by rapid thermal annealing at 550 °C to form Ni-NCs. The NCs-deposited stack was subsequently embedded in the stack by depositing a Si_3N_4 (12 nm) and then SiO_2 (15 nm) films on the top, using PECVD. The SiO_2 gate oxide quality was further improved by annealing the stack in O_2 at 400 °C for 30 min. The NVM-TFT devices were followed by patterning and etching to open the contact holes. The Al electrodes were finally

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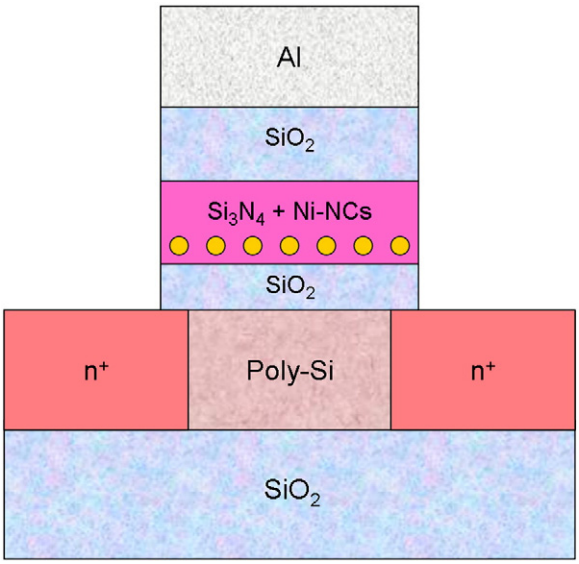

Fig. 1. The schematic cross sectional structure of Ni-NCs embedded in NVM-TFT device.

patterned by depositing a 300 nm Al film, patterning, etching and then sintering at 400 °C in N_2 atmosphere for 30 min. The etching solution for Al electrodes is H_3PO_4:HNO_3:CH_3COOH:H_2O (50:2:10:9). The fabricated devices have a gate area of $10\times100\,\mu m^2$ (length × width). The structures and properties of the stacks after each processing step were characterized by scanning electron microscopy (SEM), transmission electron microscopy (TEM), and current–voltage (I–V) measurements.

3. Results and discussions

Fig. 2(a) shows a top view SEM micrograph of Ni-NCs on the Si_3N_4 surface before embedding into the nitride layer. The NCs were formed by rapid thermal annealing the Ni film (4.5 nm) at 550 °C for 1 min. The corresponding size distribution of NCs is shown in Fig. 2(b). It indicates that the range of diameters and number density of the Ni-NCs are 5–13 nm and 5.3×10^{11} cm^{-2}, respectively. These values are functions of initial Ni thickness, substrate material, annealing temperature and time, as described elsewhere [11]. A thinner film thickness generally results in a smaller particle size.

The cross sectional TEM images of the SiO_2/Ni-NCs in Si_3N_4/SiO_2 dielectric stack and the same stack without Ni-NCs are shown in Fig. 3 (a) and (b), respectively. Darker circular-like particles in Fig. 3(a) are Ni-NCs with sizes ranging from 5–9 nm, which are embedded in the nitride matrix. The thickness of each layer with and without Ni-NCs can be clearly seen in these two figures.

Regarding the current–voltage (I–V) features of the Ni-NCs assisted MONOS-TFT, Fig. 4 shows the drain current versus drain voltage (I_d–V_d) curves across the stack with poly-crystal Si active layer using gate voltages from 0 to 6 V. The drive current density of 0.4 μA/μm^2 at 6 V gate voltage can be reached, which is derived by dividing the current by the gate area of $10\times100\,\mu m^2$ (length × width). It signifies a favorable range for display and integrated circuit applications. Fig. 5 shows the drain current versus gate voltage (I_d–V_g) curves of these devices with and without Ni-NCs, which are electrically programmed and erased with a gate bias of 18 V, 1 s and −18 V, 1 s, respectively. The threshold voltage shift (ΔV_{TH}) of the device with Ni-NCs is about 3.2 V in contrast to 2.0 V for device without NCs. In addition, the on/off current ratios (i.e. maximum value of asymptotic curve divided by the value at the minimum point of each curve under the sweeping voltage range) do not show significant change with or without Ni-NCs in the stack, and can go up to 10^5. The sub-threshold swing (S.S.), calculated from a range close to the maximum slope

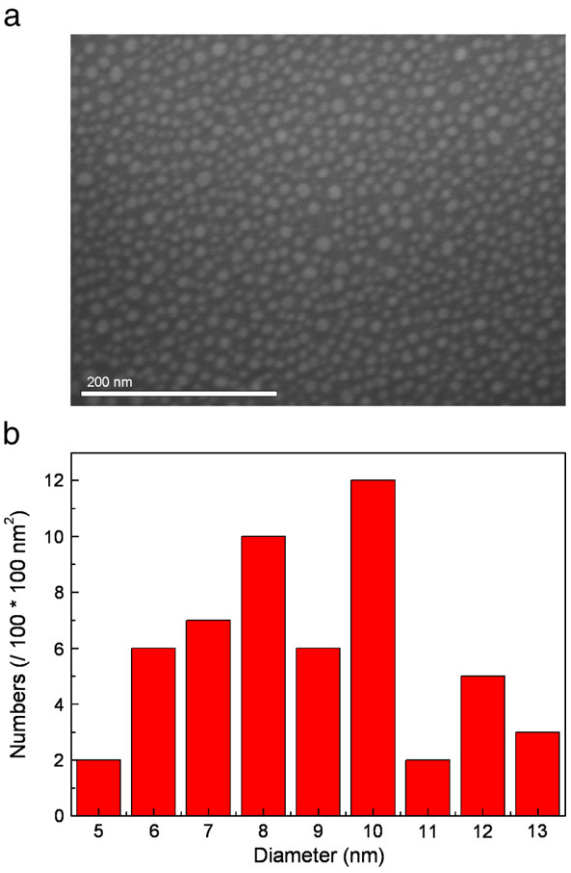

Fig. 2. (a) Top view SEM micrograph of Ni-NCs on Si_3N_4 surface before embedding into nitride layer for Ni film (4.5 nm) treated by rapid thermal annealing at 550 °C for 1 min, and (b) the corresponding size distribution of NCs.

point of each curve, can go down to 1.1–1.4 V variation per decade of current variation in amperes, signifying a quick response and low leakage current in the poly-Si channel. In other words, the ΔV_{TH} of 3.2 V is more than enough memory window to be sensed either "1" or "0" by an amplifier, signifying less operating voltage or less power consumption to pump electrons in and out. A better performance may be due to creating more defects as trapping centers from mismatches of the Ni-NCs and Si_3N_4 interfaces [12–16]. These defects are mainly the dangling bonds in the Ni-NCs/Si_3N_4 interface due to different lattice constants of Ni and Si_3N_4. In addition, the NCs metal might also induce many gap states to be the traps. In summary, the SiO_2/Ni-NCs in Si_3N_4/SiO_2 stack has been successfully demonstrated as able to manipulate the charging and discharging of electrons in the stack for potential applications as NVM devices.

Fig. 6(a) and (b) shows our proposed energy band diagrams to compare the stack under programming condition with and without Ni-NCs in the stack, respectively, which is similar to the reported diagram [17]. In this condition, electrons are injected by the Fowler–Nordheim (F–N) tunneling effect from Si substrate through the tunneling oxide layer into the trapping nitride layer. Each of Ni-NCs can provide an additional deeper energy well to store the electrons for good data retention. The curves of retention time versus threshold voltage for MONOS-TFT under "1" and "0" states, with or without Ni-NCs in the device are shown in Fig. 7. It shows that the devices under the same programming/erasing condition can have a memory window of 2.6 V and 1.7 V up to 10^4 s, with and without Ni-NCs, respectively. In general, the leakage current of a TFT is more serious in the reverse bias region, known as the Frenkel–Poole region, in which the trapped electrons can be more easily tunneled out through defects in the tunnel oxide layer by the Frenkel–Poole mechanism [18]. In

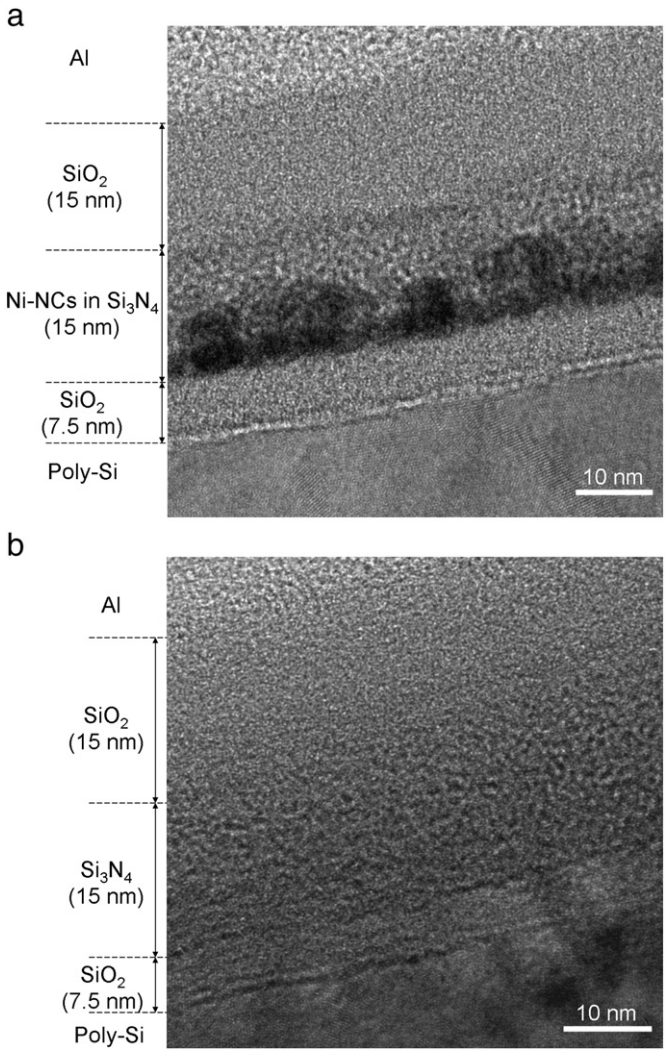

Fig. 3. (a) The cross sectional TEM images of the "SiO_2/Ni-NCs in Si_3N_4/SiO_2" dielectric stack, and (b) the same stack without Ni-NCs.

other words, one of the advantages of storing electrons in the layer of Ni-NCs in the Si_3N_4 matrix is that electrons are stored in many nanocrystals, where most of NCs are insulated from each other to minimize the possibility of tunneling out simultaneously in the reverse bias operation for reading. In summary, the larger initial

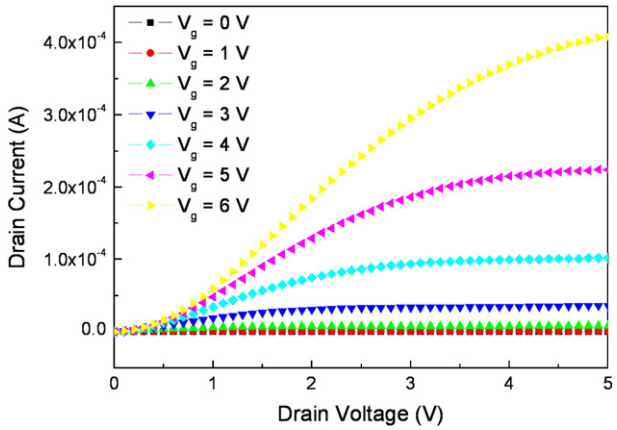

Fig. 4. The drain current versus drain voltage (I_d–V_d) curves across the stack with poly-crystal Si active layer under gate voltages from 0 to 6 V.

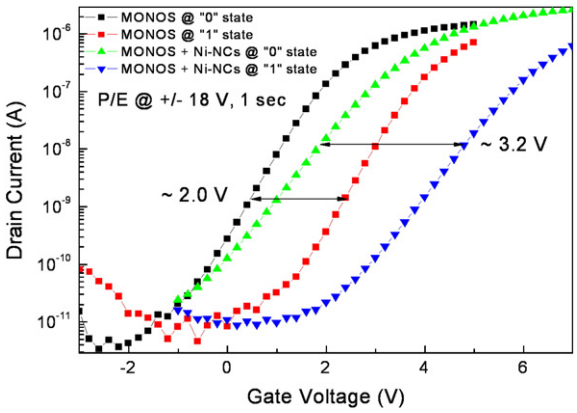

Fig. 5. The drain current versus gate voltage (I_d–V_g) curves of devices with or without Ni-NCs, which are electrically programmed and erased with a gate bias of 18 V, 1 s and −18 V, 1 s, respectively.

memory window for the stack with the layer of Ni-NCs in Si_3N_4 matrix provides a good starting point to store more electrons for each data state to delay data loss, and the high work function (~5.15 eV) of Ni-NCs offer a deep energy well for storage of electrons to minimize data loss and to achieve good data retention.

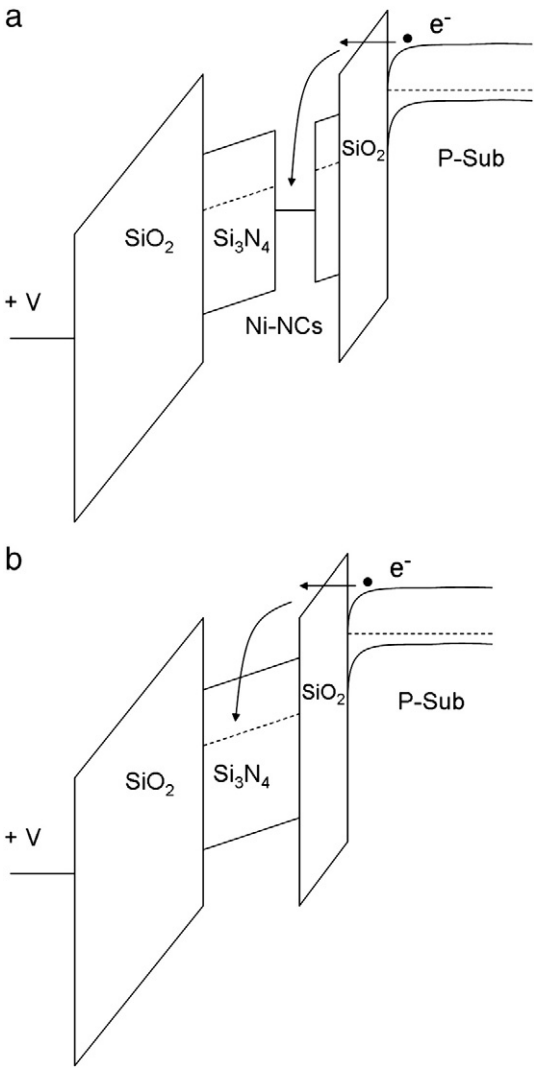

Fig. 6. (a) and (b) showing our proposed energy band diagrams to compare the stack under programming condition with and without Ni-NCs in the stack, respectively.

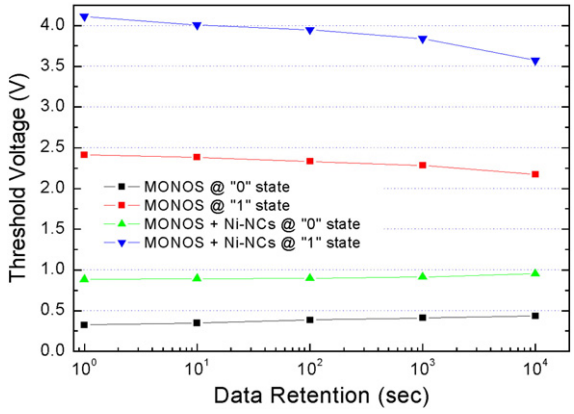

Fig. 7. The curves of retention time versus the threshold voltage for MONOS-TFT under "1" and "0" states, with and without Ni-NCs in the device.

4. Conclusions

In this work, the Ni-NCs assisted LTPS-MONOS-TFT devices were fabricated and their performance demonstrated. Our proposed "Al/SiO_2/Ni-NCs in Si_3N_4/SiO_2/Si" stack devices provide the following advantages over the traditional "oxide/nitride/oxide" stack devices. The Ni-NCs provide more trapping centers for storing more electrons, and cause larger V_{TH} shifts or memory windows to enhance data state recognition and to delay data loss. The higher work function of Ni-NCs can create an additional energy well for each NC to minimize electron loss and improve data retention. It can be concluded that the Ni-NCs-assisted NVM-TFT devices were successfully fabricated on SiO_2 substrate to simulate its potential applications on glass panels and to extend the possibilities of applications in SOP, 3-D stacked NVM, and OLEDs.

Acknowledgments

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