The Zero-Temperature-Coefficient Point Modeling of DTMOS in CMOS Integration

Kuan-Ti Wang, Wan-Chyi Lin, and Tien-Sheng Chao

***Abstract*—For the first time, analytical expressions of zero-temperature-coefficient (ZTC) point modeling of DTMOS transistor are successfully presented in detail. New analytical formulations for the linear and saturation regions of DTMOS transistor operation that make certain the drive current to be temperature independent for the ideal gate voltage are developed. The maximum errors of 0.87% and 2.35% in the linear and saturation regions, respectively, confirm a good agreement between our DTMOS ZTC point model and the experimental data. Compared to conventional MOSFET, the lower V_g (ZTC) with higher overdrive current of DTMOS improves the integrated circuit speed and efficiency for the low-power-consumption concept in green CMOS technology.**

***Index Terms*—DTMOS, modeling, strain, zero temperature coefficient (ZTC).**

I. Introduction

RECENTLY, the idea of attaining high performance with low power consumption by using dynamic threshold (DT) technique [1] applications has become popular in the development of a number of MOS technologies, including 6T-SRAM, RFID circuit, multiplier, and low-voltage analog circuit [2]–[4]. However, the DT technique operated at elevated temperature should seriously degrade the performance, caused by the phonon scattering, which results in some of the reference circuit failures. To solve these unstable temperature problems, the zero-temperature-coefficient (ZTC) point, which is an important parameter for stable CMOS integrated circuit work over an operated temperature, is applied [5]. In this letter, the ZTC design criterion for a stable integrated circuit under consideration of elevated temperature DT operation means that to drive circuits at an optimal gate voltage with temperature independence is desired. Based on these concepts [5], [6], for the first time, we derived and verified the ZTC point model of a DTMOS transistor for operations at typical room temperatures to military range (25 °C–125 °C).

II. DTMOS ZTC Modeling

Fig. 1 shows the I_d-V_g characteristics of DTMOS transistor with ZTC. In order to accurately express the ZTC point analytical solutions for DTMOS, employing an appropriate analytical drain current model is important. As a result, our DTMOS ZTC point theory is based on the simple and accurate charge sheet approximation of the MOSFET drain current model with depletion approximation which considers both the linear and saturation regions by simultaneously including the channel potential and body effect [7]. For DTMOS, the drain current expressions may be expressed as follows:

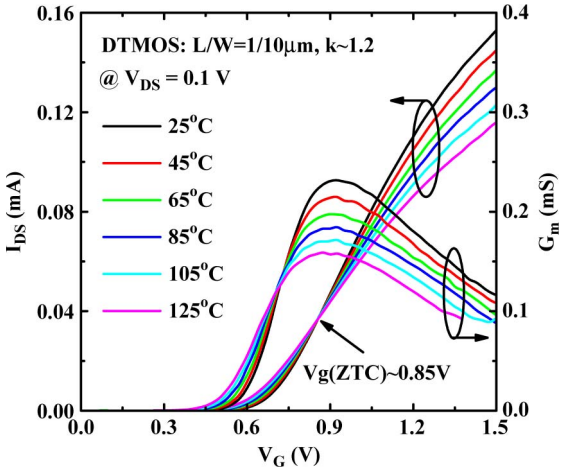

Fig. 1. Experimental I_d-V_g and G_m characteristics of n-channel DTMOS in the linear region over a temperature range of 25 °C–125 °C. Note that the ZTC point is 0.85 V when $V_{\rm DS} = 0.1$ V in the linear region.

Linear region:

$$I_{\rm DS} = \frac{W}{L} C_{\rm ox} \mu_n \left\{ \left(V_G - V_T(V_{\rm BS}) \right) V_{\rm DS} - \frac{m}{2} V_{\rm DS}^2 \right\} \quad (1)$$

Saturation region:

$$I_{\rm DS} = \frac{W}{L} C_{\rm ox} \mu_n \frac{\left(V_G - V_T(V_{\rm BS}) \right)^2}{m} \quad (2)$$

where

$$m = 1 + \delta \quad (3)$$

$$\delta = -\frac{dV_T}{dV_{\rm BS}} = \frac{1}{C_{\rm ox}} \sqrt{\frac{q \varepsilon_{\rm Si} N_a}{2(2\phi_{\rm fp} - V_{\rm BS})}} \quad (4)$$

m is the body effect coefficient, $C_{\rm ox}$ is the gate oxide capacitance per unit area, μ_n is the effective channel mobility, uniform channel doping N_a is assumed, and W and L are the channel width and length, respectively. It should be noted that, because the DTMOS transistors are operated by connecting the gate with the substrate, the substrate bias may thus be given as

$$V_{\rm BS} = \alpha V_G \quad (0 \le \alpha \le 1). \quad (5)$$

Manuscript received May 30, 2010; revised June 24, 2010; accepted June 26, 2010. Date of publication August 5, 2010; date of current version September 24, 2010. This work was supported by the National Science Council, Taiwan, under Contract NSC-97-2221-E-009-153-MY3. The review of this letter was arranged by Editor X. Zhou.

The authors are with the Department of Electrophysics, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: tschao@mail.nctu.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2010.2057404

The α is defined as a constant ratio of the dynamical biases between the gate and the substrate. Due to the limitation of $V_{\rm BS} < 0.7$ V under DT mode, the validation range of α is also defined in (5). Devices operated under normal and DT modes, while the $\alpha = 0$ and $\alpha > 0$, respectively. In our experiment, $\alpha = 0.4$ is used to validate the ZTC model accuracy of DTMOS.

Furthermore, the effective mobility dependence on operation temperature, for an ideal MOS transistor, is usually given as

$$\mu_n(T) = \mu_n(T_i)\left(\frac{T}{T_i}\right)^{-K_1} \tag{6}$$

where T_i is the initial room absolute temperature and K_1 is the corresponding constant, smaller than the previous reports; K_1 is 1.2 in our DTMOS transistor, which is extracted from the transconductance degradation of ZTC point at elevated operation temperature, as shown in Fig. 1. By using the method, the mobility variations of DTMOS caused by the threshold voltage decrease with different temperature have also been included.

In this letter, V_t is extracted by the linear extrapolation method [8], [9]. The assumptions of V_t dependence on temperature and body bias are modeled simultaneously in the following approximate expressions:

$$V_T(T, V_{\rm BS}) \cong p_0 T + r_0 V_{\rm BS} + q_0 \tag{7}$$

where

$$p_0 = \left.\frac{dV_T}{dT}\right|_{T_i \sim T_f, V_{\rm BS} < 0.6\ \rm V} \tag{8}$$

$$r_0 = \left.\frac{(V_T(T, V_{\rm BS}) - q_0 - p_0 T)}{V_{\rm BS}}\right|_{T_i \sim T_f, V_{\rm BS} < 0.6\ \rm V} \tag{9}$$

$$q_0 = V_T(T_i, V_{\rm BS}) - r_0 V_{\rm BS} - T_i \left.\frac{dV_T}{dT}\right|_{T = T_i, V_{\rm BS} < 0.6\ \rm V}. \tag{10}$$

The p_0, q_0, and r_0 are the average values extracted from the experimental data. Furthermore, the temperature dependence of the body effect coefficient may be approximated by

$$m = 1 + \delta \cong 1 + sT + t \tag{11}$$

where

$$s = \left.\frac{d\delta}{dT}\right|_{T_i \sim T_f} \tag{12}$$

$$t = \delta(T_i) - T_i \left.\frac{d\delta}{dT}\right|_{T = T_i}. \tag{13}$$

The detailed physical expressions of dV_T/dT and $d\delta/dT$ may also be found in [7].

After deriving the initial definition of $dI_{\rm DS}/dT = 0$ under the DTMOS ZTC model, by substituting the assumptions described by (5)–(13) into the results and using the least square method to ensure drain current independence over the temperature range T_i to T_f [5], consequently, by solving the equations, we propose the following formulations for the linear and saturation regions of the ZTC point model of the DTMOS transistor:

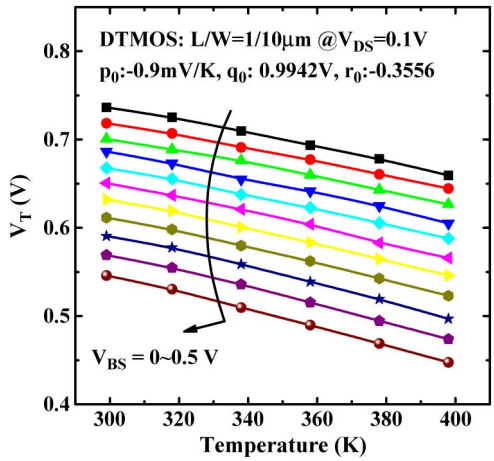

Fig. 2. Temperature dependence of the threshold voltage with different body biases at elevated temperatures from 298 to 398 K.

Linear region:

$$V_G(\rm ZTC) = \frac{\left(p_0 + \frac{sV_{\rm DS}}{2}\right)\left(1 - \frac{1}{K_1}\right)(T_i + T_f) + V_{\rm DS}(1+t) + 2q_0}{2(1 - \alpha r_0)} \tag{14a}$$

Saturation region:

$$V_G(\rm ZTC) = \frac{p_0\left(\frac{K_1 - 1}{K_1 + 1}\right)(T_i + T_f) + 2q_0 - \frac{p_0 T_\delta}{K_1}\left(\frac{4}{K_1 + 1}\right)\left[1 - \frac{T_\delta}{(T_f - T_i)}\ln\left(\frac{T_f + T_\delta}{T_i + T_\delta}\right)\right]}{2(1 - \alpha r_0)} \tag{14b}$$

where

$$T_\delta = \frac{K_1(1+t)}{s(1+K_1)}. \tag{15}$$

III. Modeling Validation

The proposed model is verified using the experimental data obtained from our DTMOS device in which channel length and width is 1 and 10 μm, respectively. Fig. 2 shows the threshold voltage dependences on the temperature from 25 °C to 125 °C with different body biases. The physical parameters p_0, q_0, and r_0 of the ZTC point model for DTMOS can be extracted easily from our model. In general, the threshold voltage decrease with increasing body bias can be considered a continued reduction of the depletion region in DTMOS, as shown in Fig. 3. The straight black line shows that the body bias varies dynamically with gate bias, and the crossover point shows a gradual reduction in threshold voltage, due to the increase in n_i with increasing operating temperature.

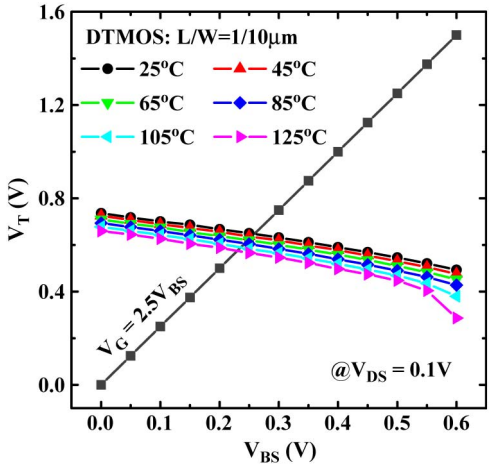

Fig. 3. Body bias dependence of the threshold voltage at elevated temperatures from 298 to 398 K. The straight black line shows that the body bias varies dynamically with the gate bias.

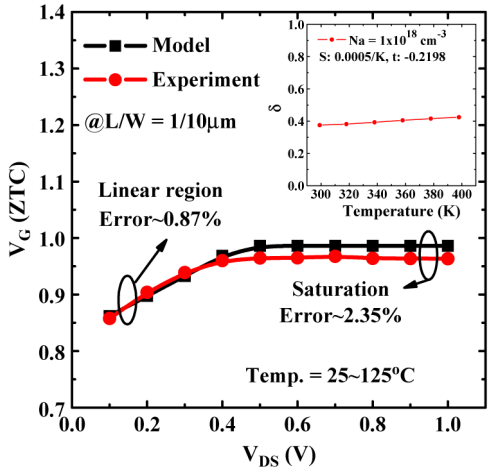

Fig. 4. Theoretical values of the ZTC point model and actual experimental data of the DTMOS transistor in both the linear and saturation regions. The inset figure shows the temperature dependence of the body effect coefficient over the temperature range from 298 to 398 K.

The predicted values of the ZTC point model and the experimental data from the DTMOS transistor in both the linear and saturation regions are shown in Fig. 4. The inset in Fig. 4 shows the temperature dependence of the body effect coefficient over the temperature range of 298–398 K. The characteristic features s_0 and t_0 in our ZTC point model of DTMOS are extracted from the slope and extrapolated point of a body effect coefficient versus absolute temperature curve, simultaneously. The channel doping is 10^{18} cm^{-3} in our device. Estimations of the disagreement between the DTMOS ZTC model and the experimental data, roughly 0.87% in the linear region and 2.35% in the saturation region, are obtained. Our proposed model gives results that are sufficiently accurate to predict the ZTC behaviors of DTMOS.

IV. Conclusion

Analytical expressions of the ZTC point modeling of DTMOS transistor have been successfully presented in detail. The maximum errors of 0.87% and 2.35% in the linear and saturation regions, respectively, confirm the good agreement between our DTMOS ZTC point model and the experimental data. The proposed formulations are useful for future integrated circuit design using DT technology.

Acknowledgment

The authors would like to thank the National Nano Device Laboratories and the Nano Facility Center of the National Chiao Tung University for the process support.

References

[1] Z. Yan, M. J. Deen, and D. S. Malhi, "Gate-controlled lateral PNP BJT: Characteristics, modeling and circuit applications," *IEEE Trans. Electron Devices*, vol. 44, no. 1, pp. 118–128, Jan. 1997.

[2] M. E. Hwang and K. Roy, "A 135 mV 0.13 μW process tolerant 6 T subthreshold DTMOS SRAM in 90 nm technology," in *Proc. IEEE CICC*, Sep. 2008, pp. 419–422.

[3] F. Mohd-Yasin, Y. K. Teh, M. B. I. Reaz, and A. Kordesch, "Developing designs for RFID transponder using DTMOS," *Microw. RF*, vol. 46, no. 4, pp. 70–80, Apr. 2007.

[4] M. Maymandi-Nejad and M. Sachdev, "DTMOS technique for low-voltage analog circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 10, pp. 1151–1156, Oct. 2006.

[5] F. Shoucair, W. Hwang, and P. Jain, "Electrical characteristics of large scale integration (LSI) MOSFETs at very high temperature," *Microelectron. Reliab.*, vol. 24, no. 3, pp. 465–485, 1984.

[6] Z. D. Prijic, S. S. Dimitrijev, and N. D. Stojadinovic, "The determination of zero temperature coefficient point in CMOS transistors," *Microelectron. Reliab.*, vol. 32, no. 6, pp. 769–773, Jun. 1992.

[7] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 2009.

[8] M. J. Deen and Z. Yan, "A new method of measuring the threshold voltage for small geometry MOSFETs from subthreshold conduction," *Solid State Electron.*, vol. 33, no. 5, pp. 503–511, May 1990.

[9] D. K. Schroder, *Semiconductor Material and Device Characterization.*, 3rd ed. New York: Wiley-Interscience, 2005.