A 60 GHz Injection-Locked Frequency Tripler With Spur Suppression

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***Abstract*—A 60 GHz injection-locked frequency tripler is designed to improve spectral purity with spur suppression of the fundamental and the even-order harmonics. Several circuit designs are utilized in the harmonic current injection circuit to maximize the third-order harmonic and minimize the undesired harmonic current outputs, including notch filters and a capacitive cross-coupled transistor pair. With the input signal of 0.5 dBm at 19.7 GHz, the harmonic rejection ratios of the fundamental, and the second-order achieve 31.3 dBc, and 45.8 dBc, respectively. Implemented in 0.13 μm CMOS technology, the core circuit consumes power of 9.96 mW with 1.2 V supply voltage. The entire die occupies an area of 985 $\times$ 866 μm^2**

***Index Terms*—Capacitive cross-coupling, frequency tripler, injection-locking, notch filter.**

I. Introduction

INJECTION locking has been found useful in RF integrated circuit design. One interesting application is the frequency tripler circuit for LO signal generation in 60 GHz millimeter-wave transceivers [1]–[3]. At such a high frequency, the conventional tripler with a nonlinear device or a hard-limiter generates the third-order harmonic output in a power-hungry manner. The injection-locking approach is an extension to allow a large output voltage assisted by an oscillator such that frequency tripling comes efficiently in power consumption. The oscillator tank is chosen with a low Q-value to enlarge the locking frequency range, namely, the operation range.

A critical issue of the injection-locked tripler is spectral purity. To LO signals, spurious noise is required as low as possible to avoid any undesired frequency conversion of interferers. The typical injection node is often directly at the oscillator output nodes [1], [2], [4]. Although oscillator locking is limited to the third-order harmonic frequency range, undesired spurious noise from the harmonic generator still directly feeds through and appears at the output. Suppression is insufficient by the low-Q oscillator tank. It is typical to apply additional external filtering. In this work, circuit design is aimed at spur rejection by several techniques, and verified with a 60 GHz tripler in 0.13 μm RF CMOS technology.

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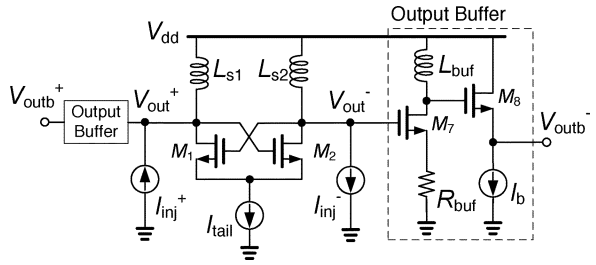

Fig. 1. Injection-locked frequency tripler, including the output buffers for measurements. The differential harmonic injection circuit $\mathrm{I_{inj}}$ is shown in Fig. 2.

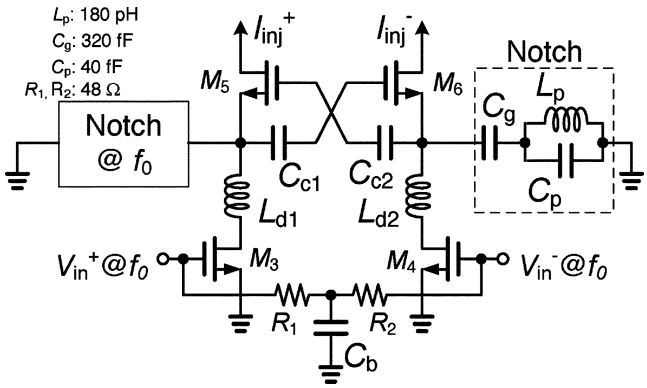

Fig. 2. Differential harmonic injection circuit with spur suppression.

II. Tripler Design

The injection-locked frequency tripler in this work is shown in Fig. 1. It consists of an oscillator and a differential harmonic current injection circuit. The oscillator is designed at the frequency around three times the input frequency $3f_0$ using the typical configuration of a cross-coupled pair, M_1 and M_2. Together with parasitic capacitance at the transistor drain ports, the inductors L_{s1} and L_{s2} form the resonator without frequency control in this work. The third-order harmonic frequency locks the oscillator and turns it to a tripler. The locking range is determined by the magnitude of third-order harmonic injection current and the Q-value of the LC tank [4].

The spur issue can be alleviated by the proposed differential harmonic injection circuit as shown in Fig. 2. Instead of using an external filter at the oscillator output, spurious noise is suppressed before injecting into the oscillator. Several circuit designs are utilized. They include a harmonic generator (M_3 and M_4) with inductive load (L_{s1} and L_{s2}) for the third-order harmonic enhancement, a capacitive cross-coupled pair (M_5 and M_6) for the even-order harmonic rejection, and a notch filter for the fundamental suppression. The design goal is a large harmonic rejection ratio (HRR), defined as

$$\mathrm{HRR_n} = 20\log\left(\left|\frac{3^{\mathrm{rd}}\text{-order harmonic output}}{\mathrm{n^{th}}\text{-order harmonic output}}\right|\right) \quad (1)$$

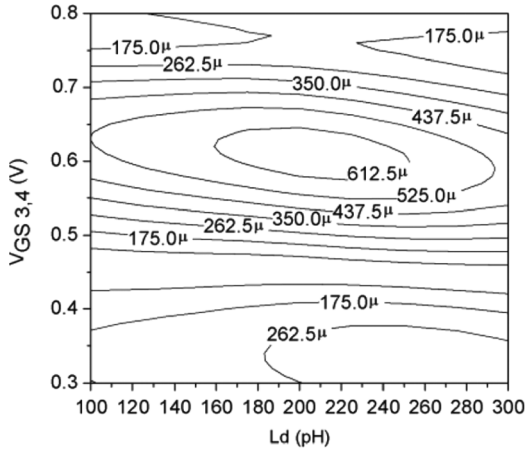

Fig. 3. Contour plot of the generated third-order harmonic current for analysis of the optimal bias voltage and the drain load inductance.

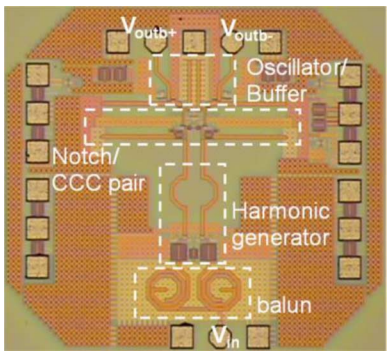

Fig. 4. Micrograph of the fabricated frequency tripler.

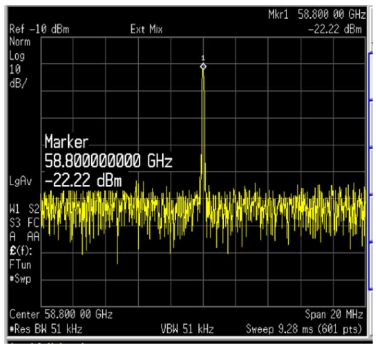

Fig. 5. Output spectrum under the injection locked condition.

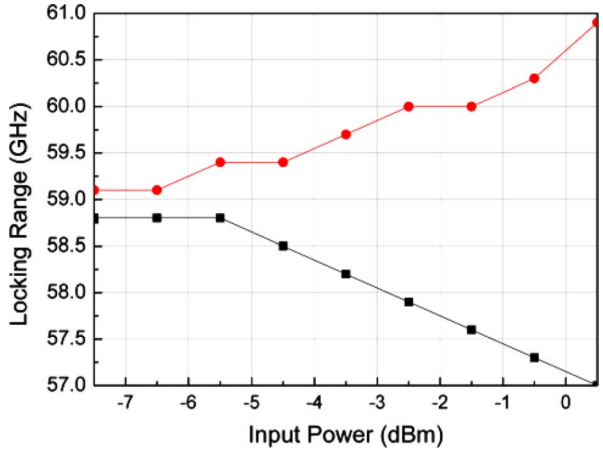

Fig. 6. Measured frequency locking range of the tripler.

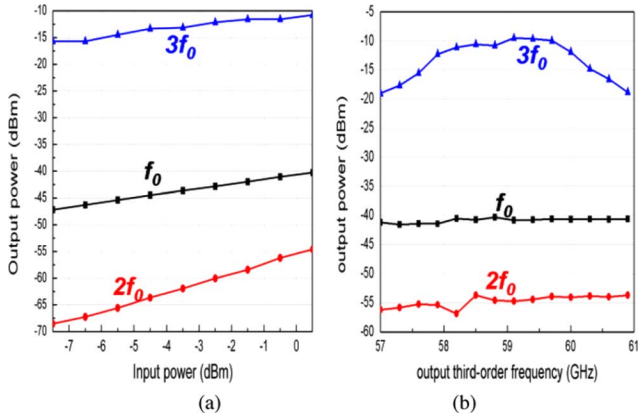

Fig. 7. Measured harmonic output power levels after calibration of the cable loss over (a) different chip input power at the input frequency f_o of 19.6 GHz, and (b) the frequency range of interest with the input power of 0.5 dBm.

TABLE I
DEVICE WIDTH AND MEASURED BIAS CURRENT

Device	Width	Current
M_1, M_2	14 × 2μm	5.89 mA (M_1+M_2)
M_3, M_4	14 × 2.8μm	2.41 mA (M_3+M_4)
M_5, M_6	14 × 1.2μm	2.41 mA (M_5+M_6)
M_7	12 × 1.2μm	Total devices of buffer consume 13.41 mA.
M_8	12 × 1.4μm	

Note: The minimum channel length of 0.13 μm is applied to all devices.

where n refers to the n$^{\text{th}}$-order harmonic.

M_3 and M_4 generate all harmonic currents of the fundamental signal at the frequency f_0. The loading impedance was suggested in [5] to be as low, low, and high at the frequency of f_0, $2f_0$ and $3f_0$, respectively, to enhance the third-order output current. $L_{\text{d1,2}}$ are, therefore, placed to result in high-impedance resonance at $3f_0$ to meet this condition. Also the gate bias voltage, V_{GS}, affects the third-order nonlinearity. The optimal bias voltage $V_{\text{GS3,4}}$ and the load inductance, $L_{\text{d1,2}}$, are determined by using the contour plot in Fig. 3. With V_{GS} of 0.6 V and L_d of 200 pH, the third-order harmonic output current achieves 612.5 μA.

The cascade configuration of M_5 and M_6 buffers the harmonic generator and relaxes the loading condition to the oscillator tank. dc current is re-used with M_3 and M_4. Since the even-order harmonic output currents from M_3 and M_4 are in phase as a common-mode response, the capacitive cross-coupling effectively rejects them all [6]. Table I lists the device sizes and the measured bias current.

The notch filter consists of L_{p}, C_{p}, and C_{g}. Connected in shunt to the signal path, it bypasses the fundamental spur with low input impedance at f_0, and sustains the third-order harmonic injection current with high impedance at $3f_0$. Its input impedance is derived as

$$Z_{\text{N}} = \frac{1 + s^2 L_p (C_p + C_g)}{s(1 + s^2 L_p C_p) C_g} \tag{2}$$

which carries out a zero frequency at

$$f_{\text{z}} = \frac{1}{\sqrt{L_p (C_p + C_g)}} \tag{3}$$

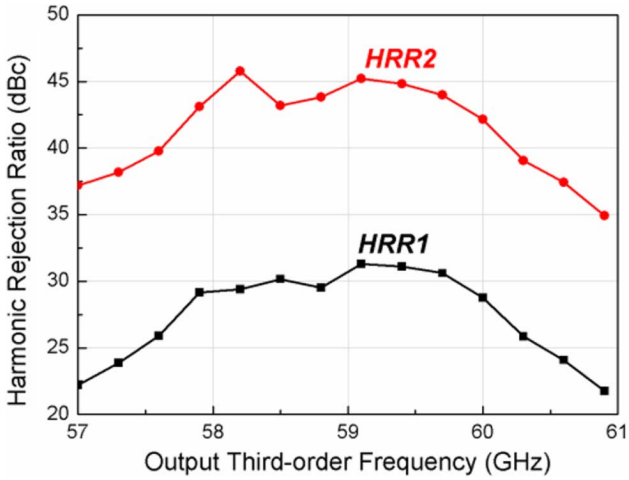

Fig. 8. Calculated harmonic rejection ratios of the tripler.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

Ref.	This Work	[1]	[2]	[3]
Technology	CMOS 130 nm	CMOS 90 nm	CMOS 90 nm	CMOS 130 nm
Free-running frequency	58.92 GHz	60.61 GHz	29.3 GHz	60.025 GHz
Locking range	3.9 GHz	8 GHz	2.6 GHz	1.1 GHz
f_{in}	19.7 GHz	20.2 GHz	9.7 GHz	20.008 GHz
P_{in}/P_{out} (dBm)	0.5 /-9.47	0 /-27.26	5 /-14.83	4 /-5.21
HRR1	31.3 dBc	N/A	<20 dBc	N/A
HRR2	45.8 dBc	N/A	<20 dBc	N/A
$P_{dc,core}$	9.96 mW	9.6 mW	4 mW	1.86 mW
Chip size (μm^2)	985 x 866	950 x 850	240 x 150 (core)	590 x 660

and a pole frequency at

$$f_{\rm p} = \frac{1}{\sqrt{L_p C_p}}. \tag{4}$$

As such, $L_{\rm p}$, $C_{\rm p}$, and $C_{\rm g}$ are selected to result in f_z at f_0 and f_p at $3f_0$.

A two-stage differential output buffer is employed for the measurement purpose. Only one side of the buffer is shown in the dashed box in Fig. 1. For a minimum loading effect on the oscillator, a common-source stage with a small device size is adopted at the first stage. A source follower stage is used to drive 50 Ω impendence at the second stage.

III. Measurement Results

The tripler circuit is designed and fabricated in 0.13 μm CMOS technology. The die micrograph is shown in Fig. 4, occupying an area of 985×866 μm ^{2}, including an on-chip balun placed at the input to provide a differential input signal to the harmonic generator. The measured input return loss of the entire chip is better than 10 dB from 18 to 22 GHz. The circuit is characterized single-ended at one output while the other output is terminated into 50 Ω load. The signal loss due to the cable setup is around 11.3 dB. The output signal spectrum is observed on a spectrum analyzer equipped with the option of an external harmonic down-converter, which conversion loss is calibrated automatically by the spectrum analyzer itself.

The measured free-running frequency of the oscillator is at 58.92 GHz, with an output power level of -27.14 dBm without calibration of the cable loss. Fig. 5 shows the measured output spectrum under the injection locked condition with a chip input signal of 0.5 dBm at 19.6 GHz. The frequency locking range increases as the input power increases. As shown in Fig. 6, the locking range achieves 3.9 GHz at the input power of 0.5 dBm.

The measured harmonic output power after calibration of the cable loss is shown in Fig. 7, over different input power levels and the frequency range of interest. It also demonstrates successful broadband suppression of the undesired fundamental and the second-order harmonic such that those output power levels appear to be flat across the entire band. The maximum conversion gain of -10 dB occurs at the input frequency of 19.7 GHz. The output 3 dB bandwidth is about 2.18 GHz. Fig. 8 shows the calculated harmonic rejection ratios of two major harmonic outputs. The HRRs of the fundamental and the second-order with the input signal at 19.7 GHz are 31.3 and 45.8 dBc, respectively. The phase noise is measured with a signal source analyzer using an input signal at 19.65 GHz. The data shows an increase around 10 dB at the injection-locked output, in agreement with the theoretical value of 9.5 dB.

With the input power of 0.5 dBm, the core circuit and the output buffer under operation consume dc power of 9.96 and 16.1 mW, respectively, with 1.2 V supply voltage. The circuit performance of this tripler is summarized in Table II, together with those of other works for comparison. It shows that the harmonic rejection of the proposed tripler is superior to the others.

IV. Conclusion

Spur suppression is implemented and verified in a 60 GHz frequency tripler utilizing the injection locking approach. Not much mentioned in other literatures, the spurious noise issue is greatly alleviated in the proposed circuit without using any external filtering. The circuit offers rejection better than 31 and 45 dB to the fundamental and the second-order harmonic spurious noise, respectively.

References

[1] W. K. Chan and J. R. Long, "A 56–65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2739–2746, Dec. 2008.

[2] S.-W. Tam, E. Socher, A. Wong, Y. Wang, L. D. Vu, and M.-C. F. Chang, "Simultaneous sub-harmonic injection-locked mm-wave frequency generators for multi-band communications in CMOS," in *IEEE RFIC Symp. Dig*, Jun. 2008, pp. 131–134.

[3] M.-C. Chen and C.-Y. Wu, "Design and analysis of CMOS sub-harmonic injection-locked frequency triplers," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 8, pp. 1869–1878, Aug. 2008.

[4] B. Razavi, "A study of injection locking and pulling in oscillator," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[5] J. E. Johnson, G. R. Branner, and J.-P. Mima, "Design and optimization of large conversion gain active microwave frequency triplers," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 7, pp. 457–459, Jul. 2005.

[6] M.-C. Kuo, S.-W. Kao, C.-H. Chen, T.-S. Hung, Y.-S. Shih, T.-Y. Yang, and C.-N. Kuo, "A 1.2 V 114 mW dual-band direct-conversion DVB-H tuner in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 950–961, Mar. 2009.