Low-power VCO with phase-noise improvement in 0.18 μm CMOS technology

C.-P. Liang, T.-J. Huang, P.-Z. Rao and S.-J. Chung

A low-power 5.25 GHz voltage-controlled oscillator (VCO) with phase-noise improvement is designed in a 0.18 μm CMOS 1P6M process. Owing to the use of a larger value of parallel capacitor, an additional harmonic-suppressed capacitor, and an appropriate bulk bias voltage of transistor, a good figure of merit of −190 dBc/Hz can be achieved without extra chip area and CMOS process steps. The fabricated VCO operates from 5.12 to 5.36 GHz with a core power consumption of 1.9 mW and active chip area of 0.15 mm^2. The measured phase noise at 1 MHz offset is about −119 dBc/Hz.

Introduction: Phase noise is one of the most critical parameters since it affects the overall performance of a communication system; therefore, there are numerous attempts in the design of VCOs to optimise phase-noise performance. The harmonic tuned LC tank is employed to attenuate the second-harmonic power while maintaining a superior fundamental power, which is of benefit in making the output voltage waveform steeper for reducing flicker noise of the transistor [1]. Phase-noise suppression is achieved by maximising the slope of the output voltage at the zero crossing point. However, it inevitably results in high implementation cost because additional on-chip inductors are required. On the other hand, inductively coupled plasma (ICP) deep-trench technology, which selectively removes the silicon underneath the inductors, also can be utilised to improve the phase noise of a VCO [2]. Nevertheless, the extra CMOS process steps will increase the complication of the circuit implementation.

In this Letter, we adopt the design of a current-reused configuration because of its excellent low-power characteristic [3], and focus on improvement of phase-noise performances without additional chip area and CMOS process steps. By a larger parallel capacitor, an extra harmonic-rejected capacitor, and an appropriate bulk bias voltage of transistor, a good figure of merit (FOM) of −190 dBc/Hz will be attained.

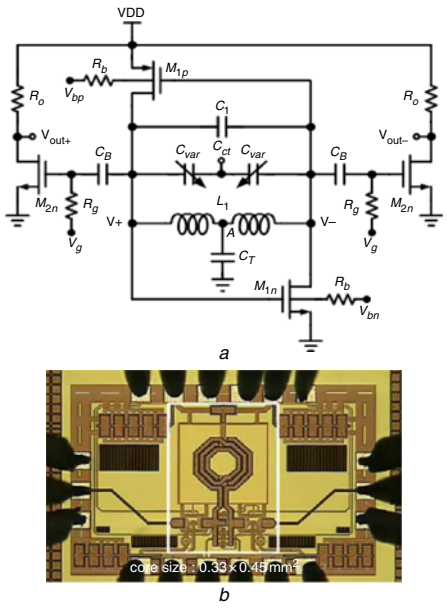

Fig. 1 *Complete schematic and die microphotograph of proposed VCO with phase-noise reduction techniques*

a Complete schematic
b Die microphotograph

Circuit design: The proposed VCO, shown in Fig. 1, uses a cross-connected pair consisting of NMOS and PMOS transistors as a negative conductance generator. Power consumption and the use of inductors can be cut by half compared to the traditional VCO while providing the same negative conductance [3]. However, an unbalanced voltage swing at node V_+ will deteriorate the phase-noise performance when V_+ changes between high and low statuses. To improve this drawback, a larger value of the capacitor C_1 is required to maintain the similar impedances in both operation statuses. It can be observed from Fig. 2 that a larger capacitor C_1 effectively provides a balanced voltage swing at node V_+. On the other hand, the suppression of the second-harmonic power with the series *L-C* sections has been utilised to improve the phase noise of a VCO [1]; however, the extra inductors will occupy additional chip area. In this study, we introduce an additional capacitor C_T in the VCO circuit (Fig. 1) to attenuate the second-harmonic signal. To begin with, it can be anticipated that node A is a virtual ground owing to the differential outputs of the fundamental signal, and this means that the existence of the capacitor C_T will have no influence on the oscillation frequency. However, the in-phase second-harmonic signals can be suppressed by the use of a suitable capacitor C_T because a series resonance is produced. Consequently, the introduction of the suitably designed capacitor C_T can diminish the second-harmonic signal without increasing chip area and influencing the oscillation frequency.

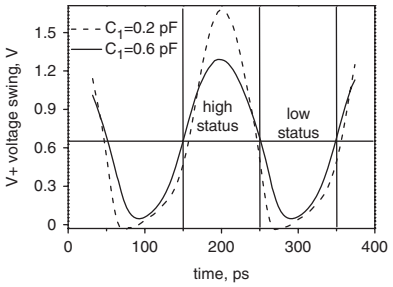

Fig. 2 *Simulated V_+ voltage swing for different values of C_1*

Moreover, the $1/f^3$ corner in the phase noise spectrum can be given from [4]

$$\omega_{1/f^3} \simeq \omega_{1/f}\left(\frac{c_0}{c_1}\right)^2 = \frac{K}{C_{0x}WL}\frac{g_m^2}{\gamma g_{d0}}\frac{1}{4kT}\left(\frac{c_0}{c_1}\right)^2 \quad (1)$$

where $\omega_{1/f}$ is the corner of the transistor $1/f$ noise and c_0 and c_1 represent the first and second Fourier series coefficients of the impulse sensitivity function (ISF). From (1), the $1/f^3$ corner of the phase noise spectrum can be reduced by selecting a larger channel width W; however, this will indirectly increase the value of the transconductance g_m, which is proportional to the size of the transistor. To overcome this drawback, here we introduce the additional bulk bias voltages V_{bp} and V_{bn} of the transistors, as shown in Fig. 1, for further obtaining a smaller g_m. By providing an appropriate bulk bias voltage, the threshold voltage can effectively be raised to diminish the current of the transistor since the threshold voltage is governed with the body effect. Fig. 3 shows the simulated results of the phase noise characteristics with and without improvement. It can be observed and demonstrated that a 15 dB decrease at 10 kHz offset frequency can be attained owing to the use of a larger capacitor C_1, an extra capacitor C_T, and the appropriate bulk bias voltage V_b.

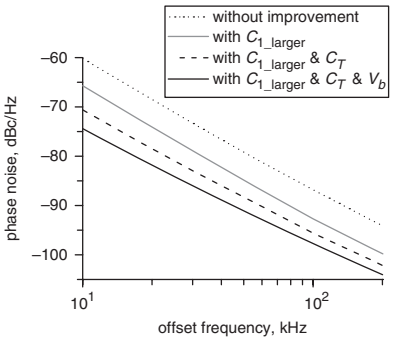

Fig. 3 *Simulated phase noises with and without improvement*

Results: The microphotograph of the low-power VCO fabricated by 0.18 μm TSMC CMOS process is shown in Fig. 1*b*. The core chip area is 0.33 × 0.45 mm^2, and the core DC power dissipation is 1.9 mW at a 1.3 V supply voltage. The value of R_o in the proposed VCO is set as 50 Ω to achieve the output match for testing purposes. The fabricated VCO is measured with an Agilent E5052A signal

source analyser. The measured tuning range is from 5.12 to 5.36 GHz when the tuning voltage V_{ct} is between 0 and 1.3 V. The measured phase noise, as shown in Fig. 4, is about −119 dBc/Hz at 1 MHz offset frequency with the centre frequency at 5.14 GHz and an output power of −2.4 dBm. The proposed VCO performance is compared with recently published CMOS VCOs and summarised in Table 1 [5–7].

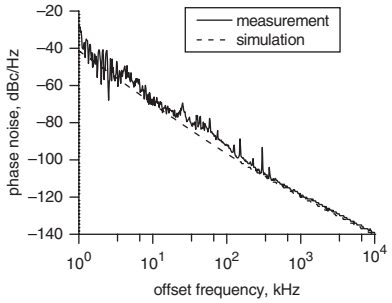

Fig. 4 *Measured and simulated phase noises of proposed VCO*

Table 1: Comparison with previous works

Ref.	Technique	Frequency (GHz)	PN at 1Mz (dBc/Hz)	P_{diss} (mW)	Area (mm^2)	FOM (dBc/Hz)
[5]	0.18 μm CMOS	4.5	−122.5	6.75	0.55	−187
[6]	0.18 μm CMOS	5.1	−116.7	3.9	0.5	−185
[7]	0.18 μm CMOS	5.6	−110.8	8.3	0.5	−177
This work	0.18 μm CMOS	5.25	−119	1.9	0.15	−190

Conclusions: A low-power VCO with phase noise improvement has been designed and fabricated using 0.18 μm CMOS technology. Based on the current reused configuration, a larger value of capacitor C_1, an additional capacitor C_T, and the appropriate bulk bias voltage V_b of the transistor are adopted to achieve a better noise performance. The measured results of the proposed VCO agree quite well with the simulated results.

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One or more of the Figures in this Letter are available in colour online.

C.-P. Liang, T.-J. Huang, P.-Z. Rao and S.-J. Chung (*Institute of Communications Engineering, National Chiao Tung University, Hsinchu 300, Taiwan*)

E-mail: sjchung@cm.nctu.edu.tw

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