A Fully Integrated Built-In Self-Test $\Sigma-\Delta$ ADC Based on the Modified Controlled Sine-Wave Fitting Procedure

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***Abstract*—This paper demonstrates the first fully integrated built-in self-test (BIST) $\Sigma-\Delta$ analog-to-digital converter (ADC) chip to the best of our knowledge. The ADC under test (AUT) comprises a second-order design-for-digital-testability $\Sigma-\Delta$ modulator and a decimation filter. The purely digital BIST circuitry conducts single-tone tests for the signal-to-noise-and-distortion ratio (SNDR), the dynamic range, the offset, and the gain error of the AUT. The BIST design is based on the proposed modified controlled sine-wave fitting procedure to address the component overload issues, reduce the setup parameter numbers, and eliminate the need for parallel multipliers. The total gate count of the whole BIST circuitry is only 13 300. The hardware overhead is much less than the BIST design using the traditional fast Fourier transform (FFT) analysis. Measurement results show that the peak SNDR results of the proposed BIST design and the conventional FFT analysis are 75.5 and 75.3 dB, respectively. The subtle SNDR difference is already within analog test uncertainty. The BIST $\Sigma-\Delta$ ADC achieves a digital test bandwidth higher than 17 kHz, very close to the rated 20-kHz bandwidth of the AUT.**

***Index Terms*—Analog-to-digital conversion (ADC), built-in self-test (BIST), design for testability, integrated circuit testing, mixed analog–digital integrated circuits, $\Sigma-\Delta$ modulation.**

I. Introduction

As FABRICATION cost of modern mixed-signal IC keeps decreasing while testing cost does not, reducing high testing cost becomes a substantial issue for industry. The root causes of the high testing cost include expensive mixed-signal automatic test equipment (ATE), long test time, and ultralow noise testing environment [1]. To address high testing cost, many built-in self-test (BIST) techniques for mixed-signal circuits have been proposed [2]–[17]. The functional-test-based BIST techniques are particularly appealing for analog-to-digital converters (ADCs) [2]–[4], [13], [14], [16]–[18]. The key idea is to embed the mandatory equipment of functional tests, including the analog stimulus generator (ASG) and the output response analyzer (ORA) on chip. Therefore, no costly mixed-signal ATE is needed. The test environment setup also becomes easier because of the absence of off-chip analog signal paths. In addition, the BIST approaches could provide standard test results as conventional functional tests do because of their functional-test-based feature.

The major challenge of the BIST design is to implement the embedded high-precision ASG and ORA cost effectively. Jiang *et al.* proposed a deterministic dynamic element matching (DDEM) approach for digital-to-analog converters (DACs). With the DDEM, a low-resolution DAC can generate uniformly spaced voltage samples for testing ADCs [4]. Hence, the BIST hardware cost can be reduced.

Alternatively, we proposed a design-for-digital-testability (DfDT) structure for implementing digitally testable $\Sigma-\Delta$ modulators in [19]. During digital tests, the DfDT structure is reconfigured as a 1-bit digital-to-charge converter (DCC). The 1-bit DCC then takes a $\Sigma-\Delta$ modulated bitstream as the test stimulus and generates a nonlinearity-free analog stimulus. Consequently, the DfDT structure serves as the mandatory high-precision ASG very well. An additional advantage of the DfDT scheme is that the stimulus generation and the response analysis are performed by digital circuits. Thus, the BIST functions can be integrated with the analog core more conveniently. Experimental results verified many advantages of the DfDT scheme, such as a small analog hardware overhead, high testing accuracy, high fault observability, and the capability of conducting at-speed tests.

Reference [20] demonstrates a BIST $\Sigma-\Delta$ ADC prototype using the same second-order DfDT $\Sigma-\Delta$ modulator in [19] as the modulator under test (MUT). The proposed BIST design in [20] is based on the controlled sine-wave fitting (CSWF) method [21]. A field-programmable gate array is used to implement the purely digital BIST circuits, including the digital stimulus generator (DSG) and the ORA. Experimental results show that the BIST signal-to-noise-and-distortion ratio (SNDR) results of the 1-kHz tone tests are almost the same as those obtained by the conventional fast Fourier transform (FFT) analysis [20]. However, several issues remain. First, the test bandwidth of the BIST prototype is less than 8 kHz. Second, the BIST results significantly differ from the corresponding FFT results for stimulus levels higher than −5 dBFS. Finally, the prototype is not fully integrated.

This paper demonstrates the first fully integrated BIST $\Sigma-\Delta$ ADC to the best of our knowledge. We propose a novel CSWF procedure and a new DSG to address the aforementioned issues of [20]. The new BIST design achieves SNDR results very close

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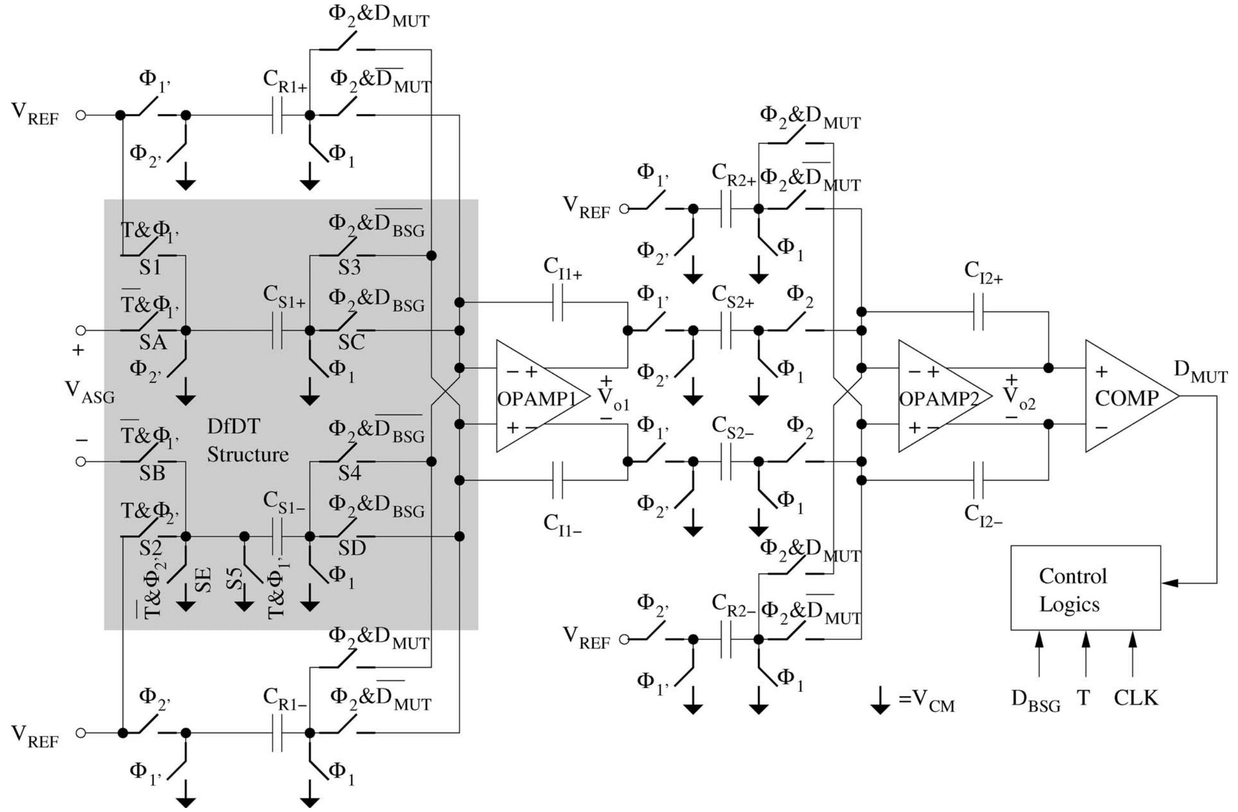

Fig. 1. Schematic of the DfDT second-order Σ−Δ modulator [19].

to that obtained by the FFT analysis, even for the −3-dBFS 1-kHz test. In addition, the new DSG design successfully extends the BIST test bandwidth from 8 kHz to higher than 17 kHz. The new DSG also improves the SNDR results of the digital tests because the generated digital stimuli achieve higher in-band SNDRs. The rest of this paper is organized as follows: Section II describes the Σ−Δ ADC under test (AUT). Section III depicts the proposed BIST procedure and the detailed circuit implementation. This paper particularly discusses the root causes and our solutions of the limited test bandwidth and stimulus level of [20]. Section IV reveals the measurement results. Finally, Section V concludes this paper.

II. AUT

The AUT consists of two parts: 1) a second-order DfDT single-bit Σ−Δ modulator as proposed in [19] as the MUT and 2) a decimation filter. The AUT is designed for audio applications with a rated passband of 20 kHz and operates at an oversampling ratio (OSR) of 128 and a 6.144-MHz oversampling clock. The DfDT Σ−Δ modulator can digitally be tested with a Σ−Δ modulated bitstream. The following reviews the design.

Fig. 1 shows the schematic of the second-order DfDT single-bit Σ−Δ modulator [19]. The modulator is composed of two cascaded summing switched-capacitor (SC) integrators and a comparator, and outputs a pulse-density-modulated (PDM) bitstream D_{MUT}, where $D_{\mathrm{MUT}}(n) \in \{0, 1\}$. Φ_1 and Φ_2 are two nonoverlapped clock phases derived from the oversampling clock f_{CLK}.

A test-mode control pin T switches the operation of the DfDT modulator between the normal mode and the test mode. By setting T to 0 and fixing the digital stimulus input D_{BSG} at 1, the switches $S1$ to $S5$ of the first SC integrator are turned off. The DfDT Σ−Δ modulator is configured as a conventional second-order Σ−Δ modulator [22]. In the normal mode, the modulator accepts the analog stimulus $V_{\mathrm{ASG}}(z)$ and converts it into the PDM output D_{MUT}.

Let A_T and $X_{\mathrm{BIST}}(z)$ be the amplitude and the Z-transform of the normalized single-tone sinusoidal stimulus. The analog stimulus is expressed as

$$V_{\mathrm{ASG}}(z) = A_T X_{\mathrm{BIST}}(z). \tag{1}$$

Without loss of generality, a Σ−Δ modulator is usually characterized by its normalized I/O relationship [22]. For convenience, $Y_{\mathrm{MUT}} \equiv 2D_{\mathrm{MUT}} - 1$ is defined as the normalized digital output of the MUT, whose value is either −1 or 1. Then, the bitstream output of the DfDT modulator in the normal mode can be described by

$$Y_{\mathrm{MUT}}(z) = \mathrm{STF}_{\mathrm{MUT}}(z) A_T X_{\mathrm{BIST}}(z) + \mathrm{NTF}_{\mathrm{MUT}}(z) E_{\mathrm{MUT}}(z) \tag{2}$$

where $\mathrm{STF}_{\mathrm{MUT}}(z)$, $\mathrm{NTF}_{\mathrm{MUT}}(z)$, and $E_{\mathrm{MUT}}(z)$ represent the signal transfer function (STF), the noise transfer function (NTF), and the quantization noise of the MUT, respectively.

Let A_1 and A_2 be the open-loop gains of the operational amplifiers in the first and second SC integrators, respectively.

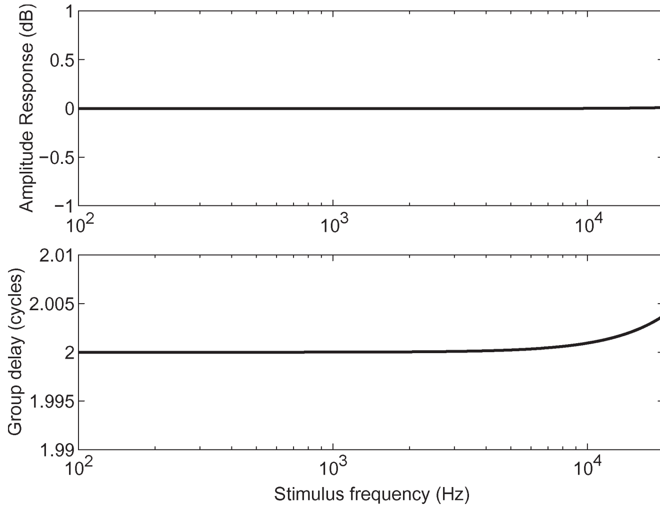

Fig. 2. In-band amplitude response and group delay of $\mathrm{STF}_{\mathrm{MUT}}(z)$ versus stimulus frequency.

The STF of the MUT is shown as [23]

$$\mathrm{STF}_{\mathrm{MUT}}(z) = \frac{\alpha_1\alpha_2 z^{-2}}{1-(\beta_1+\beta_2-\alpha_2)z^{-1}+(\alpha_1\alpha_2+\beta_1(\beta_2-\alpha_2))\,z^{-2}} \tag{3}$$

where

$$\begin{aligned}\alpha_1 &= \frac{C_{S1}}{C_{I1}+(C_{I1}+C_{S1}+C_{R1}+C_{p1})/A_1}\\ \alpha_2 &= \frac{C_{S2}}{C_{I2}+(C_{I2}+C_{S2}+C_{R2}+C_{p2})/A_2}\\ \beta_1 &= \frac{C_{I1}+(C_{I1}+C_{p1})/A_1}{C_{I1}+(C_{I1}+C_{S1}+C_{R1}+C_{p1})/A_1}\\ \beta_2 &= \frac{C_{I2}+(C_{I2}+C_{p2})/A_2}{C_{I2}+(C_{I2}+C_{S1}+C_{R2}+C_{p2})/A_2}.\end{aligned} \tag{4}$$

Fig. 2 plots the amplitude response and the group delay of $\mathrm{STF}_{\mathrm{MUT}}(z)$ by applying the nominal design parameters of [19] to (4) and (3). For the MUT, $\mathrm{STF}_{\mathrm{MUT}}(z)$ approximately has a unit gain and a group delay of two sampling cycles within the passband. These two features will be used to simplify the BIST design in Section III.

On the other hand, the MUT operates in the test mode if the test-mode control pin T is 1. The switches SA, SB, and SE are turned off. The DfDT structure, which is highlighted by the shaded area of Fig. 1, is now reconfigured as a differential 1-bit DCC. The DCC accepts the bitstream stimulus D_{BSG} and generates the required analog stimulus of the MUT in the test mode. The I/O relationship of the test-mode-enabled MUT is shown [19] to be

$$Y_{\mathrm{MUT}}(z) = \mathrm{STF}_{\mathrm{MUT}}(z)Y_{\mathrm{BSG}}(z) + \mathrm{NTF}_{\mathrm{MUT}}(z)E_{\mathrm{MUT}}(z). \tag{5}$$

A single-bit digital $\Sigma-\Delta$ modulator is used to modulate the desired test stimulus $A_T X_{\mathrm{BIST}}(z)$ and outputs the digital test stimulus Y_{BSG} for the MUT. Let $\mathrm{STF}_{\mathrm{SDM}}(z)$, $\mathrm{NTF}_{\mathrm{SDM}}(z)$, and $E_{\mathrm{SDM}}(z)$, respectively, represent the STF, the NTF, and the quantization noise of the digital $\Sigma-\Delta$ modulator. The normalized I/O relationship of the digital $\Sigma-\Delta$ modulator is

$$Y_{\mathrm{BSG}}(z) = \mathrm{STF}_{\mathrm{SDM}}(z)A_T X_{\mathrm{BIST}}(z) + \mathrm{NTF}_{\mathrm{SDM}}(z)E_{\mathrm{SDM}}(z). \tag{6}$$

By (6), (5) can be rewritten as [20]

$$\begin{aligned}Y_{\mathrm{MUT}}(z) = {}& \mathrm{STF}_{\mathrm{MUT}}(z)\mathrm{STF}_{\mathrm{SDM}}(z)A_T X_{\mathrm{BIST}}(z)\\ &+ \mathrm{STF}_{\mathrm{MUT}}(z)\mathrm{NTF}_{\mathrm{SDM}}(z)E_{\mathrm{SDM}}(z)\\ &+ \mathrm{NTF}_{\mathrm{MUT}}(z)E_{\mathrm{MUT}}(z).\end{aligned} \tag{7}$$

Equations (7) and (2) indicate that the only difference between the normal-mode and the test-mode outputs is the $\mathrm{STF}_{\mathrm{MUT}}(z)\mathrm{NTF}_{\mathrm{SDM}}(z)E_{\mathrm{SDM}}(z)$ term given $\mathrm{STF}_{\mathrm{SDM}}(z) = 1$. Since the quantization noise $E_{\mathrm{SDM}}(z)$ is high-pass shaped by $\mathrm{NTF}_{\mathrm{SDM}}(z)$, the digital and the corresponding analog tests should have very similar output spectra and test results.

The single-bit characteristic of the reconfigured DCC ensures the generated analog stimuli in the test mode being purely linear. In addition, the digital test does not require a bulky antialiasing filter since the generated analog charge stimulus is already a discrete-time signal and is synchronized by the same oversampling clock f_{CLK}.

The PDM output of the MUT is oversampled and contains significant out-of-band shaped quantization noise. The successive decimation filter removes the out-of-band noise and downsamples the output to the Nyquist rate. The decimation filter is similar to the design in [20]. The transfer function of the decimation filter $H_{\mathrm{DEC}}(z)$ has an approximate unity amplitude response within the passband.

Since the decimation filter removes most out-of-passband noise in (7) and $\mathrm{STF}_{\mathrm{SDM}}(z') = 1$ in our design, the decimated output of the test-mode-enabled $\Sigma-\Delta$ AUT can approximately be expressed by

$$\begin{aligned}Y_{\mathrm{DEC}}(z') = {}& \mathrm{STF}_{\mathrm{MUT}}(z')H_{\mathrm{DEC}}(z')A_T X_{\mathrm{BIST}}(z')\\ &+ \mathrm{THDN}_{\mathrm{MUT}}(z')H_{\mathrm{DEC}}(z') + \mathrm{OS}_{\mathrm{MUT}}\end{aligned} \tag{8}$$

where $\mathrm{THDN}_{\mathrm{MUT}}(z')$ and $\mathrm{OS}_{\mathrm{MUT}}$ are the in-band total-harmonic-distortion-plus-noise (THD+N) and the offset of the MUT, respectively. Here, we use the notation $z' \equiv e^{j2\pi f\cdot 128/f_{\mathrm{CLK}}}$ to indicate that the decimation filter's output has been downsampled by a factor of 128.

III. Design of the BIST Circuitry

The proposed BIST design is based on the CSWF method [21] and conducts single-tone tests. The key idea of the CSWF method is that an AUT's output $y_{\mathrm{DEC}}(n')$ can always be expressed by

$$y_{\mathrm{DEC}}(n') = y_{\mathrm{REF}}(n') + \mathrm{thdn}(n') + \mathrm{OS}_{\mathrm{MUT}} \tag{9}$$

where $\mathrm{thdn}(n')$, $\mathrm{OS}_{\mathrm{MUT}}$, and $y_{\mathrm{REF}}(n')$ represent the THD+N signal, the offset, and the offset-and-THD+N-free stimulus tone response of the AUT, respectively. If we can generate a

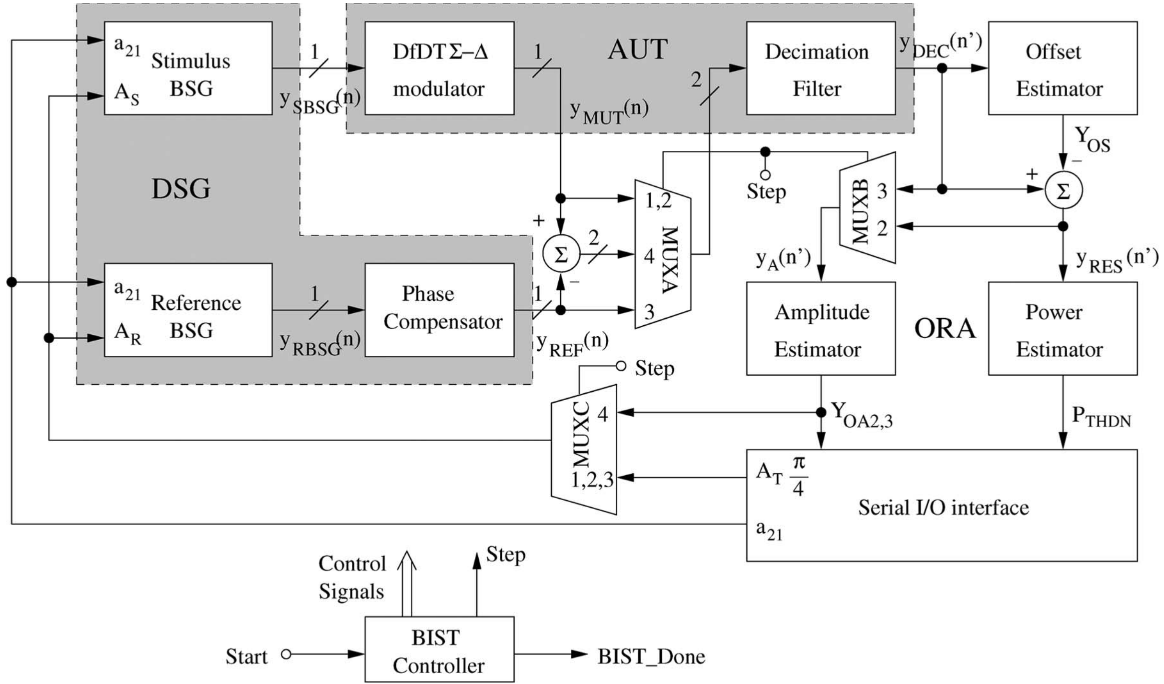

Fig. 3. Block diagram of the proposed fully integrated BIST Σ−Δ ADC.

digital reference signal identical to $y_{\mathrm{REF}}(n')$, then the digitized THD+N signal can be derived in the time domain according to

$$\mathrm{thdn}(n') = y_{\mathrm{DEC}}(n') - \mathrm{OS}_{\mathrm{MUT}} - y_{\mathrm{REF}}(n'). \qquad (10)$$

Calculating the power of the resulted $\mathrm{thdn}(n')$ signal results in the desired total THD+N power.

Fig. 3 shows the block diagram of the proposed fully integrated BIST Σ−Δ ADC, comprising a DSG, an ORA, and the aforementioned Σ−Δ AUT in Section II.

The DSG consists of two bitstream generators (BSGs): The stimulus BSG (SBSG) is in charge of generating the digital bitstream stimuli for the AUT, whereas the reference BSG (RBSG) generates the digital reference bitstream $y_{\mathrm{REF}}(n)$ for the BIST operation. The same stimulus frequency parameter a_{21} sets the frequency of the generated stimuli, and A_S and A_R set the stimulus amplitudes of the SBSG and the RBSG, respectively.

The proposed BIST design takes the advantages from three important MUT characteristics to reduce hardware overhead.

First, Fig. 2 indicates that the MUT has an approximate group delay of two oversampling clock cycles. Hence, the complex phase error calibration loop in [21] is not needed. Second, the input and output of the MUT are all single bit. Note that the bitstream output of the MUT contains similar in-band signals to the decimated output, implying that the BIST functions can be performed either before or after decimation. Therefore, this BIST design conducts the phase compensation and the subtraction for deriving the THD+N signal with the bitstream outputs of the DSG and the MUT to save hardware cost. For example, the phase compensator of this design is as simple as two cascaded flip-flops. Finally, the proposed BIST procedure further reduces the BIST hardware overhead as discussed in the following.

A. *Proposed BIST Procedure*

The proposed BIST procedure consists of four steps. The control signal $STEP$ in Fig. 3 represents the current BIST step index. Each BIST step must be a coherent test with the same stimulus frequency parameter a_{21}. That is, a_{21} must be chosen such that the N decimated outputs of the AUT taken for analysis exactly contain integer cycles of the stimulus tone. The following describes the proposed BIST procedure in detail.

1) Calculating the Offset: In the beginning, a_{21} is loaded into the DSG. Meanwhile, A_S is set to $A_T\pi/4$. The SBSG generates the bitstream stimulus $y_{\mathrm{SBSG}}(n)$ for the AUT. The bitstream output of the MUT $y_{\mathrm{MUT}}(n)$ flows through the multiplexer $MUXA$ and the decimation filter to the offset estimator. The function of the offset estimator is [20], [21]

$$Y_{\mathrm{OS}} = \frac{1}{N}\sum_{n'=1}^{N} y_{\mathrm{DEC}}(n'). \qquad (11)$$

By (9), (11) is rewritten as

$$Y_{\mathrm{OS}} = \mathrm{OS}_{\mathrm{MUT}} + \frac{1}{N}\sum_{n'=1}^{N} \mathrm{thdn}(n') \qquad (12)$$

since the test is coherent, and thus, the stimulus response part of $y_{\mathrm{DEC}}(n')$ vanishes after accumulation. The term $(1/N)\sum_{n'=1}^{N}\mathrm{thdn}(n')$ in (12) approximates to zero because $\mathrm{thdn}(n')$ is a random process with a zero mean. Hence, the estimated offset Y_{OS} well approximates to $\mathrm{OS}_{\mathrm{MUT}}$. Y_{OS} is stored in a register for the following BIST steps.

2) Calculating the Stimulus Amplitude of the Output Response: The test setup of the second BIST step is the same as for the first step, except that the offset estimator's output is fixed at Y_{OS}. The BIST circuitry first removes Y_{OS} from the

decimated output of the AUT. Then, the stimulus amplitude estimator accepts the offset-free response $y_{\mathrm{RES}}(n')$ through the multiplexer $MUXB$ and estimates the stimulus amplitude of $y_{\mathrm{RES}}(n')$. This paper modifies the amplitude estimator function in [21] to be

$$Y_{\mathrm{OA2}} = \frac{2}{N}\sum_{n'=1}^{N}|y_A(n')|. \quad (13)$$

Since A_S is set to $A_T\pi/4$ and the generated stimulus flows through the MUT and the decimation filter, we have

$$y_A(n') = y_{\mathrm{RES}}(n') = A_O \sin\left(2\pi\frac{f_{\mathrm{in}}}{f_{\mathrm{clk}}}n'\right) + \mathrm{thdn}(n') \quad (14)$$

where

$$A_O = \frac{\pi}{4}A_T\,|\mathrm{STF}_{\mathrm{MUT}}(f_{\mathrm{in}})|\,|H_{\mathrm{DEC}}(f_{\mathrm{in}})| \quad (15)$$

and $|\mathrm{STF}_{\mathrm{MUT}}(f_{\mathrm{in}})|$ and $|H_{\mathrm{DEC}}(f_{\mathrm{in}})|$ are the frequency amplitude responses of the MUT's STF and the decimation filter at the stimulus frequency f_{in}, respectively. By (14), (13) can be rewritten as

$$\begin{aligned} Y_{\mathrm{OA2}} &\simeq \frac{2}{N}\sum_{n'=1}^{N}\left|A_O\sin\left(2\pi\frac{f_{\mathrm{in}}}{f_{\mathrm{clk}}}n'\right)\right| \\ &= \frac{2}{N}A_O\sum_{n'=1}^{N}\left|\sin\left(2\pi\frac{f_{\mathrm{in}}}{f_{\mathrm{clk}}}n'\right)\right| \\ &= \frac{4}{\pi}A_O. \end{aligned} \quad (16)$$

Consequently, the output of the amplitude estimator becomes

$$Y_{\mathrm{OA2}} = A_T\,|\mathrm{STF}_{\mathrm{MUT}}(f_{\mathrm{in}})|\,|H_{\mathrm{DEC}}(f_{\mathrm{in}})|. \quad (17)$$

Y_{OA2} is stored in a register for the last BIST step.

In the similar BIST step of [20], A_S is set to $A_T\pi/2$ to simplify the ORA design. This means that the SBSG has to generate a 3.9-dB larger stimulus than needed. However, both the SBSG and the MUT are $\Sigma{-}\Delta$ modulators and will be overloaded if the stimulus amplitude exceeds their intrinsic limits [24]. As a result, the BIST results of [20] have large errors for the tests with an A_T larger than -5 dBFS.

In the proposed BIST procedure, the SBSG now generates a stimulus -2.1 dB smaller than A_T. Therefore, both the SBSG and the AUT are less likely to be overloaded, and the maximum A_T can be higher.

3) Calculating A_S for the Last BIST Step: The third BIST step is an optional step for calculating the setup value of A_S in the last BIST step. In the last BIST step of [20], an additional input parameter $A_T|H_{\mathrm{DEC}}(f_{\mathrm{in}})|$ is needed. This value depends on the decimation filter design and the test setup. In some cases, the BIST designer may not have the information.

With this additional step, the BIST designer does not need to know the detailed design of the decimation filter while the BIST results are still correct. The memory needed for storing the setup parameters of the tests is also reduced.

This BIST step sets A_R to $A_T\pi/4$ to generate the reference bitstream $y_{\mathrm{RBSG}}(n)$. $y_{\mathrm{RBSG}}(n)$ flows through the $MUXA$, the decimation filter, and the $MUXB$ to the amplitude estimator. The output of the amplitude estimator is shown to be

$$Y_{\mathrm{OA3}} \cong A_T\,|H_{\mathrm{DEC}}(f_{\mathrm{in}})| \quad (18)$$

and is used to set the A_S of the last BIST step.

4) Calculating the THD+N Power: The final BIST step calculates the THD+N power. The setting values of A_S and A_R are different from those in [20]. Here, A_R and A_S are set to Y_{OA2} and Y_{OA3}, respectively. According to (6), (7), (17), and (18), we have

$$\begin{aligned} Y_{\mathrm{REF}}(z) =& A_T H_{\mathrm{FC}}(z)\,|\mathrm{STF}_{\mathrm{MUT}}(f_{\mathrm{in}})|\,|H_{\mathrm{DEC}}(f_{\mathrm{in}})| \\ &\times X_{\mathrm{BIST}}(z) + \mathrm{NTF}_{\mathrm{SDM}}(z)E'_{\mathrm{SDM}}(z) \quad (19) \\ Y_{\mathrm{MUT}}(z) =& \mathrm{STF}_{\mathrm{MUT}}(f_{\mathrm{in}})A_T\,|H_{\mathrm{DEC}}(f_{\mathrm{in}})|\,X_{\mathrm{BIST}}(z) \\ &+ \mathrm{STF}_{\mathrm{MUT}}(z)\mathrm{NTF}_{\mathrm{SDM}}(z)E_{\mathrm{SDM}}(z) \\ &+ \mathrm{NTF}_{\mathrm{MUT}}(z)E_{\mathrm{MUT}}(z) \\ &+ \mathrm{THDN}_{\mathrm{MUT}}(z) + \mathrm{OS}_{\mathrm{MUT}}. \quad (20) \end{aligned}$$

The term $H_{\mathrm{FC}}(z)$ represents the transfer function of the phase compensator, which is z^{-2}. By subtracting (19) from (20), the input of the decimation filter in this step is

$$\begin{aligned} &Y_{\mathrm{MUT}}(z) - Y_{\mathrm{REF}}(z) \\ &\quad\simeq \mathrm{NTF}_{\mathrm{SDM}}(z)\left(\mathrm{STF}_{\mathrm{MUT}}(z)E_{\mathrm{SDM}}(z) - E'_{\mathrm{SDM}}(z)\right) \\ &\qquad + \mathrm{NTF}_{\mathrm{MUT}}(z)E_{\mathrm{MUT}}(z) \\ &\qquad + \mathrm{THDN}_{\mathrm{MUT}}(z) + \mathrm{OS}_{\mathrm{MUT}} \end{aligned} \quad (21)$$

because Fig. 2 indicates that the group delay of $\mathrm{STF}_{\mathrm{MUT}}(f_{\mathrm{in}})$ is very close to z^{-2}. The following decimation filter and the offset subtractor remove the out-of-band shaped noise and the offset. Consequently, the residue signal $y_{\mathrm{RES}}(n')$ in this step only consists of the in-band THD+N signal.

Finally, the power estimator calculates the total in-band THD+N power according to

$$P_{\mathrm{THDN}} = \frac{1}{N}\sum_{n'=1}^{N} y_{\mathrm{RES}}(n')^2. \quad (22)$$

The power estimator demands the only multiplication in the proposed BIST procedure. Because its input has been downsampled by a factor of OSR, a simpler serial multiplier is used to implement the power estimator.

B. Design of the ORA

The major blocks of the ORA are the offset, stimulus amplitude, and power estimators. Their functions are summarized in Table I, where $N = 2048$ is the number of the decimated outputs to be analyzed by the BIST circuitry for every BIST step. According to Table I, the design uses two simple accumulators to realize the offset estimator and the stimulus

TABLE I
FUNCTIONS OF THE ORA BLOCKS

Block name	Block function
Offset Estimator	$Y_{OS} = \frac{1}{N}\sum_{n'=1}^{N} y_{DEC}(n')$
Amplitude Estimator	$Y_{OA} = \frac{2}{N}\sum_{n'=1}^{N} \lvert y_A(n')\rvert$
Power Estimator	$P_{THDN} = \frac{1}{N}\sum_{n'=1}^{N} y_{RES}(n')^2$

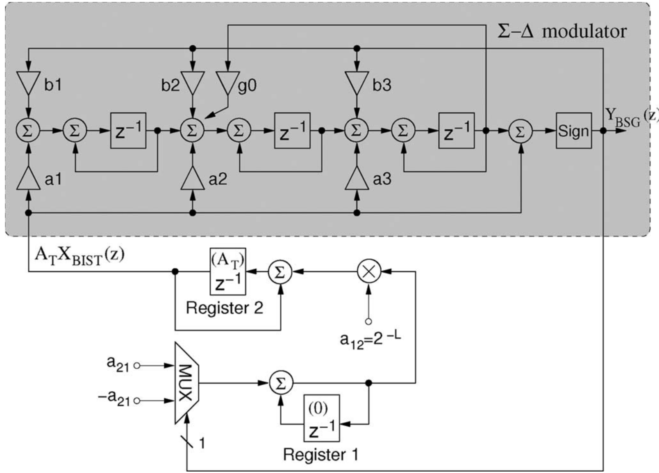

Fig. 4. Schematic of the proposed BSG with the third-order $\Sigma-\Delta$ modulator.

amplitude estimator, and a serial multiplier to implement the power estimator.

An optional serial I/O interface is added to the test chip so that the BIST can conduct various tests. The serial interface can also monitor the detailed BIST results such as the estimated offset, the stimulus amplitude in the response, and the THD+N power. In practical BIST applications, this serial I/O interface is not mandatory. Instead, these outputs can be compared with some predetermined threshold values, and a single-bit pass/fail output is sufficient.

C. Design of the BSG

The BSGs must generate well-controlled and high-quality bitstream stimuli. Intuitively, the BSG can be realized by a digital oscillator cascading the aforementioned digital $\Sigma-\Delta$ modulator in Section II. The area-efficient oscillator circuit proposed in [25] is an alternative low-cost approach because it does not require any parallel multiplier. However, the BIST design that adopts the area-efficient oscillator in [25] does not show good enough BIST results [20]. The second-order digital $\Sigma-\Delta$ modulator used in the oscillator is one of the root causes. For high-stimulus-frequency tests, the second-order digital $\Sigma-\Delta$ modulator cannot generate digital stimuli with high enough in-band SNDRs.

To enhance the SNDR of the bitstream stimulus, we propose the BSG design shown in Fig. 4. The proposed BSG is an alternative realization of a digital resonator embedded with a third-order digital $\Sigma-\Delta$ modulator. The third-order digital $\Sigma-\Delta$ modulator plays the same role as that described by (6), which generates $\Sigma-\Delta$ modulated bitstreams for digital tests. According to (6), the analysis of the BSG can be divided into the stimulus and the noise parts.

For the stimulus tone part, detailed analysis shows that the loop gain of the proposed BSG is

$$L(z) = \frac{-a_{12}a_{21}z^{-1}\mathrm{STF}_{\mathrm{SDM}}(z)}{(1-z^{-1})^2}. \tag{23}$$

To keep the oscillation stable, the Barkhausen criterion requests $L(z) = 1$. Let $\mathrm{STF}_{\mathrm{SDM}}(z) = 1$, the characteristic equation (CE) of the BSG becomes

$$z^{-2} + (a_{12}a_{21} - 2)z^{-1} + 1 = 0. \tag{24}$$

Equation (24) is the same as that of [25]. Therefore, the same design criterion of [25] holds in our design as

$$0 < a_{12}a_{21} < 4 \tag{25}$$

$$f_{\mathrm{in}} = f_{\mathrm{CLK}}\frac{\cos^{-1}(1 - a_{12}a_{21}/2)}{2\pi}, \qquad 0 < a_{12}a_{21} < 2$$
$$f_{\mathrm{in}} = f_{\mathrm{CLK}}\left(\frac{1}{2} - \frac{\cos^{-1}(1 - a_{12}a_{21}/2)}{2\pi}\right), \qquad 2 < a_{12}a_{21} < 4. \tag{26}$$

We set a_{12} to 2^{-6} to simplify the circuit implementation. The desired amplitude of the generated stimulus can precisely be controlled by the initial value of Register 2 while setting the initial value of Register 1 to zero [25].

In addition to the signal part, the shaped quantization noise of the digital $\Sigma-\Delta$ modulator, i.e., $\mathrm{NTF}_{\mathrm{SDM}}(z)E_{\mathrm{SDM}}(z)$, also circles in the oscillation loop. The shaped quantization noise may disturb the stable oscillation of the BSG. Taking the term $\mathrm{NTF}_{\mathrm{SDM}}(z)E_{\mathrm{SDM}}(z)$ into account, the CE of the proposed BSG is shown to be

$$z^{-2} + (a_{12}a_{21} - 2)z^{-1} + 1 + a_{12}a_{21}z^{-1}\frac{\mathrm{NTF}_{\mathrm{SDM}}(z)E_{\mathrm{SDM}}(z)}{A_T X_{\mathrm{BIST}}(z)} = 0. \tag{27}$$

Equation (27) must also have solutions on the unit circle of the z-plane to generate purely sinusoidal stimuli. Since $E_{\mathrm{SDM}}(z)$ is a random process, an additional criterion for the BSG design is

$$\left|\frac{a_{12}a_{21}\mathrm{NTF}_{\mathrm{SDM}}(z_T)E_{\mathrm{SDM}}(z_T)}{A_T X_{\mathrm{BIST}}(z_T)}\right| \to 0 \tag{28}$$

where $z_T = e^{j2\pi f_{\mathrm{in}}/f_{\mathrm{CLK}}}$. To generate a well-controlled stimulus, $a_{12}a_{21}$ and $|\mathrm{NTF}_{\mathrm{SDM}}(z_T)E_{\mathrm{SDM}}(z_T)|$ should be as small as possible, and a larger A_T is preferred according to (28). However, only the term $|\mathrm{NTF}_{\mathrm{SDM}}(z_T)|$ is free for design.

Equation (28) explains why the test bandwidth of the BIST design in [20] is limited. The SNDR performance of the BSG design in [20] degrades when the stimulus frequency is

TABLE II
STRUCTURAL COEFFICIENTS OF THE THIRD-ORDER CRFB $\Sigma-\Delta$ MODULATOR

Coefficient	Value
a1	2^{-4}
a2	2^{-1}
a3	1
b1	-2^{-4}
b2	-2^{-1}
b3	-1
g0	-2^{-12}

high because of the necessity of a larger $a_{12}a_{21}$. The shaped quantization noise power term $|\mathrm{NTF}_{\mathrm{SDM}}(z_T)E_{\mathrm{SDM}}(z_T)|$ at the stimulus frequency is also higher. Both factors are against (28). Consequently, the generated high-frequency stimuli have poor SNDRs.

To fulfill (28) and the design criterion $\mathrm{STF}_{\mathrm{SDM}}(z) = 1$, we adopt the cascade of resonators with distributed feedback (CRFB) structure [22] to design the third-order digital $\Sigma-\Delta$ modulator shown in Fig. 4. Table II lists the structural coefficients. The proposed third-order $\Sigma-\Delta$ modulator has an STF exactly equal to 1, as desired. All the structure coefficients are designed to be powers of 2 to implement them without any metal–oxide–semiconductor field-effect transistor but wiring.

The proposed third-order $\Sigma-\Delta$ modulator has higher order noise shaping capability and an extra zero in its NTF. Both features lower the power spectral density (PSD) of the in-band quantization noise. As a result, (28) has a superior approximation to zero, although a large a_{21} is set. That is, the BSG can sustain more stable oscillation and generates high-frequency stimuli with higher SNDRs and leads to more accurate high-frequency BIST results. The proposed BSG also improves the test accuracy of low-stimulus-level BIST results because the generated stimuli have higher SNDRs.

D. Test Setup

An important feature of the proposed BIST design is the flexibility of conducting plural tests with the same hardware. Given a single-tone test with a desired stimulus amplitude A_T and a stimulus frequency f_{in}, the proposed BIST procedure requires only two setup parameters per test, including the stimulus frequency parameter a_{21} and the stimulus amplitude parameter $A_T\pi/4$. The setup parameters are calculated in advance and stored in embedded memory or externally loaded. For the former case, the proposed BIST procedure saves the embedded memory because of the reduced number of the setup parameters. In this design, the test parameters are scanned-in through the serial I/O interface.

IV. EXPERIMENTAL RESULTS

The fully integrated BIST $\Sigma-\Delta$ ADC has been fabricated in a 0.35-μm CMOS process. Fig. 5 shows the micrograph of the test chip. The area of the analog core is 0.66 mm^2, whereas the digital functions, including the decimation filter and the BIST circuitry, occupy 2.05 mm^2. Table III lists the test chip summary. The hardware overhead of the proposed BIST design contains 13 300 digital gates, much less than the BIST design using the conventional FFT method [26]. Although the BIST area ratio seems to be high, it is because we used 0.35-μm CMOS to implement the test chip. Since all the added BIST circuits are digital, their areas will become much smaller if the BIST design is ported to an advanced process such as 0.18- or 0.13-μm CMOS. On the other hand, the MUT itself is analog, and thus, its area benefits little from the advanced process. Consequently, the area overhead ratio of the BIST design will become smaller in advanced CMOS. It is noteworthy that, since the fabrication cost per transistor is lower in advanced CMOS, the silicon cost of the additional BIST circuitry is lower as well.

In the following measurements, the oversampling frequency and the OSR are 6.144 MHz and 128, respectively. The test stimulus is a -6-dBFS sinusoidal tone with a frequency of $41f_{\mathrm{clk}}/262\,144$, unless otherwise noted. The minimum-four-term window is applied to derive all spectra. Although the AUT is designed to have a 20-kHz passband, it is noteworthy that the BIST design cannot but calculate the total THD+N power within 24 kHz. Hence, the following test results are calculated using the 24-kHz THD+N bandwidth.

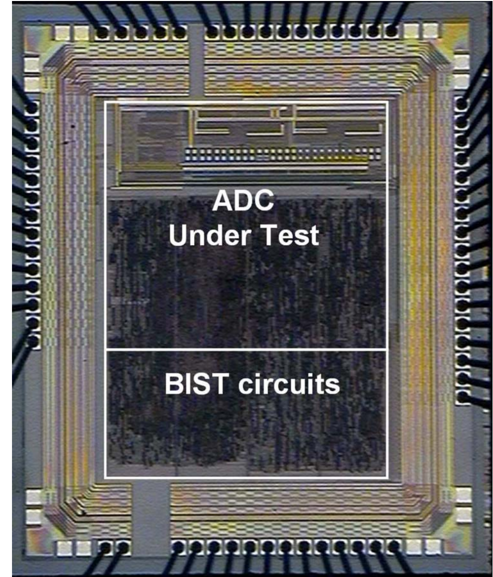

Fig. 5. Micrograph of the proposed fully integrated $\Sigma-\Delta$ ADC.

TABLE III
SUMMARY OF THE TEST CHIP

Process	0.35μm DPTM CMOS
Block	Area/gate count
BSGs	3.05k $\times 2$ gates
ORA	5.6k gates
Serial I/O and Controller	1.6k gates
Total BIST circuitry	13.3k gates
Decimation filter	15k gates
Digital core*	2.05 mm^2
Analog core	0.66 mm^2
BIST area overhead	35.5%
Test chip area	2.33mm by 2.72mm

* includes the decimation filter and the BIST circuits

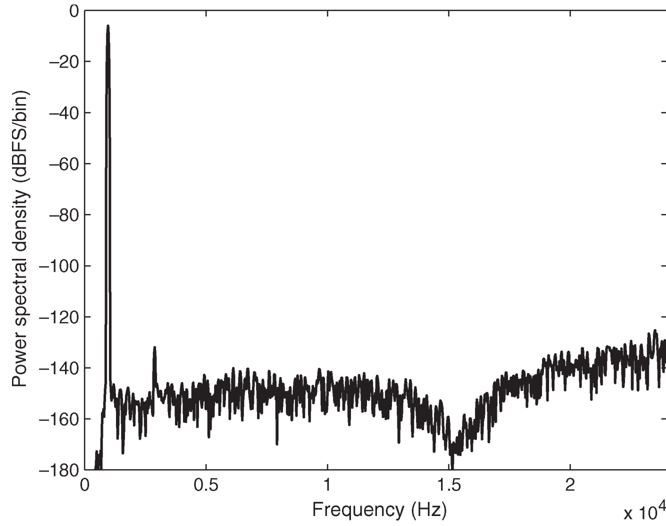

Fig. 6. Measured in-band output spectrum of the proposed BSG with the third-order digital $\Sigma-\Delta$ modulator. The BIST setup is $A_T = -6$ dBFS and $f_{\rm in} \simeq 1$ kHz.

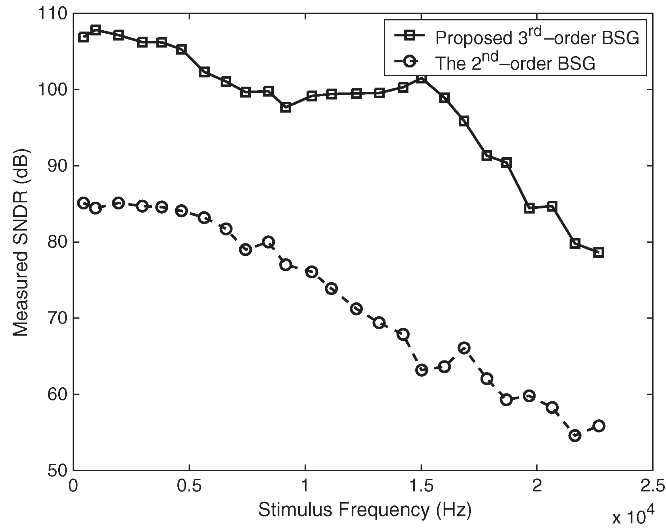

Fig. 7. In-band SNDRs of the proposed third-order BSG and the second-order BSG in [20].

A. Digital Stimulus Purity

Fig. 6 shows the spectrum of the generated bitstream stimulus by the proposed BSG. The digital stimulus achieves an in-band SNDR of 107.8 dB, which is much higher than the theoretical peak SNDR of the AUT. The zero of its NTF locates at around 15 kHz, which lowers the in-band noise floor.

Fig. 7 compares the performance of the proposed BSG with the second-order BSG in [20]. Due to better noise shaping capability, the third-order BSG provides the digital stimuli with in-band SNDR values higher than 90 dB up to 18.7 kHz. On the other hand, the SNDR values of the second-order one degrade to less than 80 dB for stimulus frequencies higher than 7.4 kHz. Since the AUT achieves a peak SNDR higher than 76 dB, the digital stimuli should have an in-band SNDR higher than 82 dB for an accurate enough peak SNDR result.

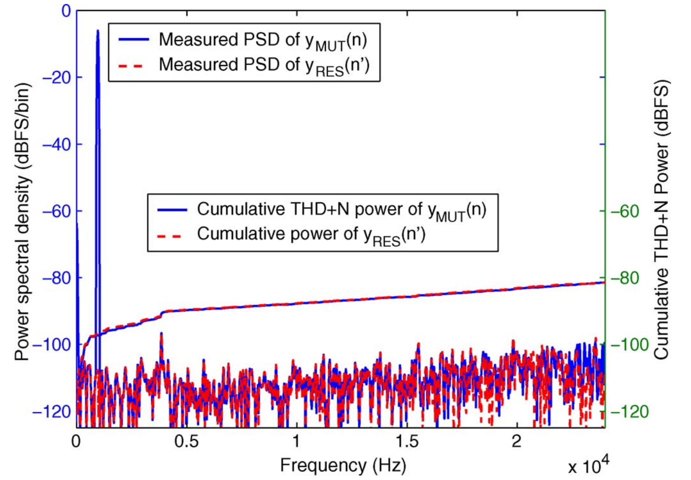

Fig. 8. Measured spectra of $y_{\rm MUT}(n)$ and $y_{\rm RES}(n')$ in the fourth BIST step of the 1-kHz test.

B. BIST Results

According to the proposed BIST procedure, the decimated residue signal $y_{\rm RES}(n')$ and the AUT's decimated output should have the same THD+N spectra in the fourth BIST step. In addition, the offset and the stimulus tone power of $y_{\rm RES}(n')$ should be zero. Since the current implementation cannot provide the decimated AUT's output of the fourth BIST step (an additional decimation filter is required for this purpose), we analyze the raw bitstream output $y_{\rm MUT}(n)$ instead to check the test accuracy of the BIST.

Fig. 8 shows the measured in-band spectra of $y_{\rm MUT}(n)$ and $y_{\rm RES}(n')$ in the last BIST step of the 1-kHz test. Indeed, the offset component of $y_{\rm RES}(n')$ has successfully been alleviated from -63.6 dBFS to less than -110 dBFS. The stimulus tone part of $y_{\rm RES}(n')$ is also eliminated. The residue stimulus tone power is less than -110 dBFS. In fact, the noise dominates the PSD values on the frequency bins belonging to the offset and the residue stimulus tone. Furthermore, the THD+N floors of both spectra are almost the same. The comparisons show that the THD+N information tested by the proposed BIST scheme is very similar to that by the conventional FFT analysis.

The THD+N floors have a somewhat larger difference at the frequencies close to the passband edge. It is because $y_{\rm MUT}(n)$ is not low-pass filtered by the decimation filter, whereas $y_{\rm RES}(n')$ is.

Fig. 9 compares the BIST results with the corresponding FFT results at various stimulus levels to show that the proposed CSWF BIST procedure is as accurate as the conventional FFT analysis. The SNDR differences are within 0.3 to -0.7 dB. The proposed BIST design can conduct the test with a peak A_T as high as -3 dBFS. However, an A_T higher than -3 dBFS is not applicable since such an A_T overloads the proposed third-order CRFB $\Sigma-\Delta$ modulator. Most high-order single-bit $\Sigma-\Delta$ modulators have similar limitations [27].

We also plot the test results of using the conventional analog test approach in Fig. 9 as references. The analog test results have good correlation to the digital test results and are somewhat higher than the corresponding BIST test results. For low stimulus levels, the SNDR differences between analog tests

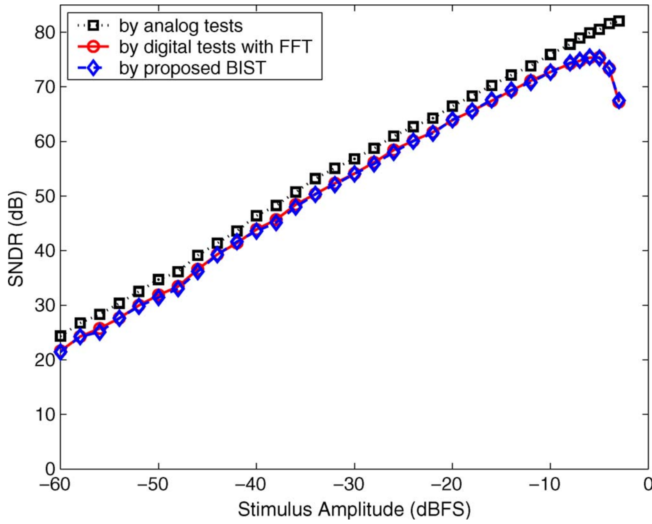

Fig. 9. Measured SNDR versus stimulus amplitude.

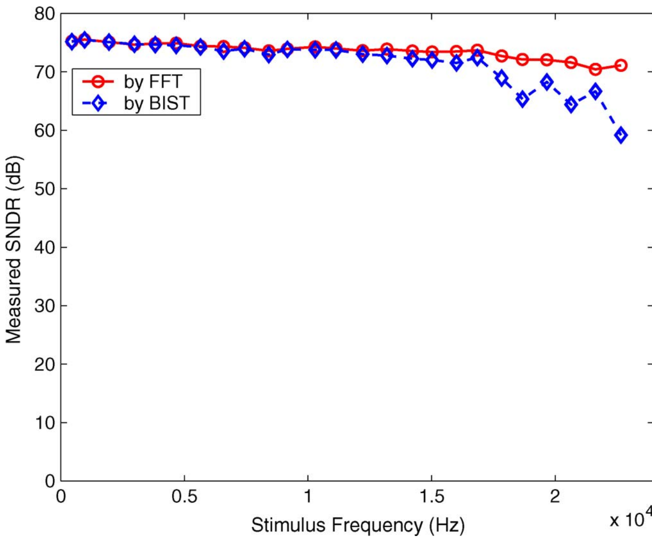

Fig. 10. Measured SNDR results of the proposed BIST design and the FFT analysis.

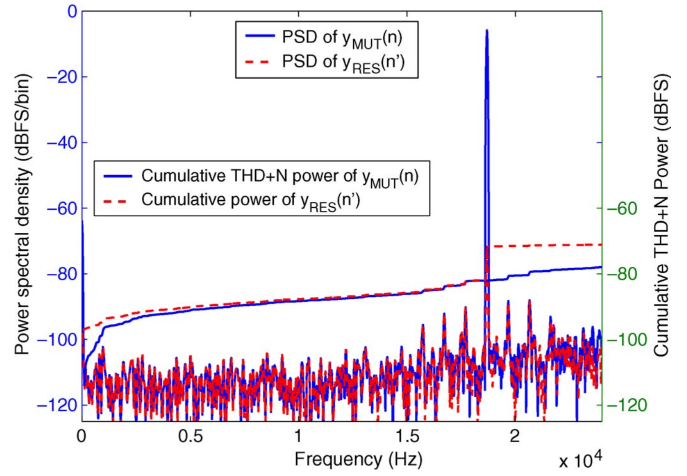

Fig. 11. Measured spectra of the decimated $y_{\rm MUT}(n)$ and $y_{\rm RES}(n')$ in the fourth BIST step of the test, where $f_{\rm in} = 18.7$ kHz.

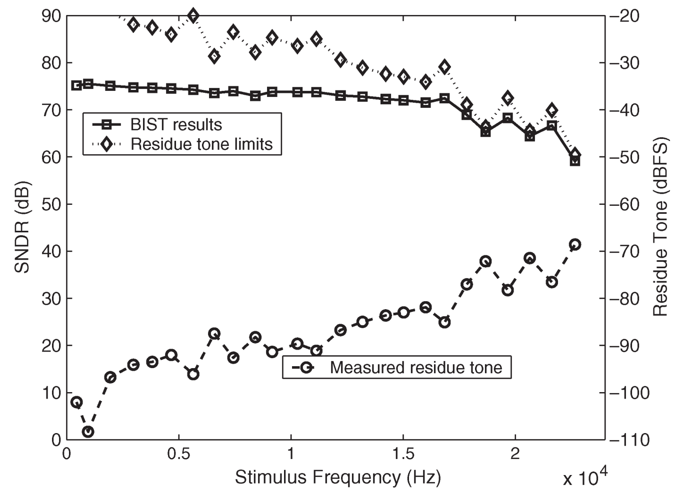

Fig. 12. Measured BIST SNDR results, residue tone power, and the SNDR limits set by the residue tone power.

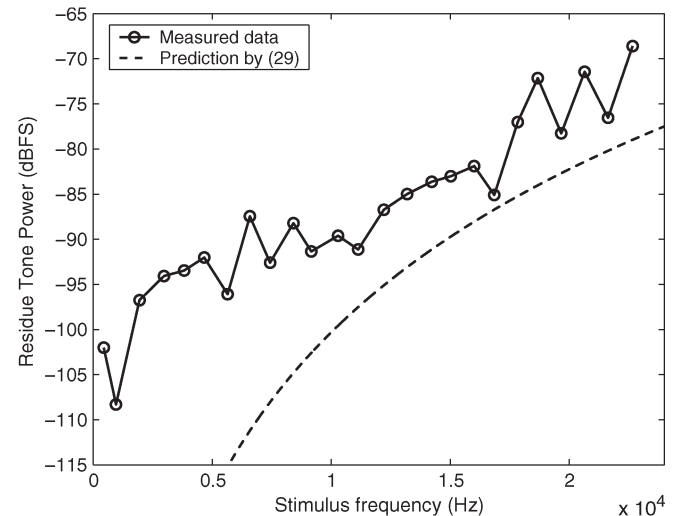

Fig. 13. Comparison of the theoretical residue tone power according to (29) with the measured data. $A_T = -6$ dBFS.

and the corresponding digital tests are less than 3 dB. The SNDR differences are higher for the stimulus levels close to the full-scale. It is noteworthy that the differences are due to the DfDT structure of the MUT, not due to the proposed BIST design [19], [24]. Since the digital stimuli are $\Sigma{-}\Delta$ modulated signals, their extra shaped noise saturates the MUT at a lower stimulus level. As a result, the digital test results with FFT and the BIST results bend down after -6 dBFS. Reference [24] proposed a decorrelating design-for-digital testability structure that can reduce the gap between the analog test results and the corresponding digital test results.

Fig. 10 compares the BIST results with their FFT counterparts of different stimulus frequencies. The SNDR differences are less than 0.7 dB for stimulus frequencies up to 12.2 kHz and are less than 3 dB when stimulus frequencies are lower than 17 kHz. The proposed BIST design successfully extends the test bandwidth from 8 kHz [20] to over 17 kHz. Note that the FFT results have no significant degradation with respect to the stimulus frequency. The reason is that the proposed BSG

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON

	[13]	[20]		This work	
AUT	Dual-channel second-order Σ-Δ ADCs for BIST	The second-order DfDT Σ-Δ ADC		The second-order DfDT Σ-Δ ADC	
AUT's sampling rate	12.288MHz	6.144 MHz		6.144 MHz	
AUT's OSR	256	128		128	
AUT's rated passband	22.05 kHz	20 kHz		20 kHz	
DSG	A 2252-bit shift register	The second-order BSG [25] $\times 2$		Proposed third-order BSG $\times 2$	
DSG's gate count	14.6k*	4.7k		6.1k	
Bit-stream length (bits)	2252	262144		262144	
SNDR of the 1 kHz, -6 dBFS digital stimulus	N/A	84.4 dB		107.8 dB	
SNDR of the 20 kHz, -6 dBFS digital stimulus	N/A	58.3 dB		86 dB	
Output Response Analysis Method	BIST by Matlab®©	FFT	BIST	FFT	BIST
THD+N passband	24 kHz	24 kHz	24 kHz	24 kHz	24 kHz
Decimated output samples taken for analysis	563	2048	2048	2048	2048
A_T for the peak SNDR	-12 dBFS	-6 dBFS	-6 dBFS	-6 dBFS	-6 dBFS
Peak SNDR $@f_{in} = 1$ kHz (dB)	$\approx 82, f_{in} = 5.456$kHz	74.6	74.3	75.3	75.5
Dynamic range† (dB)	$\approx 93, f_{in} = 5.456$kHz	82.3	82.3	81.6	81.5
Offset (dBFS)	N/A	-55.7	-55.7	-63.6	-63.6
Gain error (dB)	N/A	-0.01	-0.01	-0.0126	-0.0126
Test bandwidth	$f_{in} \in \{5.456, 10.912, 16.369, 21825\}$ kHz	10 kHz	8 kHz	20 kHz	17 kHz
SNDR difference $@f_{in} = 1$ kHz (dB)	N/A	+5.67~ -1.46		+0.68~ -0.29	
Total BIST overhead (gate count)	N/A	N/A	11.9k‡	N/A	13.3k‡
Setup memory per test (bits)	2252	96		64	
Fully integrated	No	No		Yes	

* Equivalent gate count of 2252 D-type flip-flops according to the same 0.35μm cell library used by this work.
† Dynamic range = SNDR @-60 dBFS (in dB) + 60 dB [28].
‡ includes the optional serial interface.

provides an in-band SNDR higher than 84 dB, although the stimulus frequency is as high as 20.65 kHz.

Checking the 18.7-kHz test may help us understand why the BIST results degrade at high stimulus frequencies. In the test, the proposed BIST circuitry results in an SNDR of 65.3 dB, whereas the FFT analysis leads to an SNDR of 72.1 dB. The BIST underestimates the SNDR of the AUT by -6.8 dB. Fig. 11 shows the spectra of $y_{\mathrm{MUT}}(n)$ and $y_{\mathrm{RES}}(n')$ in the fourth BIST step of the test. The offset component of $y_{\mathrm{RES}}(n')$ is successfully removed, and the THD+N floors of both spectra are also very similar. However, the residue stimulus tone in $y_{\mathrm{RES}}(n')$ is as high as -72.1 dBFS. Since the residue tone itself is counted as part of the THD+N signal, it dominates the calculated THD+N power and limits the BIST SNDR result to be less than $-6-(-72.1) = 66.1$ dB.

Fig. 12 shows the BIST SNDR results and the residue tone powers of different stimulus frequencies. Indeed, the worst three BIST results are limited by the too large residue tones.

The root cause of the large residue tones is the assumption used to simplify the BIST design that the group delay of the MUT is two clock cycles. Fig. 2 shows that this assumption is getting worse as the stimulus frequency increases. Let θ be the phase error in the sampling cycle. The phase error results in a residue tone whose amplitude is

$$2A_T \sin\left(\pi\theta \frac{f_{\mathrm{in}}}{f_{\mathrm{clk}}}\right). \quad (29)$$

Fig. 13 plots (29) and the measured residue tone power data of different stimulus frequencies when $A_T = -6$ dBFS. At low frequencies, the noise floor of the AUT dominates the residue tone power. At high frequencies, the measured data follow (29) quite well. The plots show that the increasing phase errors result in the increasing residue tones. Nevertheless, the proposed BIST design provides a test bandwidth very close to the rated signal bandwidth of the AUT. Table IV summarizes the performance of the proposed BIST design and compares with those of [13] and [20].

V. CONCLUSION

This paper has demonstrated a fully integrated BIST $\Sigma-\Delta$ ADC with a wide test bandwidth and high test accuracy. The new BIST procedure alleviates the possible overloading issues in [20] and reduces the number of setup parameters per test. The new BSG design with the proposed third-order $\Sigma-\Delta$ modulator extends the test bandwidth by a factor of 2. Experimental results show that SNDR differences between BIST results and the corresponding FFT results are less than 3 dB within a test bandwidth of 17 kHz, which is very close to the rated passband of the AUT. The hardware overhead of the proposed BIST design only consists of 13 300 gates, making it very suitable for embedded BIST applications. The BIST design can be applied to the $\Sigma-\Delta$ ADCs with other DfDT structures such as the decorrelating DfDT structure [24].

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